

# Design and Implementation of Reliable Voltage Level Shifter Using Different Current Mirroring Phenomena

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## ABSTRACT

The project focuses on creating a reliable voltage level shifter through the implementation of various current mirror topologies in VLSI technology. Current mirrors, known for their precision in copying currents between transistors, offer versatile circuit configurations for biasing, current scaling, and power management. By leveraging the unique properties of different current mirrors, the suggested solution aims to enhance voltage shifting processes, reduce power dissipation, and improve circuit stability. Power has been decreased than the existed method. It has approximately obtained as  $41.75\mu\text{W}$  for Cascode and  $18.38\mu\text{W}$  for Wilson Current Mirrors. The real-world application of this design seeks to elevate the robustness and reliability of voltage shifting in electronic circuits. This design and implementation are performed in mentor graphics (EDA tool). **Keywords :** Tanner EDA tool, Voltage level shifter, Wilson current mirror, Cascode current mirror, Robust Design, Voltage conversion, Topological Current Mirrors, Analog design.

## I. INTRODUCTION

A circuit known as a "current mirror" is made to replicate the flow of current through one active component in a circuit while maintaining a consistent output current independent of loading [12]. A fluctuating signal current may be, and occasionally is, the current being duplicated. A current-controlled

current source (CCCS) is the foundation of an ideal current mirror, which is essentially an ideal inverting current amplifier that also reverses the direction of the current. Circuits are supplied with active loads and bias currents through the employment of the current mirror. As ideal current sources do not exist, it can also be utilized to mimic a more practical current source. An analogue circuit known as the current mirror

detects the reference current and produces one or more replicas of the reference current with the same properties. Similar to the reference current source, the copied current is stable. The duplicated current may be multiples of or a fraction of the reference current ( $I_{copy} = N * I_{REF}$  or  $I_{copy} = (1/N * I_{REF})$ ), or it may be the same as the reference current ( $I_{copy} = I_{REF}$ ) [13].

The primary purpose of current mirrors in integrated circuits is for bias amplifiers. High voltage gain and biasing stability are the primary advantages for biasing the amplifiers with the current source. A MOS transistor or a basic PMOS transistor can be used to create this current source [1]. Since MOSFETs have a higher input impedance than bipolar transistor-based mirrors, they are frequently utilised in current mirrors. The high input impedance prevents it from getting into the noise. Furthermore, MOSFET is not a power-hungry component. They are perfect for properly duplicating currents because of their low output impedance and good matching properties. Thus, MOSFETs are preferred over BJTs.

Current mirror circuits can use either BJT (bipolar junction transistor) or MOSFET (metal-oxide-semiconductor field-effect transistor) devices, with a choice based on the circuit's specific requirements. BJTs are often chosen because of their high transconductance, low output impedance, and linearity, which makes them ideal for precision current mirrors. On the other hand, MOSFETs are popular for their high input impedance, low input bias current, and low output impedance, in which it can be beneficial in certain current mirror circuit applications. Ultimately, choosing between BJT and MOSFET for a current-mirrored circuit is determined by specifications such as desired efficiency, power supply constraints, and application requirements.

There are two ways to design the current mirrors. They are MOSFET-based and bipolar. Depending on the unique application and design specifications, each

type has benefits and limitations. Using these techniques MOSFET current mirrors are widely used because of their low power consumption and high input impedance.

1. Cascode Current Mirror: it is one kind of current mirror configuration that uses a cascode amplifier. To enhance the performance of a basic current mirror design, one or more transistors (often MOSFETs) are cascaded on top of it to create a cascaded current mirror.
2. Wilson Current Mirror: By offering superior output impedance and output voltage swing, the Wilson current mirror outperforms the simple current mirror. George Wilson created it in 1967. A feedback loop is incorporated into a Wilson current mirror in order to stabilize the output current in the face of fluctuations in the power supply voltage and device specifications.
3. Folded Current Mirror: To obtain better performance, a folded current mirror combines the advantages of folded cascode and cascode structures. By folding the load resistor back to the input stage in a folded current mirror, the circuit topology becomes more balanced and symmetrical.
4. Golden Current Mirror: The phrase "Golden Current Mirror" describes a particular current mirror arrangement that seeks to attain the best possible results in terms of accuracy, linearity, and stability. Given its performance attributes, the configuration referred to as "golden" is seen to be extremely desirable or optimal.

A level shifter, also known as a level converter, logic level shifter, voltage level translator, or level shifter in digital electronics, is a circuit that converts signals between one logic level and one voltage domain. The shifting often occurs between 3.3V and 5V. Level shifters are used these days to span domains between

logic, sensors, processors, and other circuit components.

## II. LITERATURE SURVEY

Current mirrors can be designed by using MOSFET's and BJT's but, most preferable is MOSFET. Because BJT has low input impedance, due to low input impedance it can enter noise easily but MOSFET has high input impedance it cannot enter noise easily. Current mirror is nothing but, it is designed to copy a current flow through an active device by controlling the current in another active device [1]. Level shifting means which converts low level voltage domain to high level voltage domain or vice versa. For designing the level shifter there are mainly topologies one is cross coupled level shifter and another topology is current-mirror based level shifter [2]. While cross coupled operation is performing the switching operation then there will be effect on speed as well as energy [3]. So due to this effect considering of current mirror is the best techniques for voltage level shifting. In current-mirror based level shifter while the switching operation is performing then the speed and energy will not affect and the energy and power will decrease [5]. The robust level is designed by using the pull up networks which are connected in parallel to reduce the power and energy per transition [5]. Compare the analysis between different techniques of current-mirror based level shifter the techniques like cascode and Wilson current mirrors. They are used to compare the analysis of power and energy per transition.

The drawback in level shifter based current mirror can reside in the strong contention current between pull-up and pull-down networks, particularly when VDDL is in the sub-threshold region [7]. So, the next implementation can be done by using the cascode based current mirror using the level shifter. By implementing this circuit, the area can be optimized. Power can also be reduced far better as in VLSI (low

power VLSI). And also, the benefits of this mirror can provide better matching of output currents and larger output resistance. So, Cascoded current mirror can match the input and outputs.

Wilson current mirror can also be designed by cross-coupled and current-mirror based level shifter. By scaling down, short circuit power of the circuit reduces along with static power, but there is huge limitation of scaling down supply voltage because it limits the speed of the system [4]. It also eliminates the shortcoming of typical Wilson current mirror level shifters in utilizing the current mirror which uses a high aspect ratio are considerably saves the power and area of the design [2]. The proposed Wilson current mirror can reduce the current far better than cascode current mirror which will be apt for low power VLSI technology. The full implementation of the proposed WCMLS with Reflected Output where the conventional Wilson current mirror Level shifters' circuit sizing is minimized [2].

## III. IMPLEMENTATION METHODOLOGY

### Existed Methods:

#### 1. Basic Current mirror:

In an integrated circuit, a current mirror is used to precisely (accurately) copy a reference current. Current mirror technology is used to design monolithic integrated circuits, or silicon single crystals. The reference current must remain constant throughout the n linked transistors in a cascaded transistor configuration; else, the current mirror is meaningless [13]. Circuits can also receive bias currents and active loads from the current mirror. A basic current mirror's drawback is that it can be sensitive to changes in temperature and mismatched transistor parameters, which could result in inaccurate mirrored current.

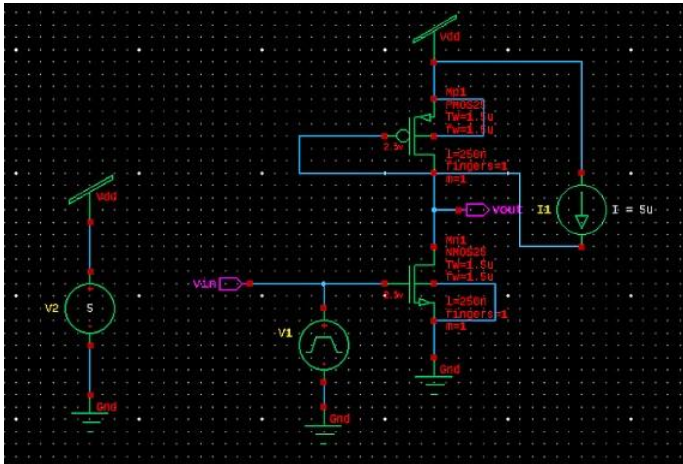


Fig 1: Basic Current Mirror Schematic

| Vin  | Mp1 | Mn1 |
|------|-----|-----|
| LOW  | ON  | OFF |
| HIGH | OFF | ON  |

Table 1: Working of Basic Current Mirror

## 2. Cross-Coupled based level shifter:

CC-based level shifters are a half-latch method which can absorb near-zero leakage current from the PUN (Pull-Up Network) and PDN (Pull-Down Network) networks. Switching reduces both speed and energy efficiency. Up-converting sub-threshold voltages increases the need for more NMOSFET transistors. Ultra-low voltage level shifters are in high demand in heterogeneous voltage domains [5]. This can provide high input voltage and low output voltage which may affect the power.

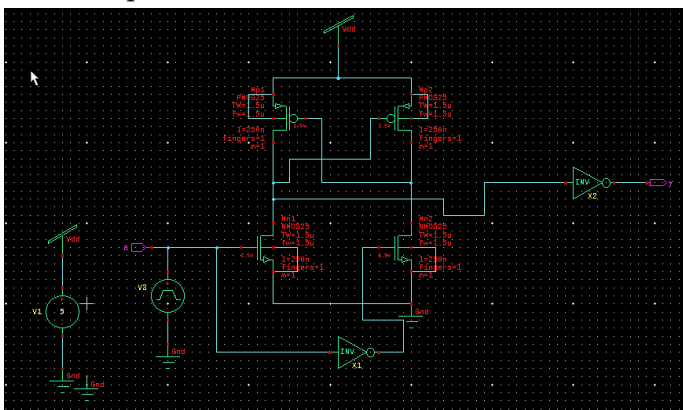


Fig 2: Cross-Coupled based level shifter Schematic

| Input Voltage | Transistors |     |     |     |
|---------------|-------------|-----|-----|-----|
| Vin(V)        | Mp1         | Mp2 | Mn1 | Mn2 |
| LOW           | ON          | OFF | OFF | ON  |
| HIGH          | OFF         | ON  | ON  | OFF |

Table 2: Working of Cross-Coupled level shifter

## 3. Current-Mirror based level shifter:

The PMOSFET transistors P1 and P2 have their gate terminals connected to each other as well as to the drain terminal of P1. In other words, when the gate to source voltage of two exactly similar transistors are equivalent, it implies that the drain current flowing through them is also equivalent. Most Wilson Mirror circuits are based on CM topology which reduces the delay and power consumption significantly [5].

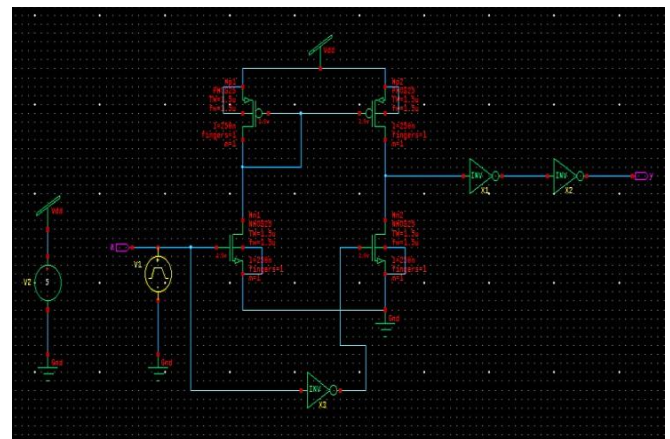


Fig 3: Current Mirror based level shifter Schematic

| Input Voltage(V) | Transistors |     |     |     |
|------------------|-------------|-----|-----|-----|
| Vin              | Mp1         | Mp2 | Mn1 | Mn2 |
| LOW              | OFF         | OFF | OFF | ON  |
| HIGH             | ON          | ON  | ON  | OFF |

Table 3: Working of Current Mirror based level shifter

#### 4. Robust Based Voltage Level Shifter:

In electronic circuits, a strong level shifter is essential, particularly when connecting various voltage domains. Its function is to convert signals between different voltage levels while maintaining stability, dependability, and security from different electrical risks.

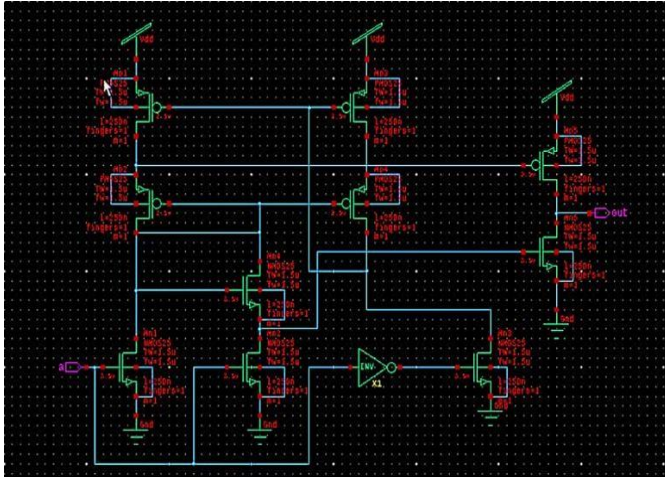


Fig 4: Robust Level shifter

| INP<br>UT | TRANSISTORS |         |         |         |         |         |         |         |         |
|-----------|-------------|---------|---------|---------|---------|---------|---------|---------|---------|
| V         | M<br>p1     | M<br>p2 | M<br>p3 | M<br>p4 | M<br>p5 | M<br>n1 | M<br>n2 | M<br>n3 | M<br>n4 |
| 0         | 1           | 1       | 1       | 0       | 0       | 0       | 0       | 1       | 1       |
| 1         | 0           | 0       | 1       | 1       | 1       | 1       | 1       | 0       | 0       |

- 1=ON
- 0=OFF

Table 4 : Working of Robust Shifter

#### IV. Proposed Methods

##### 1.Cascoded current-mirror based level shifter:

Cascode Current Mirror is another topology in which it can be used instead of cross-coupled CM technique[5]. This current mirror topology is improved with an extra transistor in the cascode design. Usually connected at the top of the output transistor, this second transistor

is attached in a common source configuration (for MOSFETs). The proposed cascode current mirror (CM) based circuit (CCMLS) has a conversion range from 90 mV to 1.8 V, which means that it can level shift up a voltage as low as 90 mV to a larger supply voltage of 1.8 V [5]. This circuit is proposed in order to reduce delay and improve the conversion range which in turn leads to a more efficient design [5]. By having this design, the power and energy per transition can be improved better than the previous designs.

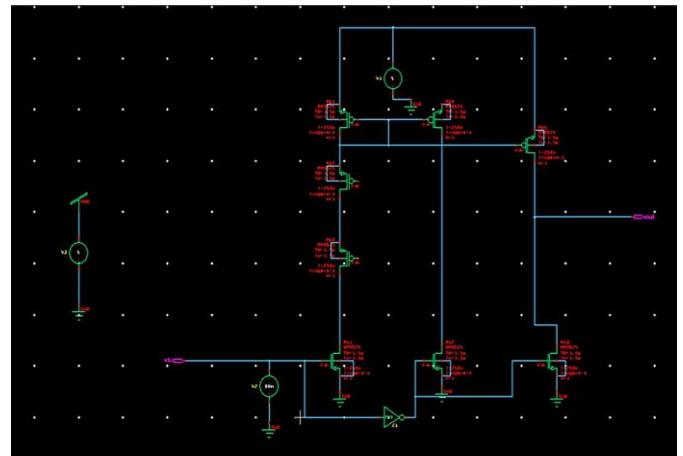


Fig 5: Cascode Current Mirror based level shifter Schematic

| Input<br>Voltage | Transistors |         |         |         |         |         |         |             |
|------------------|-------------|---------|---------|---------|---------|---------|---------|-------------|
| Vin              | MP<br>1     | MP<br>2 | Mp<br>3 | Mp<br>4 | Mp<br>5 | Mn<br>1 | Mn<br>2 | M<br>N<br>3 |
| LOW              | 0           | 1       | 1       | 0       | 1       | 0       | 1       | 1           |
| HIGH             | 1           | 0       | 0       | 1       | 0       | 1       | 0       | 0           |

- 1=ON
- 0=OFF

Table 5: Working of Cascode current mirror-based level shifter

##### 2.Wilson current mirror-based level shifter:

Since, there is a tradeoff in cascade current mirror i.e.

Since, there is a tradeoff in cascade current mirror i.e. it with the Wilson current-mirror based level shifter [5]. To further reduce power consumption, a PMOS diode Mp1 is connected in series with Mn1 [11]. The output buffer is the snap input inverter that reduces short circuit current via the buffer. The Mp1 diode produces a voltage discrepancy between nodes Q1 and Q4, preventing the output buffers Mn3 and Mp5 from turning on at the same time [11]. The inverter has been eliminated from the input in the proposed Level shifter, and Mn2 has been used to restore it as a pass transistor [10].

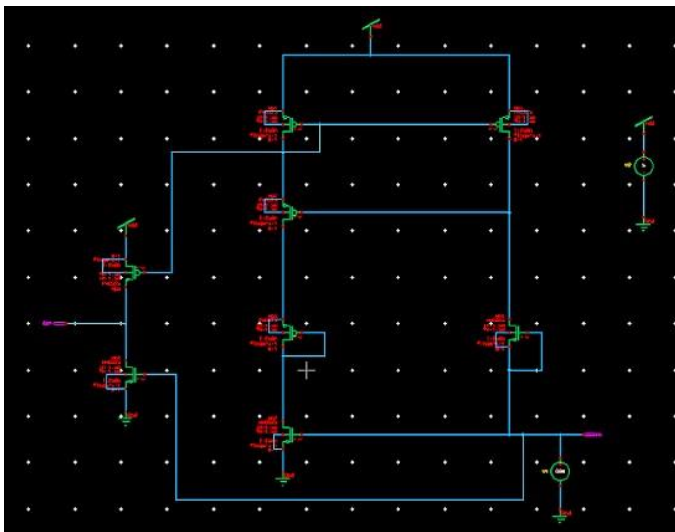


Fig 6: Wilson current-mirror based level shifter Schematic

| Vin  | Mp1 | Mn1 |
|------|-----|-----|
| Low  | ON  | OFF |
| High | OFF | ON  |

Table 6 : Working of Wilson Current Mirror based level shifter

## II COMPARISON RESULTS AND DISCUSSION

Cascode Current Mirror is another topology in which it can be used instead of cross-coupled CM technique [5]. This current mirror topology is improved with an extra transistor in the cascode design. Usually

connected at the top of the output transistor, this second transistor is attached in a common source configuration (for MOSFETs). The proposed cascode current mirror (CM) based circuit (CCMLS) has a conversion range from 90 mV to 1.8 V, which means that it can level shift up a

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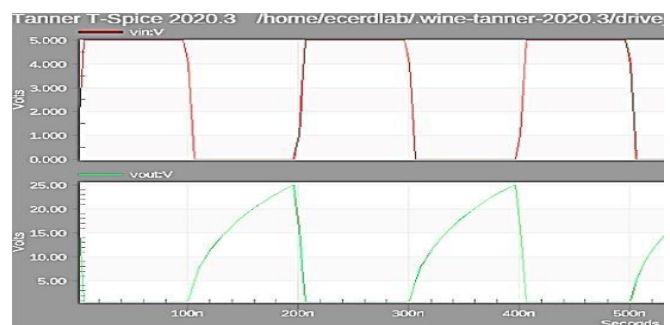


Fig 7: Basic Current Mirror wave form

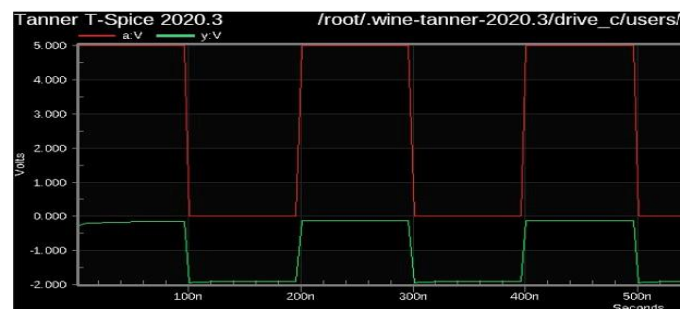


Fig 8 : Cross-Coupled based level shifter waveform

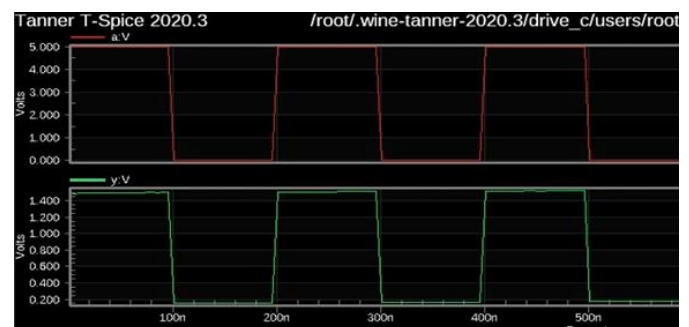


Fig 9: Current-mirror based level shifter wave form

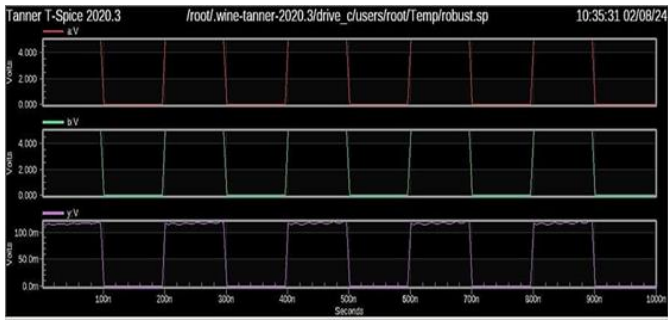


Fig 10: Robust based Voltage Level Shifter

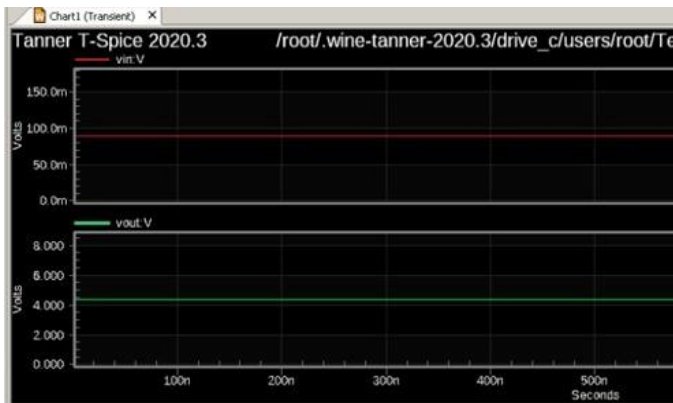


Fig 11: Cascode Current Mirror based level shifter wave form

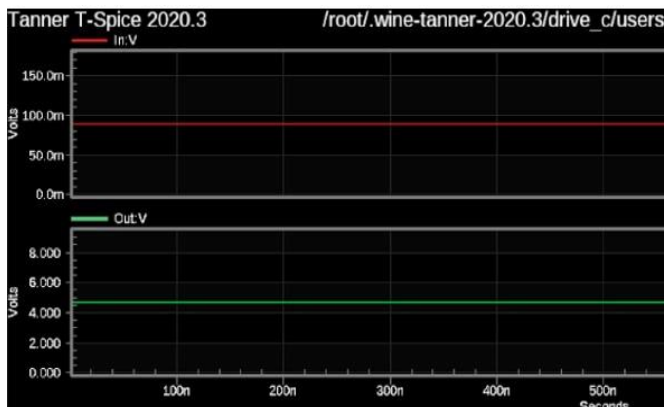


Fig 12: Wilson Current Mirror based level shifter

| S.NO | CURRENT MIRROR TECHNIQUES       | Average power | Energy per transition |
|------|---------------------------------|---------------|-----------------------|
| 1    | ROBUST LEVEL SHIFTER            | 53.07mW       | 5.307nJ               |
| 2    | CASCODED CM BASED LEVEL SHIFTER | 41.75μW       | 4.175pJ               |
| 3    | WILSON CM BASED LEVEL SHIFTER   | 18.38μW       | 1.838pJ               |

Table 7: Comparison of Current Mirrors

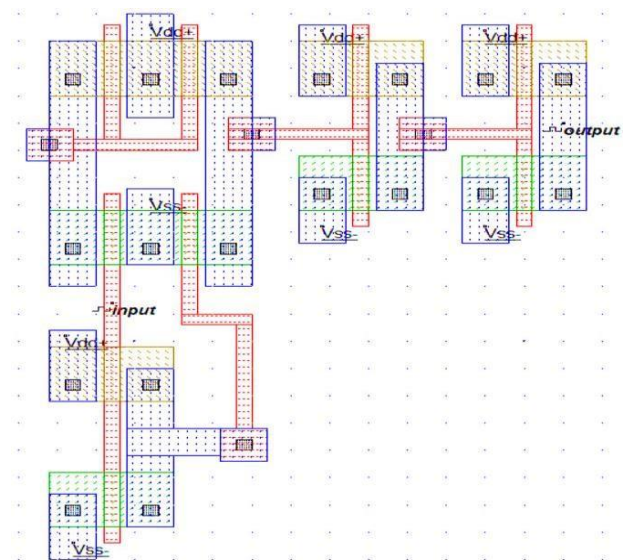


Fig 13: Layout of Current Mirror based level shifter

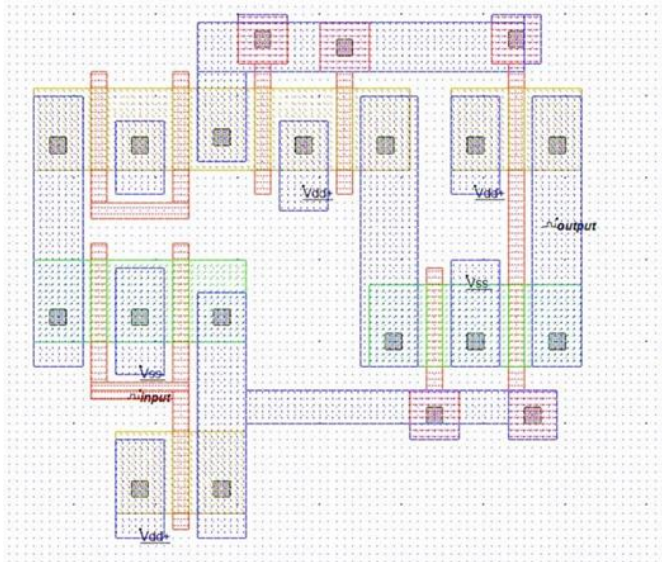


Fig 14: Layout of Cascode Current Mirror based level shifter

## V. CONCLUSION

The main aim of this design is to implement and extract the parameters (power, energy per transition and delay) for various voltage level shifters current mirroring phenomena. It gives low power by implementing various current mirrors. These designs give accurate and precised values. By using voltage level shifters, it can give voltage supply limitations, wide bandwidth and low-power consumption. Overall, these implementations are represented as analogue and Integrated circuit

## VI. REFERENCES

- [1]. Chen, C., Labrousse, D., Lefebvre, S., Petit, M., Buttay, C., & Morel, H. (2015). Study of short-circuit robustness of SiC MOSFETs, analysis of the failure modes and comparison with BJTs. *Microelectronics Reliability*, 55(9- 10), 1708-1713.
- [2]. Luo, S. C., Huang, C. J., & Chu, Y. H. (2014). A wide-range level shifter using a modified Wilson current mirror hybrid buffer. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 61(6), 1656-1665.
- [3]. Kabirpour, S., & Jalali, M. (2018). A low-power and high-speed voltage level shifter based on a regulated cross-coupled pull-up network. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 66(6), 909-913..
- [4]. Fassio, L., Settino, F., Lin, L., De Rose, R., Lanuzza, M., Crupi, F., & Alioto, M. (2020). A robust, high-speed and energy-efficient ultralow-voltage level shifter. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 68(4), 1393-1397.
- [5]. Jaisinghani, D., Aarthi, U. S., & Pande, K. S. (2022, October). A cascode current mirror based 90 mv to 1.8 v level shifter with alleviated delay. In *2022 International Conference on Distributed Computing, VLSI, Electrical Circuits and Robotics (DISCOVER)* (pp. 45-50). IEEE.
- [6]. Ramirez-Angulo, J., Carvajal, R. G., & Torralba, A. (2004). Low supply voltage high-performance CMOS current mirror with low input and output voltage requirements. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 51(3), 124-129.
- [7]. You, H., Yuan, J., Tang, W., Qiao, S., & Hei, Y. (2020). An energy-efficient level shifter for ultra low-voltage digital LSIs. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 67(12), 3357-3361.
- [8]. Minch, B. A. (2007, May). Low- voltage Wilson current mirrors in CMOS. In *2007 IEEE International Symposium on Circuits and Systems* (pp. 2220-2223). IEEE.
- [9]. Aggarwal, B., Arora, Y., & Dhona, J. K. (2021). Bandgap current reference using widlar current source. *Indian Journal of Engineering and Materials Sciences (IJEMS)*, 27(4), 934-938.
- [10]. Lütke-meier, S., & Rückert, U. (2010). A subthreshold to above-threshold level shifter comprising a Wilson current mirror. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 57(9), 721-724.

- [12]. Kim, T. T. H. (2018). An area and energy efficient ultra-low voltage level shifter with pass transistor and reduced-swing output buffer in 65-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 65(5), 607-611.
- [13]. Aggarwal, B., Gupta, M., Gupta, A. K., & Bansal, S. (2014). A very high-performance compact CMOS current mirror. Analog Integrated Circuits and Signal Processing, 81, 367-375.
- [14]. Razavi, B. (2005). Design of analog CMOS integrated circuits. Tsinghua University Press Co., Ltd