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Design of 4-Bit Universal Shift Register Using Reversible Gates

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ABSTRACT

Power dissipation is one of the important factor in digital circuit design. Landauer's principle states that logic computations which are not reversible necessarily generate KT*ln2 Joules of heat energy for every bit of information that is lost, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. Reversibility is the property of digital circuits in which there is one-to-one mapping between the inputs and the output vectors that is for each input vector there is a unique output vector and vice-versa. Thus one of the primary motivations for adopting reversible logic lies in the fact that it can provide a logic design methodologies for designing low power dissipating circuits. Fredkin gate, Feynman Gate is popularly used reversible logic gate which are used to implement various sequential circuits which are basic for design of digital circuits.

Keywords: Landauer's Principle, Reversibility, Fredkin Gate, Feynman Gate, R-USR, Quantum Cost, Low Power.

I. INTRODUCTION

A gate is considered to be reversible only if for each distinct input there is a distinct output assignment. Thus inputs to reversible gates can be uniquely determined from its outputs. A reversible logic gates must have the same number of inputs and outputs and they satisfy the property of bijective. Some of the major problems with reversible logic synthesis are fan outs cannot be used, and also feedbacks from gate outputs to inputs are not permitted.

Difference between conventional gate and reversible gate:

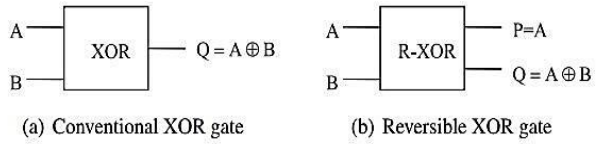

Figure 1: Block Diagram of Conventional Gate and Reversible Gate

The difference between the conventional gate and the reversible gate is shown in the above block diagram. Figure 1(a) is a conventional XOR gate with A, B as inputs and Q as output. In this gate input signals A, B cannot be obtained from the output signals. Figure 1(b) is a reversible XOR gate with A, B as inputs and P, Q as outputs. In reversible gates reverse computation can be carried. The signals A, B can be obtained from the Output signals P, Q here output signal p is the copy of the A and output signal Q is the XOR operation between

The inputs A and B. Truth tables for conventional and reversible gates are in the Table 1.

Table 1: Truth Table for Conventional Gate and Reversible Gate

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

(a) C- XOR

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

(b) R-XOR

II. METHODS AND MATERIAL

2. Basic Reversible Gates

2.1 Feynman Gate:

The Feynman gate (FG) is a 2 inputs 2 outputs reversible gate having the mapping (A, B) to (P=A, Q=A⊕B) where A, B are the inputs and P, Q are the Outputs respectively. It has a quantum cost of 1. The block diagram of the Feynman is shown in figure 2. It can be used for generating the complement of a signal and also for generating exact copier of signal which is shown in in the below figure 3.

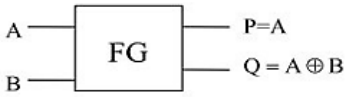

Figure 2: Feynman Gate

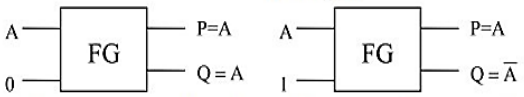

Figure 3: FG Gate as Signal Copier and Complementing the Input Signal

2.2 FREDKIN GATE:

Fredkin gate is one of the basic reversible gate. It is a (3x3) conservative reversible gate, having the mapping (A, B, C) to (P=A, Q=A'B+AC, R=AB+A'C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. It is called a 3x3 gate because it has three inputs and three outputs.

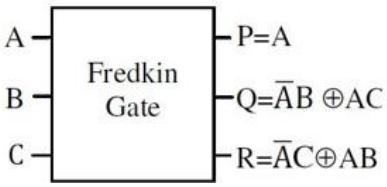

Figure 4: Block Diagram of Fredkin Gate

3. Reversible Universal Shift Register

Universal shift register is a register that has both shifts and parallel load capabilities depending upon the control bits S1, S0.The USR circuit is designed by using the basic reversible gates such as Fredkin gate and Feynman gate. Reversible universal shift register can be constructed using asynchronous set/reset Reversible D flip flop and reversible 4:1 MUX. The circuit diagram and truth table for the reversible D Flip flop is shown in the figure 5 and table 2.

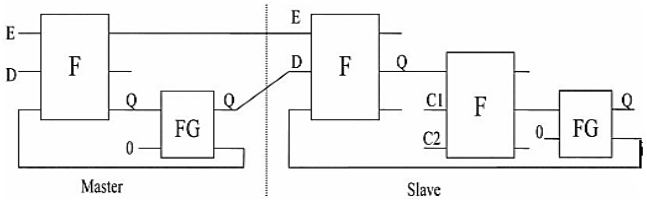

Figure 5: Fredkin Gate based Reversible D flip flop

C1	C2	CLK/E	D	Q
0	1	↓	1	1
0	1	↓	0	0
1	1	X	X	1
0	0	X	X	0

Table 2: Functional table for reversible D flip flop

The circuit diagram and truth table for reversible 4:1 MUX is shown in the figure 6 and table 3.

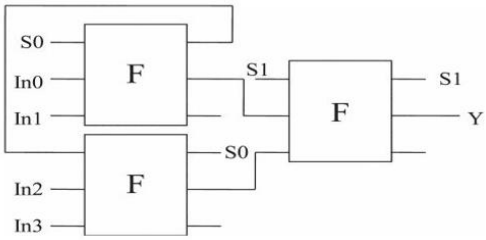

Figure 6: Fredkin Gate based reversible 4:1 MUX

Table 3: Functional table for Reversible 4:1 MUX

S1	S0	Y
0	0	In0
0	1	In1
1	0	In2
1	1	In3

The shift register consists of 4 reversible D flip-flops with asynchronous reset capability, and four reversible 4:1 multiplexers (R-4:1MUX) that work as a control unit. The design of a 4 bit reversible multiplexer has 3 Fredkin gates and 5 garbage outputs. Another component in the design of a reversible universal shift register is reversible D flip-flops with asynchronous reset capability. We need C1 and C2 signals to be passed as inputs to the next D flip-flops. In each D flip-flop, the copies of the C1 and C2 signals can be generated by using the 2 Feynman gates, one for C1 and one for

C2.The circuit diagram for 4-bit Reversible USR is shown in the figure 6. Modes of operations of the reversible USR is shown in the table 4.

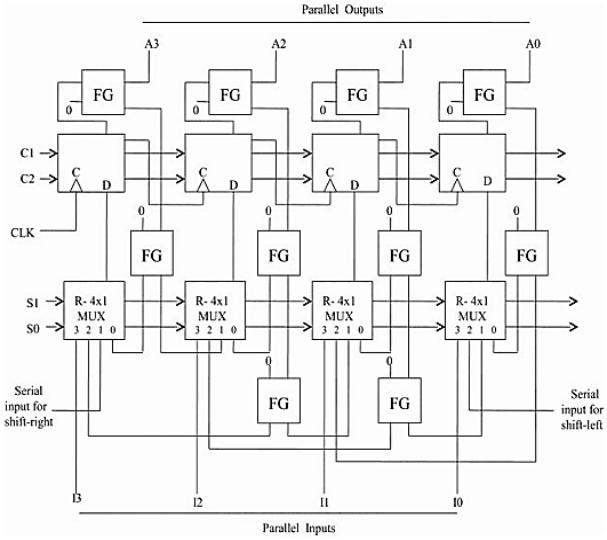

Figure 6: 4-Bit Reversible Universal Shift Register

Table 4: Modes of operation of Reversible Universal Shift Register

S1	S0	OPERATION
0	0	INHIBIT CLOCKING(DO NOTHING)
1	0	SHIFT LEFT
0	1	SHIFT RIGHT
1	1	PARALLEL LOADING

III. RESULTS AND DISCUSSION

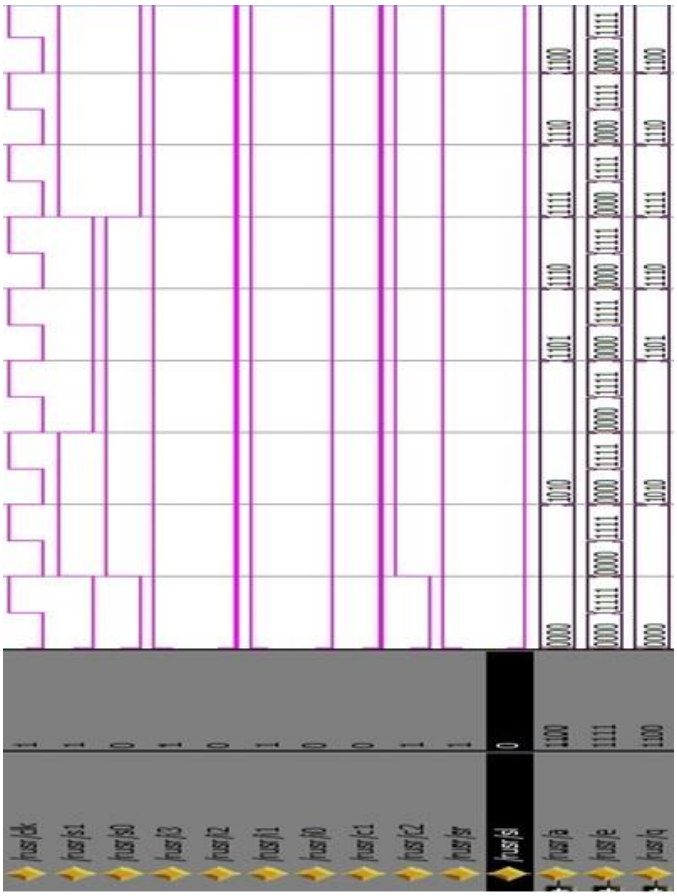

Figure 7: Simulation wave form for reversible USR

Table 5: Performance summary between conventional USR and Reversible USR

Metric		Conventional Universal Shift Register	Reversible Universal Shift Register
power	Logical	0.025 watts	0.019 watts
	Signalling	0.046 watts	0.041 watts
Quantum cost		46	42

IV. CONCLUSION

Reversible universal shift register using Fredkin gate and Feynman gate are implemented, simulated and compared it with the conventional universal shift register using Vivado tool. The quantum cost for 4-bit

reversible USR is 42 and quantum cost for 4-bit conventional USR is 46. The power required to implement the logic using the reversible USR is 0.019 watts and power required to implement the logic using the conventional USR is 0.025 watts. The signalling power required for Reversible USR and conventional USR are 0.041 and 0.046 watts

Digital systems have 32 or 64 or 128 bit processors. The shift registers used in that processors are also having higher data input bits. With the increase in the number of data inputs the power required and number of components required to implement the shifting logic using reversible USR will be less when compared with the conventional USR and power dissipated is also less using the reversible USR. Thus reversible universal shift register can be extensive used in the low power designs.

V. FUTURE SCOPE

The reversible gates can be used for the design of low power applications circuits. The proposed design can be extended to 8 bit USR and even to the higher bits by cascading the 4- bit USR circuit which is shown in this paper. This paper can be extended to a wide area of applications by applying this set of concepts to the larger logical circuits such as reversible ALU's, RAM etc. Reversible circuits also find application in the domain of quantum computation, optical computing and low power VLSI circuits.

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