© 2016 IJSRSET | Volume 2 | Issue 2 | Print ISSN : 2395-1990 | Online ISSN : 2394-4099
Themed Section: Engineering and Technology

Performance Analysis of 1-D DFT & 1-D DCT using CORDIC Algorithm

Neelam Sharma, Vipul Agrawal, Sourabh Sharma

Department of ECE, Rajiv Gandhi Proudyogiki Vishwavidyalaya, Bhopal
Trinity Institute of Technology & Research, Bhopal, Madhya Pradesh, India

ABSTRACT

This paper describes the design of a low-power DCT (Discrete Cosine Transform) architecture using varies techniques. The low-power design is one of the most important challenges to maximize battery life in portable devices and to save the energy during system operation. Discrete Cosine Transform (DCT) is one of the most popular lossy techniques used in image and video compression standards. Several algorithms have been proposed to implement the DCT. So we have to implement the multiplier-less CORDIC algorithm. CORDIC (Coordinate Rotation Digital Computer) algorithm is a class of shift- add algorithm for rotation vector and plan which is usually used for the calculation of trigonometric functions. The whole design is simulated with Xilinx ISE 14.1 software and results are completely consistent with DCT.

Keywords: Discrete Cosine Transform, Discrete Fourier Transform, Coordinate Rotation Digital Computer

I. INTRODUCTION

For a long time the field of Digital Signal Processing has been dominated by Microprocessors. This is mainly because they provide designers with the advantages of single cycle multiply-accumulate instruction as well as special addressing modes. Although these processors are cheap and flexible they are relatively slow when it comes to performing certain demanding signal processing tasks e.g. Image Compression, Digital Communication and Video Processing. Of late, rapid advancements have been made in the field of VLSI and IC design. As a result special purpose processors with custom-architectures have come up. Higher speeds can be achieved by these customized hardware solutions at competitive costs. To add to this, various simple and hardware-efficient algorithms exist which map well onto these chips and can be used to enhance speed and flexibility while performing the desired signal processing tasks [1][2][3]. One such simple and hardware-efficient algorithm is CORDIC, an acronym for Coordinate Rotation Digital Computer, proposed by Jack E Volder [4. CORDIC uses only Shift-andAdd arithmetic with table Look-Up to implement different functions. By making slight adjustments to the initial conditions and the LUT values,it can be used to efficiently implement Trigonometric,Hyperbolic, Exponential functions, Coordinate Transformations etc. using the same hardware. Since it uses only shift-add arithmetic, VLSI implementation of such an algorithm is easily achievable. DCT algorithm has diverse applications and is widely used for Image compression. Implementing DCT using CORDIC algorithm reduces the number of computations during processing, increases the accuracy of reconstruction of the image, and reduces the chip area of implementation of a processor built for this purpose. This reduces the overall power consumption. FPGA provides the hardware environment in which dedicated processors can be tested for their functionality. They perform various high-speed operations that cannot be realized by a simple microprocessor. The primary advantage that FPGA offers is On-site 2 programmability. Thus, it forms the ideal platform to implement and test the functionality of a dedicated processor designed using CORDIC algorithm [5].

The advances in IC technology have great interests in developing special purpose, parallel processor arrays such systolic arrays have been extensively used. The basic arithmetic computation of these parallel arrays has often been implemented with a MAC, because these operations arise in DSP applications.The reduction in hardware cost also motivated the development of sophisticated signal processing algorithms which need the evaluation of functions such as trigonometric and

logarithmic functions, which cannot be evaluated efficiently with MAC based arithmetic units. So when signal processing algorithms incorporate these elementary functions it is sure to observe significant performance failure. So an arithmetic computing algorithm known as CORDIC (Coordinate Rotation Digital Computer) has received great attention, as it offers an iterative formulation to efficiently calculate each of these elementary functions. Specially, all the evaluation tasks in CORDIC are formulated as a rotation of vectors in various Coordinate systems. By varying a few parameters, the same CORDIC processor is capable of iteratively calculates these elementary functions using the same hardware in the same amount of implementation of pipelined VLSI array processors.

II. METHODS AND MATERIAL

A. Literature Review

CORDIC or Coordinate Rotation Digital Computer is a simple and hardware-efficient algorithm for the implementation of various elementary,especially trigonometric, functions. Instead of using Calculus based methods such as polynomial or rational functional approximation, it uses simple shift, add, subtract and table look-up operations to achieve this objective. The CORDIC algorithm was first proposed by Jack E Volder in 1959. It is usually implemented in either Rotation mode or Vectoring mode. In either mode, the algorithm is rotation of an angle vector by a definite angle but in variable directions. This fixed rotation in variable direction is implemented through an iterative sequence of addition/subtraction followed by bit-shift operation. The final result is obtained by appropriately scaling the result obtained after successive iterations. Owing to its simplicity the CORDIC algorithm can be easily implemented on a VLSI system.

Hardware requirement and cost of CORDIC processor is less as only shift registers, adders and look-up table (ROM) are required Number of gates required in hardware implementation, such as on an FPGA, is minimum as hardware complexity is greatly reduced compared to other processors such as DSP multipliers It is relatively simple in design No multiplication and only addition, subtraction and bit-shifting operation ensures simple VLSI implementation. Delay involved during processing is comparable to that during the implementation of a division or square-rooting operation. Either if there is an absence of a hardware multiplier (e.g. uC, uP) or there is a necessity to optimize the number of logic gates (e.g. FPGA) CORDIC is the preferred choice.

B. Discrete Cosine Transform

Discrete Cosine Transformation (DCT) is the most widely used transformation algorithm. DCT, first proposed by Ahmed [9] et al, 1974, has got more importance in recent years, especially in the fields of Image Compression and Video Compression. This chapter focuses on efficient hardware implementation of DCT by decreasing the number of computations, enhancing the accuracy of reconstruction of the original data, and decreasing chip area. As a result of which the power consumption also decreases. DCT also improves speed, as compared to other standard Image compression algorithms like JPEG.

DCT Output:

$$F(0) = 0.5(f(0)+f(1)+f(2)+f(3)+f(4)+f(5)+f(6)+f(7))\cos\frac{\pi}{4}$$

$$F(1) = 0.5[\{(f(0)-f(7)\}\cos\frac{\pi}{16}+\{f(1)-f(6)\}\cos\frac{3\pi}{16}+\{f(2)-f(5)\}\cos\frac{5\pi}{16}+\{f(3)+f(4)\}\cos\frac{7\pi}{16}]$$

$$F(2) = 0.5[\{(f(0)-f(3)-f(4)+f(7)\}\cos\frac{2\pi}{16}+\{f(1)-f(2)-f(5)+f(6)\}\cos\frac{6\pi}{16}]$$

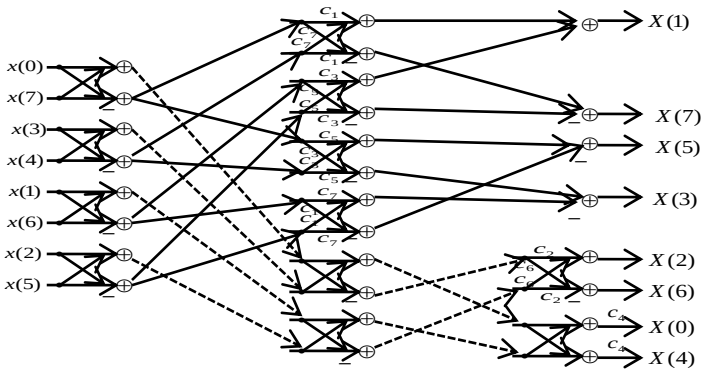


Figure 1: 8-point Discrete Cosine Transform

$$F(3) = 0.5[\{(f(0) - f(7)\}\cos\frac{3\pi}{16} + \{f(6) - f(1)\}\cos\frac{7\pi}{16} + \{f(5) - f(2)\}\cos\frac{\pi}{16} + \{f(4) + f(3)\}\cos\frac{5\pi}{16}]$$

$$F(4) = 0.5[(f(0) + f(3) + f(4) + f(7) - f(1) - f(2) - f(5) - f(6))\cos\frac{\pi}{4}]$$

$$F(5) = 0.5[\{(f(0) - f(7)\}\cos\frac{5\pi}{16} + \{f(6) - f(1)\}\cos\frac{\pi}{16} + \{f(2) - f(5)\}\cos\frac{7\pi}{16} + \{f(3) + f(4)\}\cos\frac{3\pi}{16}]$$

$$F(6) = 0.5[\{(f(0) - f(3) - f(4) + f(7)\}\cos\frac{6\pi}{16} - \{f(1) - f(2) - f(5) + f(6)\}\cos\frac{2\pi}{16}]$$

$$F(7) = 0.5[\{(f(0) - f(7)\}\cos\frac{7\pi}{16} + \{f(6) - f(1)\}\cos\frac{5\pi}{16} + \{f(2) - f(5)\}\cos\frac{3\pi}{16} + \{f(4) + f(3)\}\cos\frac{\pi}{16}]$$

Discrete Fourier Transform (DFT)

Transforms such as discrete fourier transform (DFT) are a major block in many communication systems like OFDM, etc. DFT is also considered as one of the major tools to perform frequency analysis of discrete time signals. A discrete time sequence can be represented by samples of its spectrum in the frequency domain, using DFT.The Discrete Fourier Transform is a continuous Fourier transform for the case of discrete functions. Given a real sequence of { x_n }, the DFT expresses them as a sequence { X_k } of complex numbers, the mathematical representation of the transform is:

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-j2\pi kn/N}, \qquad n = 0,1,2,\ldots\ldots\ldots N-1$$

Using simpler notation of equation is,

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{kn}$$

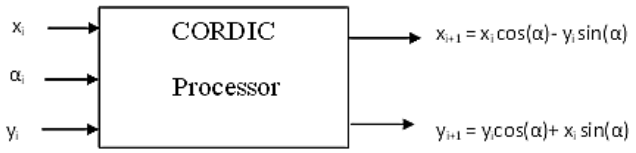
The quantity W_N^{nk} is defined as in equation

$$W_N^{nk} = e^{-j2\pi k/N}$$

III. RESULTS AND DISCUSSION

Cordic Algorithm

The simple form of CORDIC is based on observation that if a unit length vector with at (x,y)=(1,0) is rotated by an angle αdegrees, its new end point will be at $(x, y) = (\sin\alpha, \cos\alpha)$ thus coordinates can be computed by finding the coordinates of new end point of the vector after rotation by an angle α. Rotation of any (x , y) vector:



Basic equation of CORDIC algorithm

$$x_{i+1} = x_i\cos(\alpha) - y_i\sin(\alpha) \qquad (1)$$

$$y_{i+1} = y_i\cos(\alpha) + x_i\sin(\alpha) \qquad (2)$$

Rearrange Equations

$$x_{i+1} = \cos(\alpha)\,[x - y\tan\alpha] \qquad (3)$$

$$y_{i+1} = \cos(\alpha)[y + x\tan\alpha] \qquad (4)$$

$$\tan\alpha = \frac{\sin\alpha}{\cos\alpha}$$

Rotations and Pseudo Rotation

Consider the vector $OE^{(i)}$ in figure having one end point at O and other $E^{(i)}$ with Co-ordinates(x_i, y_i). If $OE^{(i)}$ is rotated the origin by angle α^i as shown in figure thaw end point $OE^{(I+1)}$ will havecoordinates (x_{i+1}, y_{i+1}) satisfying.

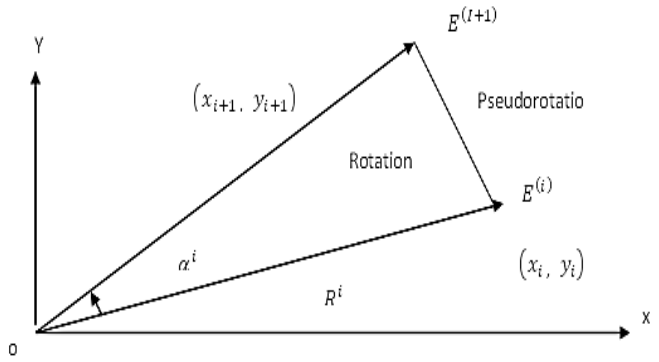


Figure 2. A pseudo rotation steps in CORDIC

Simulation Result

All the designing and experiment regarding algorithm that we have mentioned in this paper is being developed on Xilinx 14.1i updated version. Xilinx 9.2i has couple of the striking features such as low memory requirement, fast debugging, and low cost. The latest release of ISE™ (Integrated Software Environment) design tool provides the low memory requirement approximate 27 percentage low. ISE 14.1i that provides advanced tools like smart compile technology with better usage of their computing hardware provides faster timing closure and higher quality of results for a better time to designing solution.

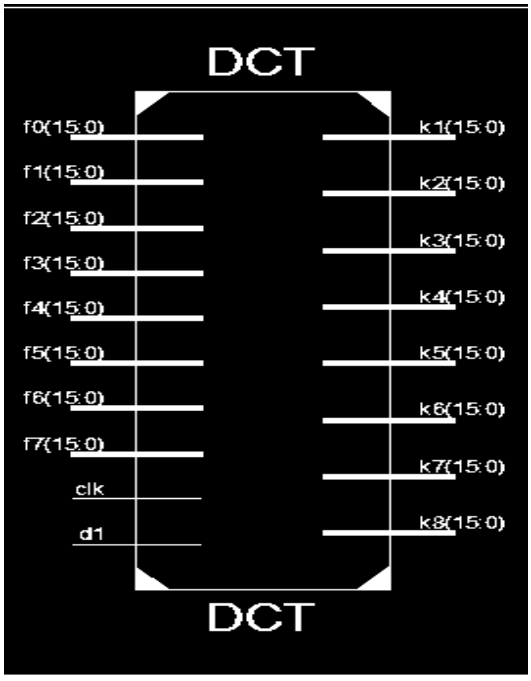


Figure 3: Resister transfer Level (RTL) View of 8-point DCT

Table 1: Device Utilization

	Mamatha I et al.	Proposed
Number of Register	1102	342
Numbe of Slice LUTs	2541	1303
LUT-FF Pairs	958	236
Number of DSP 48Es	72	-
Number of IOBs	1588	258
Maximum Frequency Operation	224.9MHz	184.556 MHz

```
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 5.418ns (Maximum Frequency: 184.556MHz)
   Minimum input arrival time before clock: 10.476ns
   Maximum output required time after clock: 11.789ns
   Maximum combinational path delay: 13.795ns
```

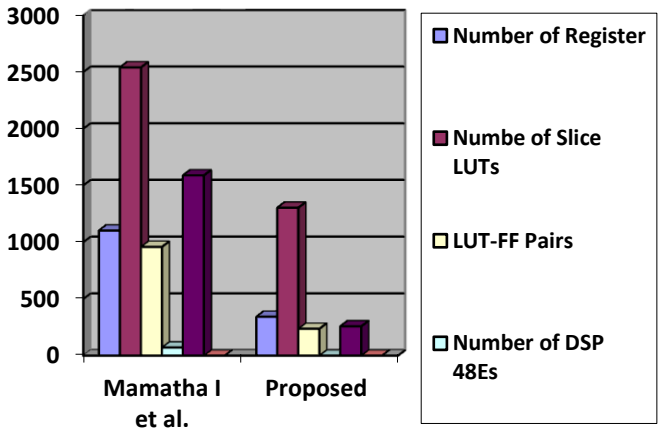


Figure 4: Bar Graph of the 8-point DCT

IV. CONCLUSION

In literature survey we found that CORDIC based DCT algorithm is the best algorithm in the existing algorithm. So we are implementation to CORDIC based DCT algorithm in this paper. The performance evaluation of the various sub modules are carried out using Xilinx 14.1 ISE Simulator and it was found that the circuits designed using DCT logic showed a reduced delay and power. As a future work more arithmetic and logical function can be used.

V. REFERENCES

[1] Mamatha I, Nikhita Raj J, Shikha Tripathi, Sudarshan TSB, "Systolic Architecture Implementation of 1D DFT and 1D DCT", 978-1-4799-1823-2/15/$31.00 ©2015 IEEE.

[2] Liyi Xiao Member, IEEE and Hai Huang, "Novel CORDIC Based Unified Architecture for DCT and IDCT", 2012 International Conference on Optoelectronics and Microelectronics (ICOM) 978-1-4673-2639-1/12/$31.00 ©2012 IEEE.

[3] Shymna Nizar N.S,Abhila and R Krishna, "An Efficient Folded Pipelined Architecture For Fast Fourier Transform Using Cordie Algorithm", 2014 IEEE International Conference on Advanced Communication Control and Computing Technologies (lCACCCT) IEEE.

[4] E. Jebamalar Leavline, S.Megala2 and D.Asir Antony Gnana Singh, "CORDIC Iterations Based Architecture for Low Power and High Quality DCT", 2014 International Conference on Recent Trends in Information Technology 978-1-4799-4989-2/14/$31.00 © 2014 IEEE.

[5] Satyasen Panda, "Performance Analysis and Design of a Discreet Cosine Transform processor Using CORDIC algorithm", 2008-2010.

[6] Keshab K. Parhi, "VLSI Digital Signal Processing Systems, design and implementation", Wiley.

[7] Deepika Ghai, "COMPAATIVE ANALYSIS OF VARIOUS CORDIC TECHNIQUES", June, 2011.

[8] Yuan-Ho Chen *et al*, "A High Performance Video Transform Engine by Using Space- Time Scheduling Strategy", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 20, NO. 4, APRIL 2012.

[9] Xue Liu, Feng Yu, Ze-ke Wang, " A Pipelined Architecture for Normal I/O Order FFT", Journal of Zhejiang University-SCIENCE C (Comput & Electron) , vol.12, no.1, 2011 , pp::76-82.

[10] Weihua Zheng, Kenli Li, Keqin Li, "A Fast Algorithm Based on SRFFT for Length N=qx2m DFTs", IEEE Trans. Circuits and Systems-II:
Express Briefs, vol. 61, no.2, 2014, pp: 110-114.

[11] Weihua Zheng, Kenli Li, and Keqin Li,″ A Fast Algorithm Based on SRFFT for Length $N = q \times 2m$ DFTs , *IEEE Trans. Circuits Syst.II, Exp. Briefs*, vol. 61, no. 2, pp.110-114, Feb. 2014