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Performance Analyzing of CMOS Gates by Sub Clocking Method Using Cadence Tools

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ABSTRACT

Reducing the power consumed by the device is the emerging trend. The aim of this project is to reduce the leakage current of the circuit by using the Sub Clocking technology. It is the process of switching the circuit by means of partially ON to reduce the power consumption. In this paper there are two modes of operation are implemented.1. Half mode operation, 2. Full mode operation. This mode of operation are implemented in the two designing method. Design-1: pMOS and nMOS are connected at the header side of the standard CMOS circuit.Design-2: pMOS and nMOS are connected at the header side of the standard CMOS circuit. pMOS and nMOS transistor at the header and footer side are refer to be as a Sub Clock control unit. Any one of the transistor is ON for a half mode operation and both the transistor are turn ON for full mode of operation. This will do by using the control signal to the unit.
Keywords: CMOS, Sub Clocking Method, Cadence Tools, HOM, SCC, VDD, DML, UMC, GND

I. INTRODUCTION

Leakage power can be as dominant as dynamic power, poses a large source of power consumption in digital circuits during the active mode, i.e., when the digital circuit is doing useful work. A number of techniques have been proposed for reducing active leakage power dissipation. To obtain the effective result with reduced power consumption the Sub Clocking is used.

In this paper a proposed technic is called the Sub Clock Controlling (SCC), which is target at low power applications. Minimizing the leakage power of the circuit is done by using a two different mode of operation. Full Operating Mode (FOP), Half Operating Mode (HOM). These two modes of operation can be implemented in a two different way (i.e.) two design methodology.

Design-1: pMOS and nMOS are connected at the header side of the standard CMOS circuit.

Design-2: pMOS and nMOS are connected at the header side of the standard CMOS circuit.

pMOS and nMOS are used as a Sub Clock Control circuit to drive the entire circuit by means of voltage divider method. In design-1 the control circuit is connected at the header side of the circuit to control the entire circuit by divide the given supply voltage (VDD).

Similarly in the second design methodology the Sub Clock Control circuit is placed at the footer side in order to reduce the leakage current through the circuit to ground terminal.

II. METHODS AND MATERIAL

A. Existing System

1. Sub threshold Dual Mode Logic

In this brief, we introduce novel low-power dual mode logic (DML) family, designed to operate in the subthreshold region. The proposed logic family can be

switched between static and dynamic modes of operation according to system requirements. In static mode, the DML gates feature very low-power dissipation with moderate performance, while in dynamic mode they achieve higher performance, albeit with increased power dissipation. This is achieved with a simple and intuitive design concept. SPICE and Monte Carlo simulations compare performance, power dissipation, and robustness of the proposed DML gates to their CMOS and domino counterparts in the 80-nm process. Measurements of an 80-nm test chip are presented in order to prove the proposed concept.

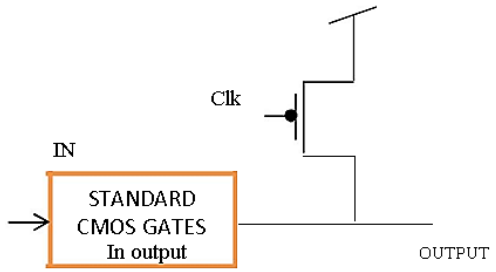

Figure 1: Dynamic mode of operation

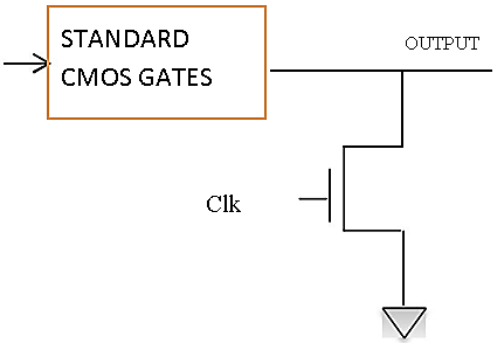

Figure 2: Static mode of operation

2. Dynamic supply and threshold voltage scaling

In this method a direct power monitoring scheme is proposed that does not need any replica and hence can sense total power consumed by load circuit across process, voltage, and temperature corners.

Design details and performance of power monitor and tracking algorithm are examined by a simulation framework developed using UMC 90-nm CMOS triple well process.

This algorithm with direct power monitor achieves a power savings of 42.2% for activity of 0.02 and 22.4% for activity of 0.04. Issues with loop convergence and design tradeoff for power monitor are also discussed.

B. Proposed System

In this paper all the above defects have been rectified and an improved strategy had been implemented by enhancing all the basic compensation techniques in the above stated projects. The following are the protocols developed to reduce the leakage power in cmos circuit during the active mode of operation.

By activating the CMOS transistor there will be a shot circuit between the Vdd and ground will happen at the 0.7 voltage switching. This causes a direct link to ground leakage current will more at this time of switching. In order to reduce the leakage current the sub clocking method is implemented. There are two design method is implemented in order to rectify the problems. Ideal clamping is used in the proposed system.

Design 1

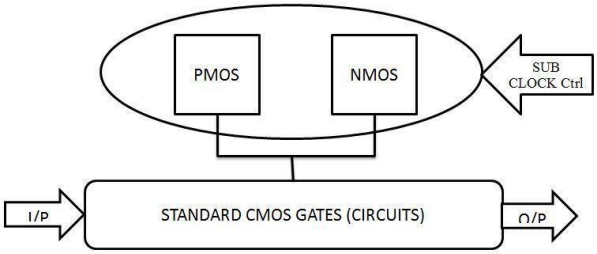

Figure 3: Design-1 block diagram

In this design technic the control circuit is placed at the header side of the CMOS circuit. By this process the operating voltage which is given to the circuit is divided into two parts by using the nMOS and pMOS transistor .These transistor are connected in parallel form as shown in the fig 3.

Thus the input is given directly to the CMOS circuit and the output is drive directly from the circuit. For half mode power output is control by the sub clock control circuit.(i.e..,)Either pMOS is ON or nMOS is switched ON. pMOS is switched ON and OFF using the control signal as 0and 1. Similarly the nMOS is switched ON and OFF by using the control signal as 1 and 0.

For a full power operation to drive the large load the control circuitry is switched ON fully mode i.e.., pMOS and nMOS both are in closed circuit. Thus the total power is given to the CMOS circuit.

Design 2

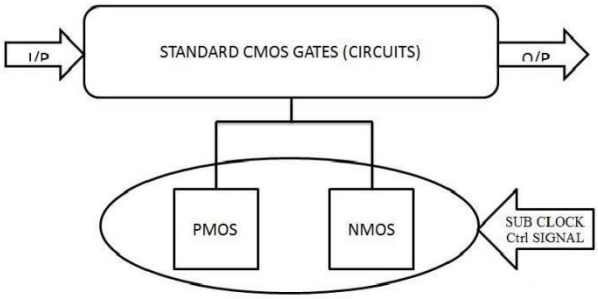

Figure 4 : Design-2 block diagram

In this design technic the control circuit is placed at the footer side of the CMOS circuit. By this process the leakage current due to the short circuit between the VDD and GND is reduced by using the nMOS and pMOS transistor .These transistor are connected in parallel form as shown in the fig 4.

Thus the input is given directly to the CMOS circuit and the output is drive directly from the circuit. For half mode power output is control by the sub clock control circuit.(i.e..,)Either pMOS is ON or nMOS is switched ON. pMOS is switched ON and OFF using the control signal as 0and 1. Similarly the nMOS is switched ON and OFF by using the control signal as 1 and 0.

For a full power operation to drive the large load the control circuitry is switched ON fully mode i.e.., pMOS and nMOS both are in closed circuit. Thus the total power is given to the CMOS circuit.

Symmetrical Virtual Rail Controlling

In this method both the design:1 and design:2 are implemented in the single circuit. By this the power consumption of the circuit is also reduced and also the leakage current is also reduced to 20%.

C. Implementation of the Design.

NOT gate:

Design: 1 is implemented in the NOT gate transistor level model.

This circuit diagram explains how the design is implemented in the standard CMOS gate. By using the control signal to pMOS and nMOS the operation is verified. The output is drive directly from the transistors

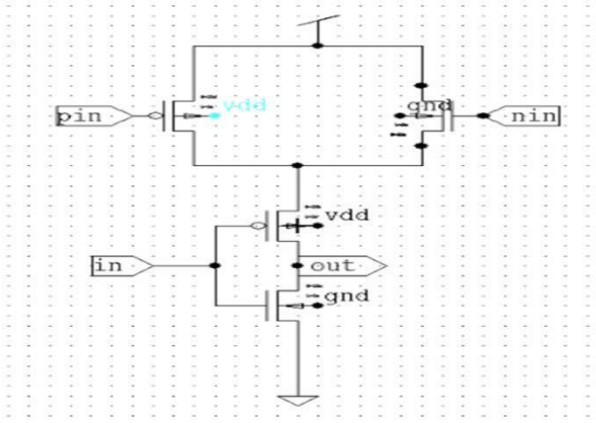

Figure 5 : NOT gate with design:1

NAND gate:

Design : 1 is implemented in the NAND gate transistor level model.

In this circuit the NAND gate is controlled by the sub clock control circuit at the header side of the circuit. The supply voltage given to the circuit is control by the control signal given to the CMOS gate.

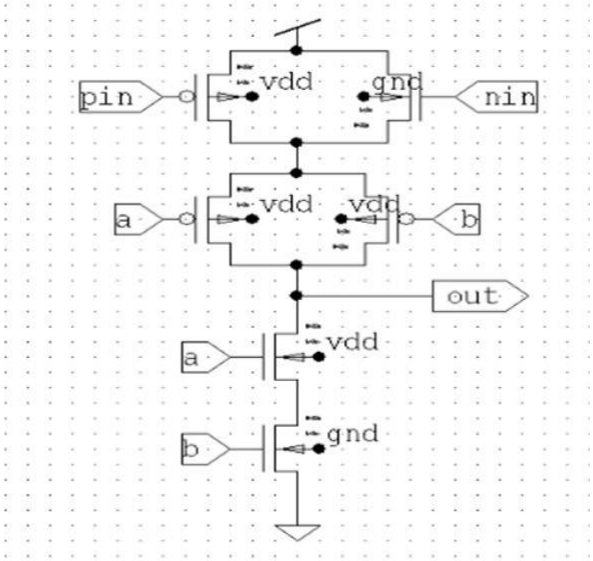

Figure 6 : NOT gate with design:1

Similarly these design is implemented various circuits and the power is calculated using the spice model in the tanner v13 simulation tool.

III. RESULTS AND DISCUSSION

Power outputs
Comparison table

S.NO	CMOS circuit	Half power mode operation	Full power mode operation
1	NOT gate	4.54*10^-08	1.73*10^-08
2	NAND gate	2.04*10^-08	3.01*10^-07
3	AND gate	7.66*10^-08	1.58*10^-07
4	OR gate	9.25*10^-08	6.31*10^-07
5	XOR gate	8.38*10^-08	8.99*10^-07

Future Work

Possible future improvements are better packaging of the circuitry with lower power consumption for main units. By reducing the nm technology the power consumption can further reduced to lower level. This technique is implement at different level using tanner or cadence tool and implement and simulation output.

IV. CONCLUSION

This paper has proposed a power gating technique that reduces leakage power during the active mode for low performance energy-constrained applications by power gating combinational logic within the clock period. Rather than shutting down completely, symmetric virtual rail clamping was proposed to reduce wake-up power mode transition energy cost.

The work proposed in this paper can be considered as an orthogonal approach to the recently proposed sub threshold technique for maximizing energy efficiency when operating at low performance. The sub threshold technique enables realization of minimum energy computation by scaling the supply voltage below Vth until a minimum energy point is found where dynamic energy equals leakage energy per operation.

Due to the aggressively scaled supply voltage, the technique comes at a cost of performance making it suitable for low performance, energy-constrained applications.

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