© 2016 IJSRSET | Volume 2 | Issue 3 | Print ISSN : 2395-1990 | Online ISSN : 2394-4099
Themed Section: Engineering and Technology

Design of a Half/Full Subtractor on Quantum-Dot Cellular Automata

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ABSTRACT

Quantum-dot cellular automata (QCA) is a novel nanotechnology which promises molecular digital circuits with ultra-high clock frequencies, alternative solution to replace to replace the conventional CMOS technology which is reaching their physical limits. Despite a lot is still needed for the large scale utilization of the technology, there has been serious effort in digital design implementation in QCA. In this paper, a new architecture of Half and Full subtractor based on the QCA is proposed. The benefit of optimal FNZ universal gate is taken in demonstrating these arithmetic units, which has already designed based on the QCA. The design helps to reduce the complexity, then the conventional subtractors based on the QCA, in terms of covered area, count of the cells, and delay. The proposed subtractors are designed and simulated using QCA Designer tool version 2.0.3.

Keywords: Quantum dot cellular automata, Half subtractor, Full subtractor, FNZ universal gate

I. INTRODUCTION

Gordon Moore in his famous theory, named as Moore's law, pointed out that every eighteen months, the number of elements built on a concrete surface doubles [1]. However, evidences of the fact that CMOS technology is reaching to its physical limitations has resulted in the conduct of various research all around the world in order to look out for the technology/technologies which could replace CMOS in order to continue following the Moore's law [2]. Quantum-dot Cellular Automata is coming out as one of such promising technologies for future generation ICs and will overcome limitations of CMOS technology [3] [4]. The concept of QCA was introduced in early 1990s, by Lent & Tougaw [5,6], and has been demonstrated in laboratory environment with small proof-of-concept systems [7-9]. It is believed that 1012devices/cm2 density can be achieved in case of the QCA architectures. Besides the advantage of the high density they provide designs are able to operate efficiently in 100GH domain whereas maintaining switching speeds as low as 10ps. Moreover, they could achieve high power of around 100W/cm2 [10-12].

The computation in case of QCA is totally different form the conventional digital circuits where the logic states are not stored in voltage levels. Here, the states are represented by a cell which is the smallest part in QCA Circuits. A cell is a nano-scale device capable of encoding data by two-electron configurations. The interaction between the neighbouring cells, when a set of systematic cells are located next to each other, leads to a locally interconnected architecture [4, 13]. This interaction supports information transfer between cells via columbic interaction between the electrons of each cell and the neighbouring cells. It is possible to implement all combinational and sequential logic functions by properly arranging cells so that the polarization of one cell sets the polarization of a nearby cell [6]. However, for the correct functionality the cells must be aligned precisely at nanoscales.

In this paper, we design and simulate half and full Subtractor which can further be extended to more bits

for its use in a variety of ALUs in the QCA framework. As the simulation results, we analyse the efficiency and performance between the proposed and previous techniques by QCA Designer. The paper is organized as follows. Introduction on the basic concepts of the QCA is laid in section 2. A brief introduction on the FNZ universal Gate is given in section 3. Section 4 introduces the proposed subtractor design and the simulation results along with comparison results are given in section 5. Finally, section 6 gives the conclusions of the paper.

II. METHODS AND MATERIAL

A. QCA Basic Concept

QCA cell forms the basic unit of QCA circuit. As can be seen from Figure 1 it consists of four quantum dots arranged in the corners of a square structure. It is expressed by an arbitrary state such as null or ground. Injected into the cell are two free electrons. These electrons are moving freely between quantum dots for the null state as shown in Figure 2. But, when a cell is in ground state electrons are fixed as an arbitrary position and tend to attain maximal separation by occupying dots in opposite corners, because of the columbic repulsive force between them. Considering the location of mobile electrons in the cell, two steady states, called cell polarizations, are possible. These two distinct polarizations, are used to represent logic "1" corresponding to p=+1 and logic "0" corresponding to p=-1. The polarizations and logic values are illustrated in Figure 3.

The combination of these cells results in different designs. One of the basic implementation is that of a wire and depending on the orientation of the cells there are two types of wires Binary wire and Inversion chain. In the first type regular cells are placed in a linear array as shown in Figure 4(a) while as the second case is obtained by arranging the rotated cells with 45° orientations as shown in Figure 4(b).

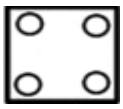


Figure 1 : QCA Cell

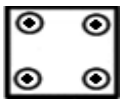
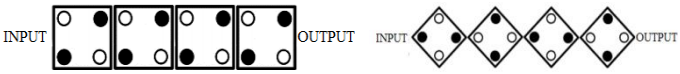


Figure 2 : QCA Cell at Null State

(a) P = -1 (0 binary) (b) P = +1 (1 binary)

Figure 3: QCA Cell at Ground State



(a) Binary wire (b) Inversion chain

Figure 4: QCA Wire

Another essential element is QCA clocking. Clocking playes an important role in the QCA circuits by providing the synchronization in the circuits. Switch, Hold, Release and Relax are the four phases of the clock which are required by a QCA cell. During Switch phase, the inter-dot barriers in a zone are raised, while this occurs, electrons within cell can be influenced by the Columbic charges of neighbouring zones. In the Hold phase the inter-dot barriers are kept up, so that electrons do not switch between dots. Inter-dot barriers are reduced in the Release phase and cells lose their polarity. Inter-dot barrier is held down and a cell has no influence on its neighbours, in the Relax phase. Figure 5 represents a cell in its four clock phases.

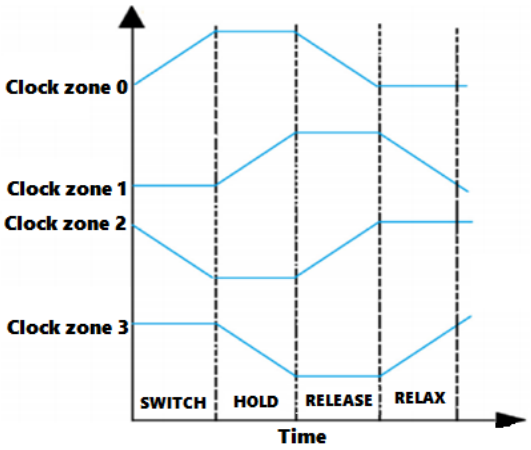


Figure 5 : QCA clocking

B. FNZ Gate

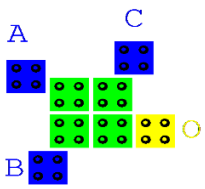
Most of the Digital circuits in QCA are designed with logic gates like AOI (And-Or-Inverter) gate, NNI (NAND-NOR-INVERTER), Majority Voter (provides the Majority of the input polarization at the output) and Inverter (provides the polarization at the output cell reverse of that of the input polarization). Recently, one

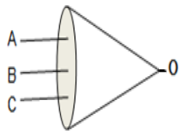
such universal gate for QCA was presented in [14], named as FNZ gate. The paper besides introducing the universal gate for QCA also claimed that the gate is highly effective regarding space and speed consideration. It provides a significant reduction in hardware cost and switching delay with respect to the other existing techniques. While realizing the basic logic gates, FNZ proves to be more effective than AOI (And-Or-Inverter) gate and NNI (NAND-NOR-INVERTER) as it offers more flexibility in terms cell setting. The QCA representation, symbol and the truth table of FNZ gate is given in Table I. The design comprises of 8 cells with three inputs and an output. One of the input is vertically translated to 10nm while as the other two inputs are horizontally translated to 10nm making the whole design to occupy 6084nm^2 (0.01μm^2). The simulation result of the gate is shown in Figure 6 and the logical expression for FNZ gate is given in (1) as

$$F = A'B' + (A \oplus B)C \tag{1}$$

TABLE I

FNZ GATE DESIGN, SYMBOL & TRUTH TABLE





A	B	C	O
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

QCA Representation	Symbol	Truth Table

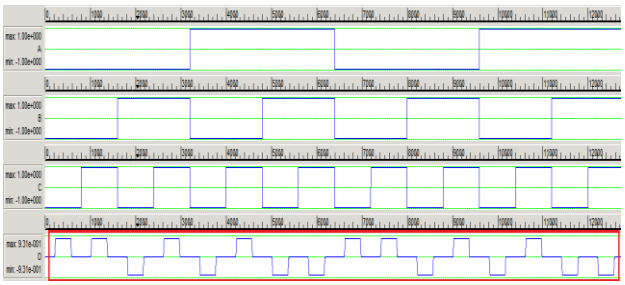


Figure 6: Simulation Result of FNZ Gate

In the next section the design of subtractor circuit using FNZ gate in QCA is introduced. The proposed subtractor design performance in terms of area, clock phase etc is also made to establish that the proposed design is better than the previously reported designs.

III. RESULTS AND DISCUSSION

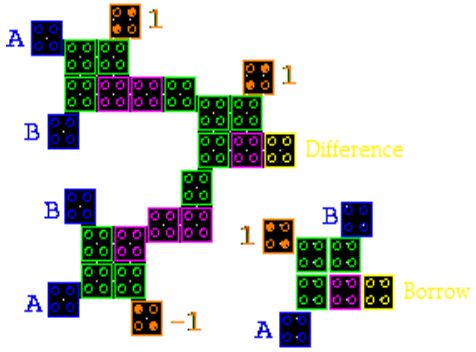
Proposed Subtractor Design

Subtractor is one of the essential arithmetic units which falls into the category of combinational circuit. Subtractor can either be half subtractor or a full subtractor depending on the number of input bits. A half subtractor, subtracts two bits applied at its input and produces two outputs of Difference (subtraction results of inputs) and Borrow (specifies if '1' has been borrowed). While as a Full subtractor is a circuit, which subtracts two bits with considering the result of lower significant stage. The truth table for a half and full subtractor are given in table 2 and table 3 respectively. Boolean expressions for Difference and Borrow in case of half subtractor is given in (2) and for full subtractor given in (3)

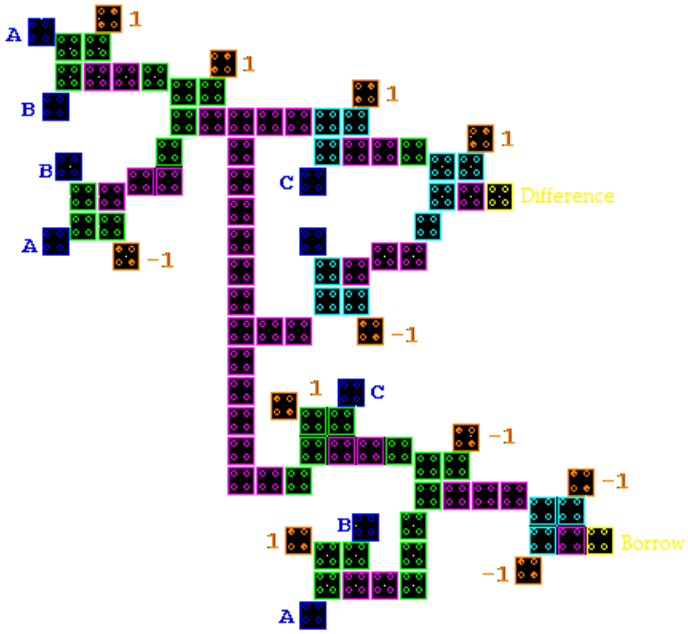
$$\begin{aligned} Difference &= A \oplus B \\ Borrow &= A'B \end{aligned} \tag{2}$$

$$\begin{aligned} Difference &= A \oplus B \oplus C \\ Borrow &= A'B + (A \oplus B)' C \end{aligned} \tag{3}$$

The QCA implementation of the half and the full subtractor unit is shown in Figure 7(a) and 7(b). while as, the Simulation result for the designed full subtractor is shown in Figure 8. The comparison between the proposed design to that of the previously reported ones is drawn in Table 4. It is obvious from the comparison table that the proposed designs are more efficient in terms of cell counts, covered area and delay.



(a)



(b)

Figure 7: Layout for the proposed subtractor based on QCA cells (a) Half subtractor, (b) Full subtractor

Subtractor Designs	Half Subtractor				Full Subtractor		
Model	Iakshmi, et al. [15]	Rubina, et al. [16]	Dallaki and Mehran [17]	Proposed	Iakshmi, et al. [15]	Dallaki and Mehran [17]	Proposed
Area (μm^2)	0.089	0.084	0.0504	0.066	0.205	0.168	0.13
Cell Count	77	70	55	33	178	136	94
Delay	3 clock phase	4 clock phase	3 clock phase	2 clock phase	8 clock phase	7 clock phase	3 clock phase

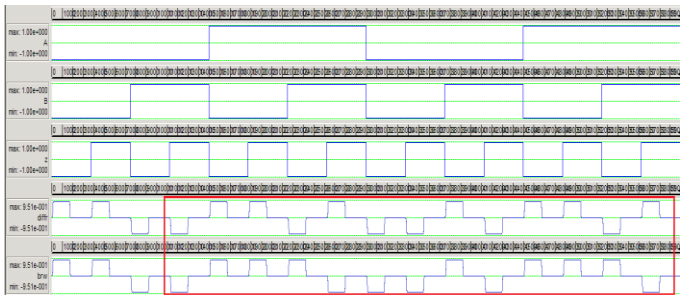


Figure 8: Simulation Result of QCA Full Subtractor

IV. CONCLUSION

In this paper, a novel design of Half and Full subtractors based on QCA using universal FNZ gate has been proposed. Using FNZ gates for designing these circuits, tends to a considerable reduction in the used QCA cell numbers in comparison with the latest counterparts. Smaller cell numbers and subsequently smaller occupied area, lower delay and less power consumption are the major specifications of the designed subtractor circuits and these specifications are of the great concerns in the arithmetic units.

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