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32-bit Signed and Unsigned Advanced Modified Booth Multiplication using Radix-4 Encoding Algorithm

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ABSTRACT

This paper presents the design and implementation of Modified Booth encoding multiplier for both signed and unsigned 32 - bit numbers multiplication. The already existed Modified Booth Encoding multiplier and the Baugh-Wooley multiplier perform multiplication operation on signed numbers only. Whereas the array multiplier and Braun array multipliers perform multiplication operation on unsigned numbers only. Thus, the requirement of the modern computer system is a dedicated and very high speed unique multiplier unit for signed and unsigned numbers. Therefore, this paper presents the design and implementation of Booth multiplier. The modified Booth Encoder circuit generates half the partial products in parallel. By extending sign bit of the operands and generating an additional partial product the SUMBE multiplier is obtained. The Carry Save Adder (CSA) tree and the final Carry Look ahead (CLA) adder used to speed up the multiplier operation. Since signed and unsigned multiplication operation is performed by the same multiplier unit the required hardware and the chip area reduces and this in turn reduces power dissipation and cost of a system.

Keywords: Modified Booth Encoding multiplier, Radix-4 algorithm, CSA, CLA Partial product, Signed-unsigned.

I. INTRODUCTION

Multipliers are essential components widely used in multimedia and Digital Signal Processing chips. These are used to give raise to the power and performance of the Chip. Parallel multipliers are predominantly used to increase the speed and reduce the cost of high area complexity. Many multiplication architectures are used to increase the speed and performance of the chips used in multimedia and digital signal processing. In these architectures predominantly modified booth algorithms have implemented significant multiplication in DSP and other multimedia applications. The important and significant Multipliers used in DSP and other multimedia applications are modified booth multipliers with the combination of low error fixed-width, fixed-width, high-accuracy error compensation circuit and low-error reduced-width architectures. All these combinations of architectures with Booth Encoder Multiplier have reduced remarkably the cost of systems and enhanced the speed of the multiplication operations.

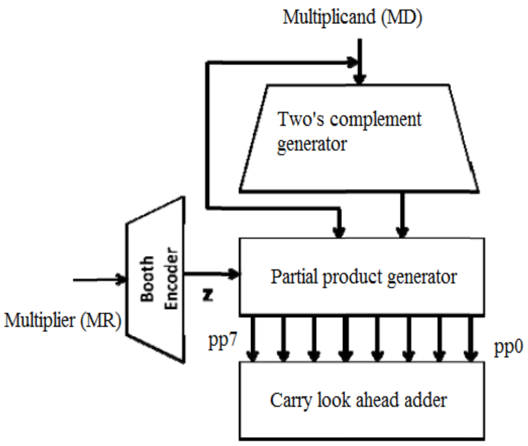


Figure 1. Architecture of Booth Multiplier

The Architecture of Booth Multiplier has shown in Figure 1. The high speed Booth multipliers and pipelined Booth multipliers are used for digital signal processing (DSP) applications such as for multimedia and communication systems. High speed DSP computation applications such as Fast Fourier transform (FFT) require additions and multiplications. The conventional modified Booth encoding (MBE) generates an irregular partial product array because of the extra partial product bit at the least significant bit position of each partial product row.

II. METHODS AND MATERIAL

Implementation

A. Proposed System

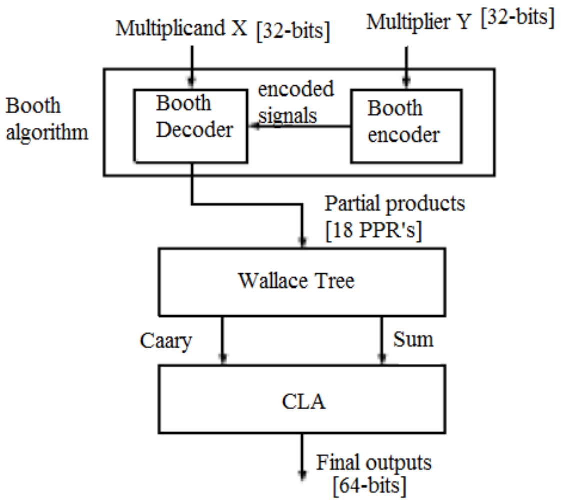


Figure 2. Architecture of the 32-bit Booth Encoder Multiplier

The proposed Booth Encoder Multiplier using Carry Select Adder is designed and developed with improved architecture and more powerful algorithms. In this architecture X is used as multiplicand and Y is used as Multiplier. The Booth Encoder which is going to be implemented encodes the input Y and extracts the encoded signals. The detailed architecture is shown in Figure 2.

B. Sign Converter

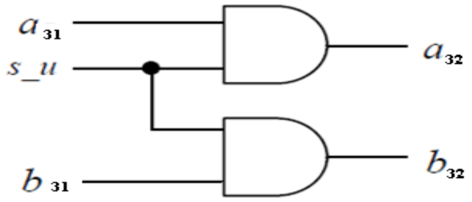


Figure 3. Sign Converter

The Logic diagram of Sign converter has shown in Figure 3. The working principle of sign extension that converts signed multiplier signed-unsigned multiplier as follows. One bit control signal called signed-unsigned (MSB) bit is used to indicate whether the multiplication operation is signed number or unsigned number. When MSB = 0, it indicates unsigned number multiplication, and when MSB = 1, it indicates signed number multiplication. It is required that when the operation is unsigned multiplication the sign extended bit of both multiplicand and multiplier should be extended with 0, that is a32= a33= b32= b33= 0. It is required that when the operation is signed multiplication the sign extended bit depends on whether the multiplicand is negative or the multiplier is negative or both the operands are negative. For this when the multiplicand operand is negative and multiplier operand is positive the sign extended bits should be generated are MSB = 1, a31=1, b31= 0, a32= a33 =1, and b32= b33=0.

B. Radix-4 Booth Encoder

Booth algorithm is a powerful algorithm for signed number multiplication, which treats both positive and negative numbers uniformly. Since a k-bit binary number can be interpreted as k/2-digit Radix-4 number, a k/3-digit Radix-8number and so on, it can deal with more than one bit of the multiplier in each cycle by using high radix multiplication. The major disadvantage of the Radix-2 algorithm was that the process required n shifts and an average of n/2 additions for an n bit multiplier. This variable number of shift and add operations is inconvenient for designing parallel multipliers .Also the Radix-2 algorithm becomes inefficient when there are isolated 1's.

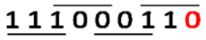


Figure 4. Grouping of 3 bits in Radix-4 method

The Radix-4 modified Booth algorithm overcomes all these limitations of Radix-2 algorithm. For operands equal to or greater than 16 bits, the modified Radix-4Booth algorithm has been widely used. It is based on encoding the two's complement multiplier in order to reduce the number of partial products to be added to n/2. Table I shows the encoding of the signed multiplier Y, using the Radix-4 Booth algorithm. Here we consider the multiplier bits in blocks of three, such that each block overlaps the previous block by one bit. It is advantageous to begin the examination of the multiplier with the least significant bit.

Multiplier Bits Block			Recoded 1-bit pair		2 bit booth	
i+1	i	i-1	i+1	i	Multiplier Value	Partial Product
0	0	0	0	0	0	Mx0
0	0	1	0	1	1	Mx1
0	1	0	1	-1	1	Mx1
0	1	0	1	0	2	Mx2
1	0	0	-1	0	-2	Mx-2
1	0	1	-1	1	-1	Mx-1
1	1	0	0	-1	-1	Mx-1
1	1	0	0	0	0	Mx0

Table 1: Booth recoding table for radix-4.

C. Partial Product Reduction

Traditionally, half and full adders, organized in a carry save adder format, have been used in the partial product reduction process. However, since their inception by Weinberger, [4:2] adders have become a topic of significant research in the arithmetic community. It has transformed the standard frame of mind of counter for partial product reduction by introducing the notion of horizontal data paths within stages of reduction. Furthermore, optimized [5:2], [6:2], [7:2] adders are proposed to improve the architecture of partial product reduction process. The MBE algorithm typically generates n/2+1 PPRs instead of n/2 due to the extra partial product bit (Neg bit) . One more PPR is needed for signed/unsigned configurations in our multiplier. Instead of using to reduce the number of PPRs, all the MSBs of PPR for sign-protection scheme are grouped with the Neg bit to form one more PPR, As a result, there are 18 PPRs in the 32-bit multiplier presented in this paper. The 18 PPRs are reduced to two rows, as shown in Fig 5.

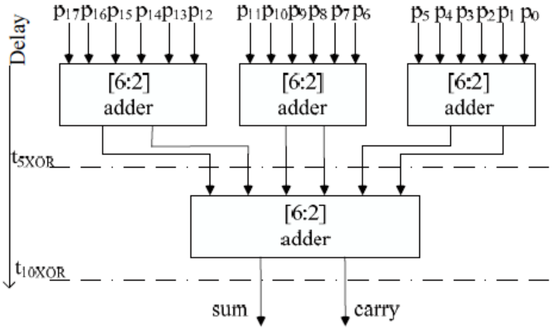


Figure 5. Tree-base compression scheme

D. Partial product addition

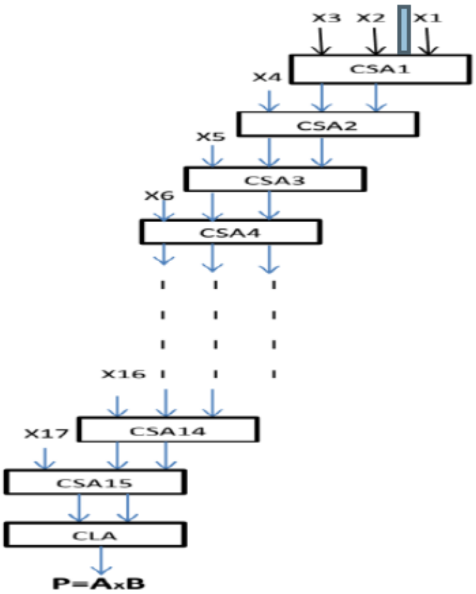


Figure 6. Partial product adder logic

These partial products are added by the Carry Save Adders (CSA) and the final stage is Carry Look ahead (CLA) adder as shown in Fig 6. Each CSA adder takes three inputs and produce sum and carry in parallel. There are three CSAs, five partial products are added by the CSA tree and finally when there are only two outputs left out then finally CLA adder is used to produce the final result. Assuming each gate delay an unit delay, including partial product generator circuit delay, then the total through the CSA and CLA is 15+16 = 31 Unit delay. Thus with present Very Large Scale Integration (VLSI) the total delay is estimated around 0.7 nanosecond and the multiplier operates at Giga hertz frequency.

III. RESULTS AND DISCUSSION

1. **Simulation Results**

A. RTL Schematic of 32-bit Booth multiplier

The modified AMBE with the mechanisms have been included for the Xilinx ISE14.5 and simulated with the ISIM for this 32-bit Multiplication logic.

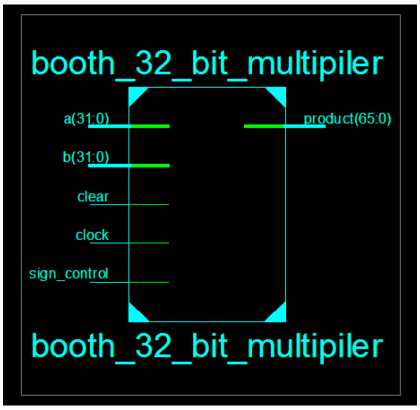
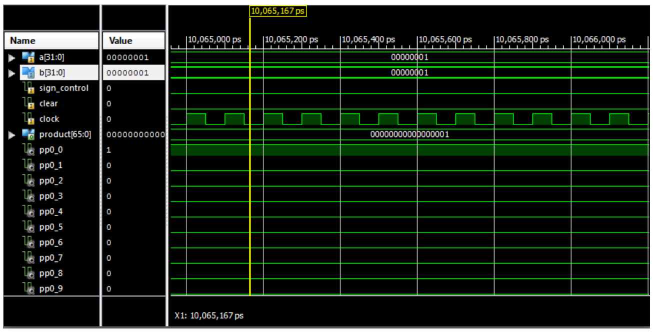


Figure 7. RTL Schematic of 32-bit Booth multiplier.

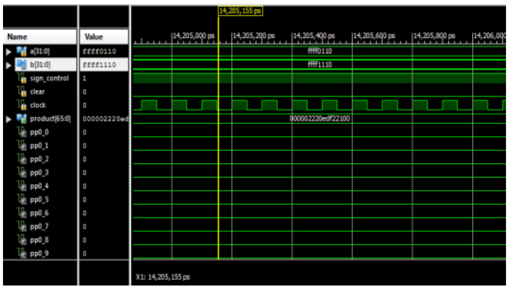
B. Simulation result for 32-bit unsigned number multiplication



Name	Value
a[31:0]	00000001
b[31:0]	00000001
sign_control	0
clear	0
clock	0
product[65:0]	00000000000
pp0_0	1
pp0_1	0
pp0_2	0
pp0_3	0
pp0_4	0
pp0_5	0
pp0_6	0
pp0_7	0
pp0_8	0
pp0_9	0

Figure 8. 32-bit unsigned number multiplication in Hexadecimal representation.

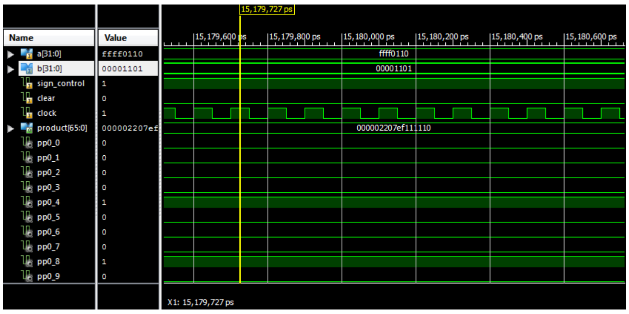
C. Simulation Result 32-bit Signed Number Multiplication



Name	Value
a[31:0]	ffff0110
b[31:0]	ffff1110
sign_control	1
clear	0
clock	0
product[65:0]	000002220ed
pp0_0	0
pp0_1	0
pp0_2	0
pp0_3	0
pp0_4	0
pp0_5	0
pp0_6	0
pp0_7	0
pp0_8	0
pp0_9	0

Figure 9. 32-bit signed number multiplication in Hexadecimal representation

D. Simulation result for 32-bit signed by unsigned numbers multiplication



Name	Value
a[31:0]	ffff0110
b[31:0]	00001101
sign_control	1
clear	0
clock	1
product[65:0]	000002207ef
pp0_0	0
pp0_1	0
pp0_2	0
pp0_3	0
pp0_4	1
pp0_5	0
pp0_6	0
pp0_7	0
pp0_8	1
pp0_9	0

Figure 10. 32-bit signed by unsigned numbers multiplication in Hexadecimal representation

IV. CONCLUSION

The paper proposes the new CLA tree structure for the AMBE which provides the less power efficient and less area computations. The designed AMBE can be used for the high speed networks solutions. In this paper, I present a 32-bit×32-bit advanced multiplier capable of carrying out both signed and unsigned operations. The proposed novel unified signed/unsigned multiplier was optimized in terms of speed, power consumption and silicon area by exploiting more regular partial product array, developing more efficient compression methods and combining several types of fast adders.

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