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Single Electron Transistor Made Nano IC Adder for High Speed Computing

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ABSTRACT

Single electron transistor (SET) is a key element of present device research which can offer high operating speed with low power consumption. Downscaling of minimum feature size of CMOS transistor has been the basis for advancement in ultra large integration for many years. But by no means it has turned to be a never ending process. The present work demonstrates a hypothetical approach to design a single electron device based commercially viable logic circuit to be embedded in next generation IC's.

Keywords: SET, SED, Adder, ,Coulomb Island,Nano IC

I. INTRODUCTION

Single electron transistor (SET) technology has been a promising technology since last decade. SET has been the most fundamental of Single Electron Device (SED) family comprising three terminals with very high operating speed and low power consumption. The schematic structure of single electron transistor (SET) may be considered as a field effect transistor (FET) whose channel consist of a small, low capacitance (C), conducting Island [Quantum Dot] which is coupled to the source and drain leads by two tunnel junctions and capacitively coupled to one or more gate which is used to control the transfer of single electron from source to drain [2,3]. Here, the tunnel junction is nothing but a thin insulating barrier between two conducting electrodes. The SET is operated in a single electronics regime in which only one electron can transfer from source to drain via island under the application of constant gate voltage on the island. The low power operational characteristic of SET controls the instability and reliability problem. Besides low power consuming operations; comparison between SET and CMOS revealed that (1) the integration density remains much higher than the present VLSI/ULSI chips; (2) the propagation delay is of 4ns, which is 1/3rd of the propagation delay of the conventional gates that take 12ns for the same device operation (3) the execution time required is nearly one third of the conventional logic based circuits and (4) the speed efficiency improves to 300% in respect to CMOS transistors. SET is extensively used in defense applications, space technologies and biotechnology where basic research work is concentrated on minimum power for maximum battery lifetime.

II. METHODS AND MATERIAL

1. THE THEORY OF SET TECHNOLOGY

The SET structure [4] comprises of two tunnel junctions positioned in series known as a Coulomb-island. Electrons enter by tunneling through one of these insulators. It resembles that of a FET having having three terminals; i.e., the outside terminal of each tunnel junction labeled as "source" and "drain"; and the "gate" terminal that are capacitively coupled to the node between the two tunnel junctions. The Tunneling of an electron occurs from point to point of a tunnel junction to the opposite end point of the tunnel junction; thereby the charge distribution of that particular circuit varies. The controlling strategy is that we require Coulomb Energy EC to charge an island with an electron where

EC=e2/(2C)>KBT; only if C is the overall capacitance of an island and KB is Boltzmann's constant (KB=1.38×10-34 J/K). In case this Coulomb Energy is greater than the available thermal energy, the movement of electrons can be controlled by controlling the available energy supplied by voltage source.

2. SET BASED ADDER IC

The attempt to design SET based IC is shown in fig2. The concept is thoroughly verified using Monte Carlo based simulation platform. Study revealed that SET based Adder possess larger efficiency compared to CMOS based circuits[17]. The power dissipation as originated for switching a single bit is of few μW which is noticeably minute when compared to conventional devices. It comprises higher prospect of providing much more component density thereby reducing the future IC sizes [18].Fig.1 shows the SET based logic circuitry of a adder circuit with two binary inputs and two binary outputs .It is an arithmetic circuit used to perform arithmetic operations of addition of two single bit words.

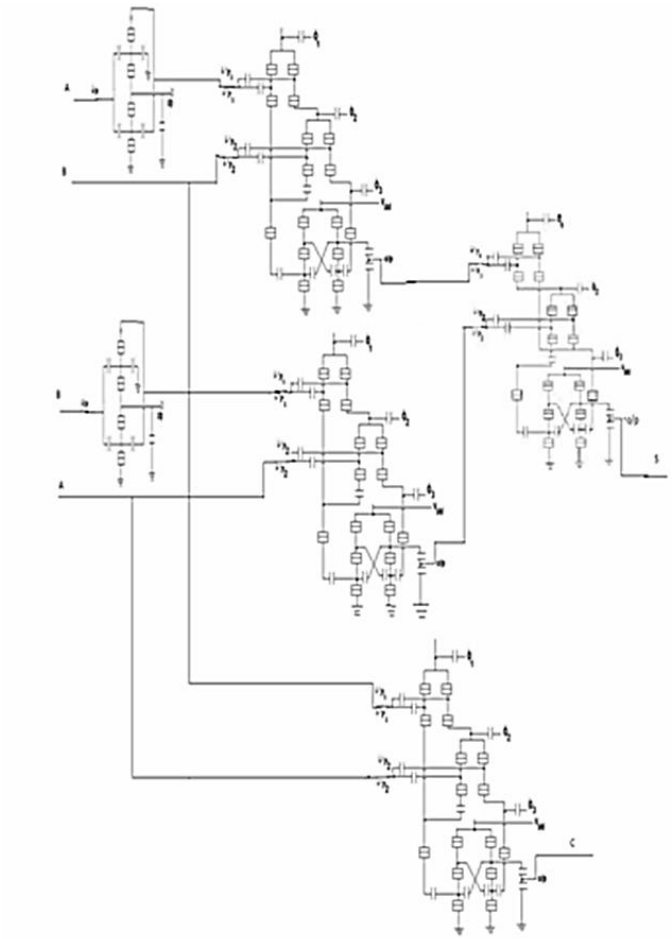

Figure 1. Set Based Adder Circuit

III. CONCLUSION

The proposed model exhibits less propagation delay which is nearly half that of CMOS design. Moreover it also revealed that the power consumption has also reduced to a great extent which is 10 to 12 times lower than conventional CMOS architectures. Further the logical model creates wide applications for future SET based logic circuits.

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