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MATLAB Implementation of a Various Topologies of Multilevel Inverter with Improved THD

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ABSTRACT

Multilevel power converters provide more than two levels of voltage to achieve smoother and less distorted ac to-dc, dc-to-ac, and dc-to-dc power conversion. This paper presents a generalized multilevel inverter (converter) topology with self voltage balancing. The generalized multilevel inverter topology provides a true multilevel structure that can balance each DC voltage level automatically without any assistance from other circuits, thus in principle providing a complete and true multilevel topology that embraces the existing multilevel inverters. From this generalized multilevel inverter topology, several new multilevel inverter structures can be derived. In addition, the generalized topology has led to some new multilevel structures such as P3D and P3C. In some applications such as capacitor-switched power conversion, voltage multiplier, and bi-directional dc/dc conversion, the generalized multilevel converter topology has a niche for implementing magnetic-less, compact, high-efficiency, zero-EMI, and low cost power conversion.

Keywords: Iris Recognition, Visual Cryptography, Segmentation, Localisation, Visual Cryptography, Log Gaber Wavelet

I. INTRODUCTION

An inverter is a device that converts DC power into AC power at desired output voltage and frequency. There are various begins with types of inverters which have the demerits such as less efficiency, high cost and high switching losses. To overcome the demerits of other types of inverters the multilevel inverter concept was introduced in the year 1975.

The term multilevel: The main features of multilevel inverter are to desire the AC voltage waveform from the several of DC voltage. The main merits of the multilevel inverter are high efficiency, low cost, low switching losses and good power quality. The output of multilevel inverter looks like a staircase and sinusoidal waveform. There are different types of inverters available these days. Few most commonly used inverter types are:

- Square wave inverters
- Modified sine wave inverters
- Multilevel inverters
- Pure sine wave inverters
- Resonant inverters
- Grid tie inverters
- Synchronous inverters
- Stand-alone inverters
- Solar inverter

II. METHODS AND MATERIAL

A two-level Inverter creates two different voltages for the load i.e. suppose we are providing V_{dc} as an input to a two level inverter then it will provide + $V_{dc}/2$ and – $V_{dc}/2$ on output. In order to build an AC voltage, these two newly generated voltages are usually switched. For switching mostly pulse width modulation is used. Although this method of creating AC is effective but it has few drawbacks as it creates harmonic distortions in the output voltage and also has a high dv/dt as compared to that of a multilevel inverter. Normally this method works but in few applications it creates problems particularly those where low distortion in the output voltage is required. The output waveform of normal two level inverter is as shown in the following figure.

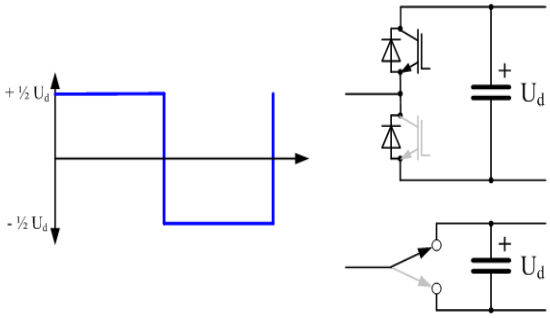

Figure 1. Two level inverter

The concept of multilevel Inverter (MLI) is kind of modification of two-level inverter. In multilevel inverters we don't deal with the two level voltage instead in order to create a smoother stepped output waveform, more than two voltage levels are combined together and the output waveform obtained in this case has lower dv/dt and also lower harmonic distortions. Smoothness of the waveform is proportional to the voltage levels, as we increase the voltage level the waveform becomes smoother but the complexity of controller circuit and components also increases along with the increased levels. The output waveform of multilevel inverter is as shown in the following figure.

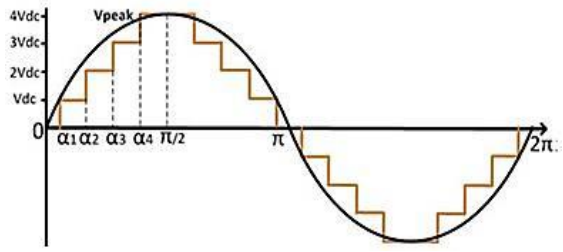

Figure 2. Multilevel inverter waveform

Multilevel converters (or inverters) have been used for power conversion in high-power applications such as utility and large motor drive applications. Multilevel inverters provide more than two voltage levels. A desired output voltage waveform can be synthesized from the multiple voltage levels with less distortion, less switching frequency and higher efficiency. The inherent high quality of the multistep waveform allows operation without PWM, thus high switching losses are avoided. It also discusses the issues affecting the application of multilevel inverter structures as reactive power compensators and compares the device MVA and reactive component MVA requirements of two topologies that have been presented in prior literature. The modulation strategy strongly affects the voltage balancing in the DC bus capacitors as well as their ripple current rating and capacitance value.

1. Multi Level Inverter Topologies

There are several topologies of multilevel inverters available. The difference lies in the mechanism of switching and the source of input voltage to the multilevel inverters. Three most commonly used multilevel inverter topologies are:

Cascaded H-bridge multilevel inverters

Diode Clamped multilevel inverters

Flying Capacitor multilevel inverters

Cascaded H-Bridge Multilevel Inverter

This inverter uses several H-bridge inverters connected in series to provide a sinusoidal output voltage. Each cell contains one H-bridge and the output voltage generated by this multilevel inverter is actually the sum of all the voltages generated by each cell i.e. if there are k cells in a H-bridge multilevel inverter then number of output voltage levels will be 2k+1. This type of inverter has advantage over the other two as it requires less number of components as compared to the other two types of inverters and so its overall weight and price is also less. Figure 2.1a shows a k level cascaded H-bridge inverter.

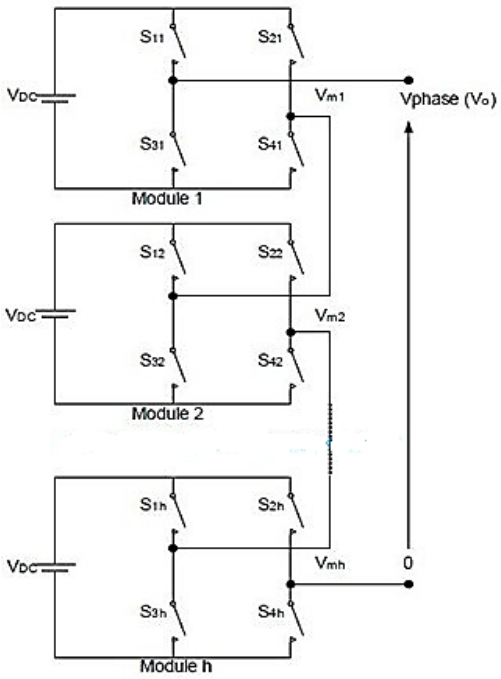

Figure 3. One phase of a cascaded H-bridge multilevel inverter

In single phase inverter, each phase is connected to single dc source. Each level generates three voltages which are positive, negative and zero. This can be obtained by connecting the AC source with the DC output and then using different combinations of the four switches. The inverter will remain ON when two switches with the opposite positions will remain ON. It will turn OFF when all the inverters switch ON or OFF. To minimize the total harmonic distortion, switching angles are defined and implemented. The calculations for the measurement of switching angle will remain the same. This inventor can be categorized further into the following types:

- 5 levels cascaded H Bridge Multilevel Inverter
- 9 levels cascaded H Bridge Multilevel Inverter

In 5 level cascaded H Bridge Multilevel Inverters, Tw
H Bridge Inverters are cascaded. It has 5 levels of outp
and uses 8 switching devices to control whereas in
level cascaded H Bridge Multilevel Inverters, Four
Bridge Invertors are cascaded. It has 9 output levels ar
use and use 16 switching devices.

Applications of Cascaded H-bridge Multilevel Inverters

Cascaded H Bridge Multilevel Inverters are mostly used for static var applications i.e., in renewable resources' of energy and battery based applications. Cascaded H Bridge Multilevel Inverters can be applied as a delta or wye form. This can be understood by looking at the work done by Peng where he used an electrical system parallel with a Cascade H Bridge. Here inverter is being controlled by regulating the power factor. Best application is when we used as photovoltaic cell or fuel cell. This is the example of Parallel connectivity of the H Bridge Multilevel Inverter.

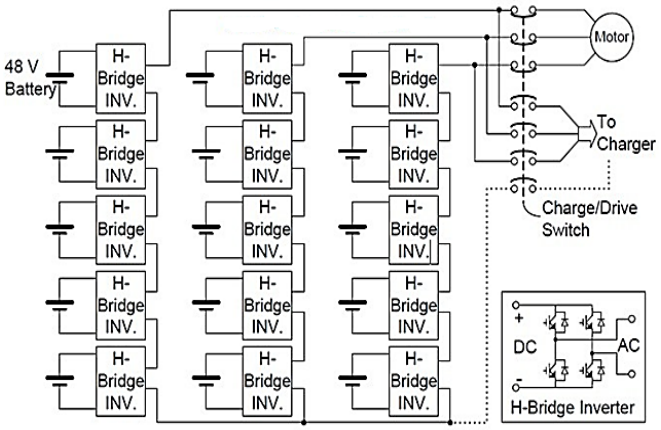

Figure 4. Example of 3 phase Wye Connection

H Bridge can also be used in car batteries to run the electrical components of the car. Also this can be used in electrical braking system of the vehicles. Scientist and engineers have also proposed the multiplicative factor on Cascade H Bridge Multilevel. It means that rather than using a dc voltage with difference in levels, it uses a multiplying factor between different levels of the multilevel i.e., every level is a multiplying factor of the previous one.

Advantages of Cascade H Bridge Multilevel Inverters

1. Output voltages levels are doubled the number of sources Manufacturing can be done easily and quickly
2. Packaging and Layout is modularized.
3.
4. Easily controllable with a transformer as shown in the Fig 4.

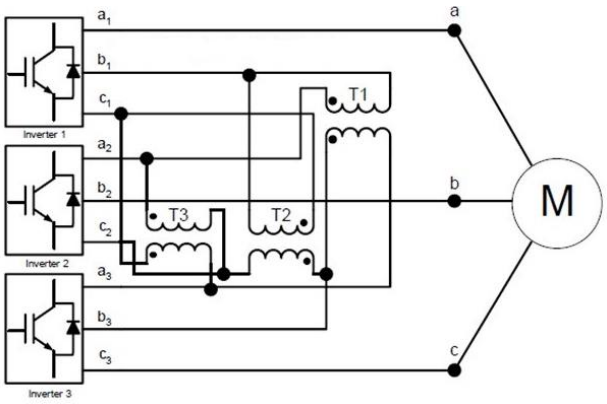

Figure 5. Cascaded Inverter with transformer

Disadvantages of Cascade H Bridge Multilevel Inverters

- Every H Bridge needs a separate dc source
- Limited applications due to large number of sources

Diode Clamped Multilevel Inverter

Diode clamped multilevel inverters use clamping diodes in order to limit the voltage stress of power devices. It was first proposed in 1981 by Nabae, Takashi and Akagi and it is also known as neutral point converter. A *k* level diode clamped inverter needs (2*k* – 2) switching devices, (k – 1) input voltage source and (k – 1) (k – 2) diodes in order to operate. *Vdc* is the voltage present across each diode and the switch. Single phase diode clamped multilevel inverter is shown in the fig.6.

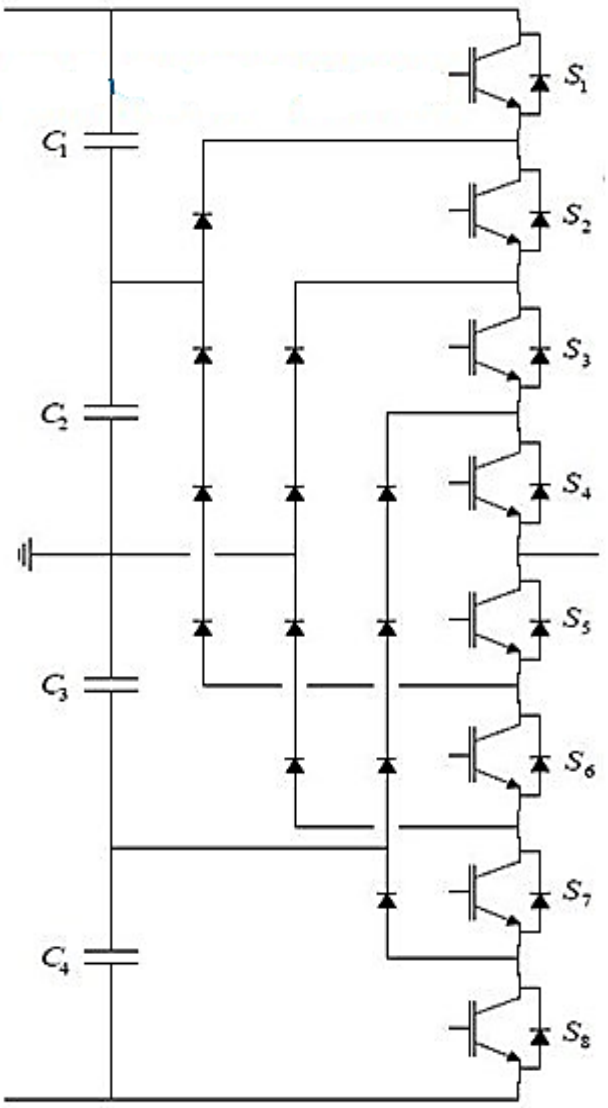

Figure 6. One phase of a diode clamped inverter

The concept of diode clamped inverter can better be understood by looking into three phase six level diode clamped inerter. Here the common dc bus is shared by all the phases, use five capacitors and six levels. Each capacitor has a voltage of Vdc and same is the voltage limit of switching devices. One important fact should be noted while considering the diode clamped inverter is that five switches will remain ON at any time. Six level, three phase dc clamped multilevel inverter is shown in the figure below.

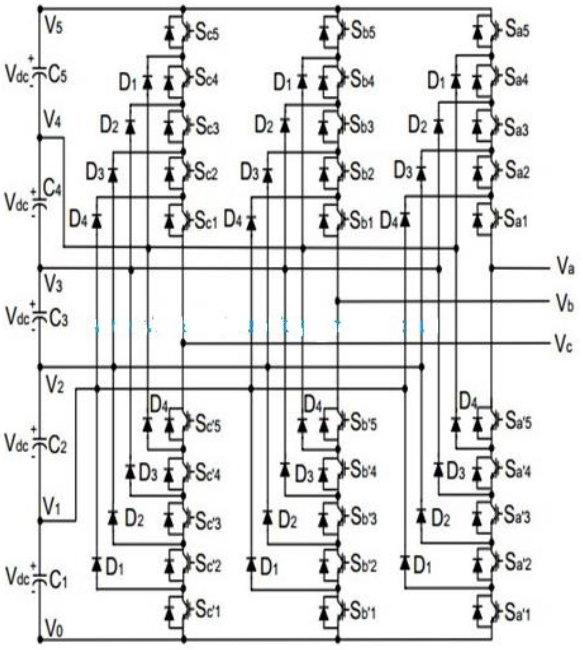

Figure 7. Six level three phase inverter

Outputs of each phase can be understood by the following table. Here reference voltage is the negative Vo. Condition 0 means switch is OFF and vice versa. Output waveforms of six level dc clamped inverter is shown below:

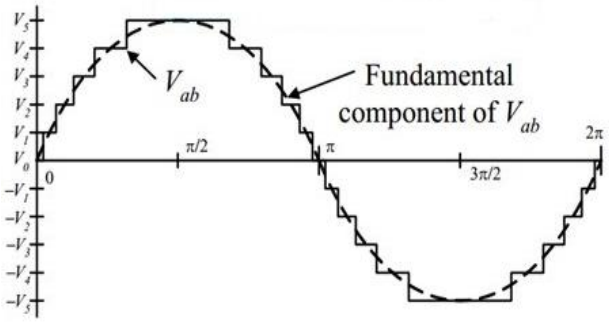

Figure 8. Waveform of Six Level Inverter

V_{ab} is the voltage due to the phase lag b and a voltage.

Applications of Diode Clamped Multilevel Inverters

The most common application of diode clamped multilevel inverter is when a high voltage Dc and Ac transmission lines are interfaced. This can also be used in variable speed control of high power drives. Static variable compensation is also an application of diode clamped multilevel inverters.

Advantages of Diode Clamped Multilevel Inverters

- Capacitance of the capacitors used is low.
- Back to back inverters can be used.
- Capacitors are pre charged.
- At fundamental frequency, efficiency is high.

Disadvantages of Diode Clamped Multilevel Inverters

- Clamping diodes are increased with the increase of each level. Dc level will discharge when control and monitoring are not precise.
-

Flying capacitor multilevel inverter

The configuration of this inverter topology is quite similar to previous one except the difference that here flying capacitors is used in order to limit the voltage instead of diodes. The input DC voltages are divided by the capacitors here. The voltage over each capacitor and each switch is V_{dc}. A k level flying capacitor inverter with $(2k-2)$ switches will use $(k-1)$ number of capacitors in order to operate. Figure below shows a five level flying capacitor multilevel inverter.

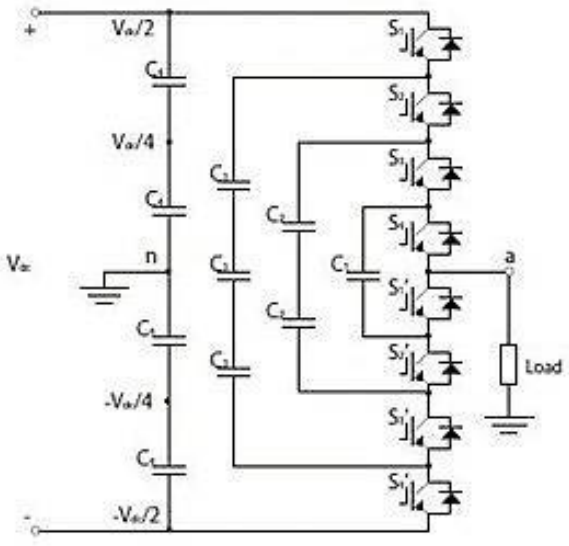

Figure 9. A Flying Capacitor Multilevel Inverter with five voltage levels

If we compare above figures, it shows that the number of switches, main diodes and DC-bus capacitors are same in both the cases. The only difference between the

two topologies is that the previous one uses clamping diodes in order to limit the voltage while this topology uses flying capacitors for this purpose, and as capacitors are incapable of blocking the reverse voltage, which diodes do, the number of switches also increases. Voltage on each capacitor is differing from the next as it has a ladder structure. Voltage difference between two back to back capacitors determines the voltage in the output frame.

Advantages of Flying Capacitor Multilevel Inverters
Static var generation is the best application of Capacitor Clamped Multilevel Inverters.

- For balancing capacitors' voltage levels, phase redundancies are available.
- We can control reactive and real power flow.

Disadvantages of Flying Capacitor Multilevel Inverters

- Voltage control is difficult for all the capacitors
- Complex startup
- Switching efficiency is poor
- Capacitors are expensive than diodes

III. RESULTS AND DISCUSSION

Proposed Model

The solution for the reduction of harmonic distortions can be obtained by using generalized multilevel inverters with self-voltage balancing. Generalized multilevel inverters can balance each dc voltage level automatically without any assistance from other circuits; whereas diode-clamped and capacitor-clamped multilevel inverters need external circuits for voltage balancing for levels greater than three. Multilevel inverters have the ability to reduce the voltage stresses on each power device due to the utilization of multiple levels on DC bus. These multiple levels are produced by self-balanced voltages which are adopted by different switching actions so that it results in reduction of harmonics. From this generalized multilevel inverter we can also derive different topologies like diode-clamped, capacitor-clamped multilevel inverters and flying capacitor multilevel inverter.

Fig. 7 shows the generalized multilevel inverter topology per phase leg, where each switching device, diode, or capacitor's voltage is 1 V. Any inverter with any number of levels including the conventional two level inverter, can be obtained from this generalized topology as shown in the figure. For example, the two-level inverter phase leg can be obtained by cutting off at the "2-level line," three level inverter leg by cutting off at the "3-level line," and so on, as shown in Fig. 7. It is evident that an M-level inverter can be constructed by the basic cell as shown in the inset of Fig 7. The generalized M-level phase leg (Fig 7) is a horizontal pyramid of the basic cells. Since the basic cell is a two-level phase leg, this generalized multilevel inverter is called the P2 multilevel inverter.

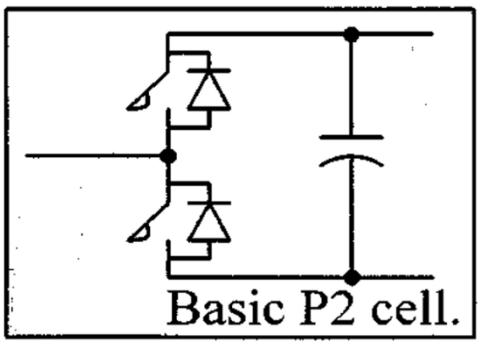

Figure 10. Basic p2 cell

To explain the operating principle and analyze the circuit, the five-level circuit is used hereafter. Fig.11 shows the generalized five-level inverter phase leg (or five-level P2 inverter phase leg). In Fig. 11, switches Sp1–Sp4 and Sn1–Sn4 and diodes Dp1–Dp4 and Dn1–Dn4 shown in bold lines are the main devices to produce desired voltage waveforms. The rest of the switches and diodes are for clamping and balancing the capacitors' voltages, i.e., voltage levels. Each component's voltage stress is 1 V. All voltage levels are self-balanced through clamping switches and clamping diodes. The circled (both solid and dashed lines) devices indicate on-state devices and current path. The un circled devices are off-state devices. In addition, the solid-line circled devices are the on-state devices necessary to produce the desired voltage level, whereas the dashed-line circled ones are the on-state devices to keep their capacitors' voltages balanced, i.e., for balancing and clamping purpose.

For example, in Fig. 11, switches Sn1–Sn4 are gated on to produce zero (0) voltage (i.e., , the zero potential is

referenced to the negative rail of the dc bus). The dashed-line circled devices are gated on to clamp and balance voltages. The switches Sc1, Sc5, and Sc11 are gated on so that the capacitors C_1, C_3, C_6, and C_{10} are connected in parallel to balance their charges (i.e. $V_{C1}=V_{C3}=V_{C6}=V_{C10}$). Similarly, the switches Sc3 and Sc9 are gated on so that the capacitors C_2, C_5, and C_9 are charge-balanced (i.e.$V_{C2}=V_{C5}= V_{C9}$). And Sc7 is gated on letting C_4 and C_8 be charge-balanced (i.e. $V_{C4}=V_{C8}$). There are three other alternative switching states as shown in Table I to produce V and balance capacitors' charges. In this way, all capacitors' voltage can be balanced. One can infer the following switching rules:

1) Each switch pole is an independent switching unit
2) Any adjacent two switches of each switch pole are complementary, (i.e., if one is on the other is off and vice versa);
3) If any switch's state is determined or known then the rest switches of the pole are automatically determined because of the complementary rule.

Table I summarizes the switching states to generate 0-, 1-, 2-, 3-, and 4-V voltage levels. Only Sp1-Sp4's states are shown because the complementary rule uniquely determines all remaining switches' states.

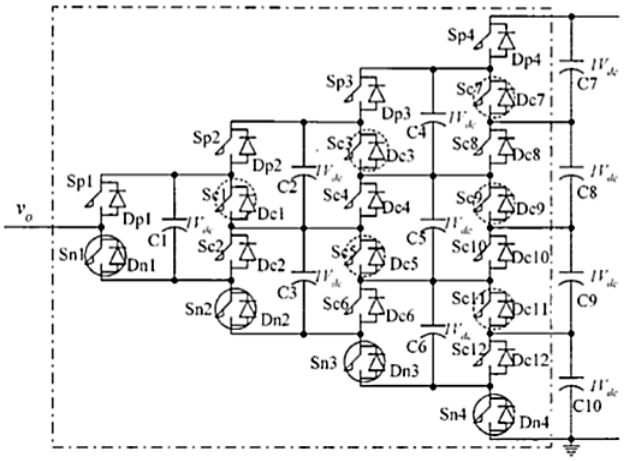

Figure 11. Five level inverter

Table 1

Output Voltage	Capacitor* Path	Switch States**			
		Sp1	Sp2	Sp3	Sp4
0Vdc	None	0	0	0	0
1Vdc	+C1	1	0	0	0
	-C1 + C2+C3	0	1	0	0
	-C3-C2 + C4+C5+C6	0	0	1	0
	-C6-C5-C4 + C7+C8+C9+C10	0	0	0	1
2Vdc	+C2+C3	1	1	0	0
	-C1 + C4+C5+C6	0	1	1	0
	-C3-C2 + C7+C8+C9+C10	0	0	1	1
	+C1 –C3-C2 +C4+C5+C6	1	0	1	0
	+C1 – C6-C5-C4 + C7+C8+C9+C10	1	0	0	1
	-C1+C2+C3-C6-C5-C4+C7+C8+C9+C10	0	1	0	1
3Vdc	+C4+C5+C6	1	1	1	0
	-C1 +C7+C8+C9	0	1	1	1
	+C2+C3–C6-C5-C4+C7+C8+C9+C10	1	1	0	1
	+C1 –C3-C2 +C7+C8+C9+C10	1	0	1	1
4Vdc	+C7+C8+C9+C10	1	1	1	1

Simulation and Results

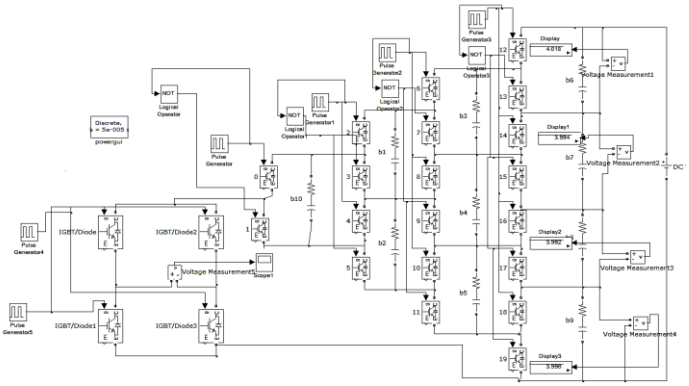

Figure 12. A Simulink model of the proposed model

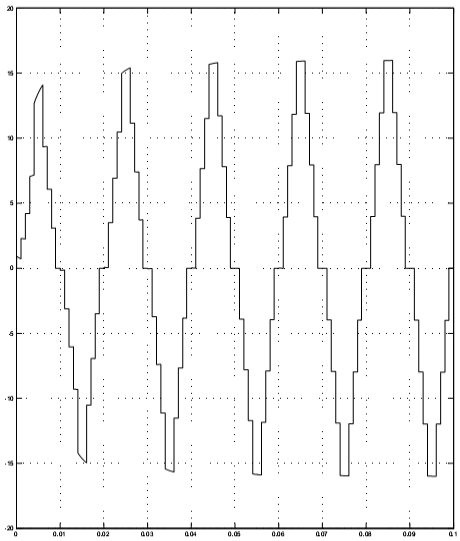

Figure 12. b

A simulation model for the generalised multilevel inverter is developed in Mat lab and SIMULINK co-simulation platform shown in in fig.12.a. The inverter output is a nine level phase voltage shown

in fig.12.b. The THD window is shown in fig.12.c

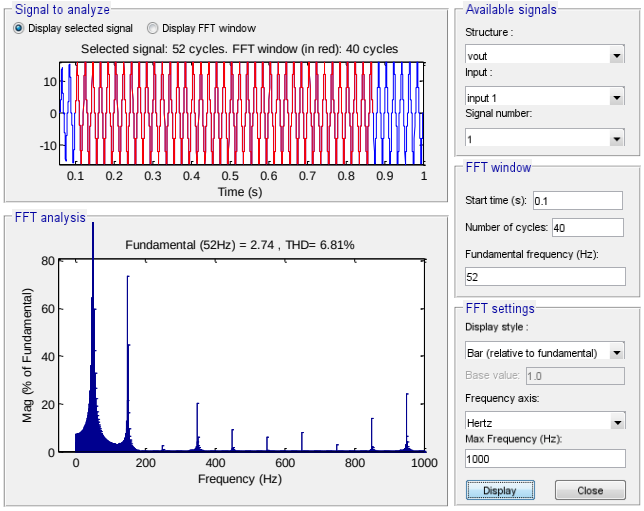

Figure 12. c

IV. CONCLUSION

The paper presents the main circuit model in Mat lab and simulation results in detail. This project has presented a generalized multilevel inverter topology. The existing multilevel inverters can be derived from this generalized structure. It has been demonstrated that the generalized multilevel inverter has self-voltage-balancing ability that the existing multilevel inverters do not have for the number of levels greater than three and for real power conversion. Although the generalized multilevel inverter needs a lot of clamping switches, diodes, and capacitors, in principle, it is a true and complete multilevel inverter (or converter).

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