

A Flyback Converter Fed Multilevel Inverter for AC Drives

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ABSTRACT

This paper presents a flyback converter fed cascaded multilevel inverter drive having developed H-bridge. The DC supply required for the inverter is developed with a flyback converter with multiwindings at the secondary. An algorithm to determine the value of DC sources required for an N level inverter is also proposed. Multilevel inverter topology was developed in order to increase the number of output levels and to reduce the number of power switches, driver circuits and the total cost of inverter. Both 7 level and 31 level inverter was simulated and verified in MATLAB/Simulink environment. The values of DC sources were made different to increase the output voltage level without increase in number of switches and voltage source. This topology can be used for high power motors. THD levels of both the inverters are also compared in this paper.

Keywords: Developed H-bridge, Multi-Level Inverter.

I. INTRODUCTION

The induction motor has well-known advantages of simple construction, reliability, ruggedness and low cost and has found very wide industrial applications. Furthermore, in contrast to the dc motor, it can be used in an aggressive or volatile environment since there are no problems with sparking and wear and tear. In the past induction motors and synchronous motors were employed mainly for constant speed applications because variable speed application of these drives are either too expensive or had very poor efficiency. But with the development of semiconductor converters employing thyristors, power transistors, IGBTs and GTOs they are widely used now a days. In this paper a converter-inverter section for AC drive application is explained.

A converter section will be used to convert the input DC voltage into required DC. Mostly inverters are used to convert this dc voltage into ac voltage at required voltage and frequency. So the most crucial step in the design of a drive is the inverter section. The converter used is a flyback converter with a specially designed flyback transformer having multiple winding so as to provide the required voltages for the inverter. The

inverter used for the drive is a multilevel inverter. The multilevel inverters have received more attention for their ability on high- power and medium voltage operation and because of other advantages such as high power quality, lower order harmonics, lower switching losses, and better electromagnetic interference. These multilevel inverters will generate stepped voltage waveform by using a number of dc voltage sources produced by the flyback converter. In this paper, in order to increase the number of output voltage levels and reduce the number of power switches, driver circuits, and the total cost of the inverter, a new topology of cascaded multilevel inverter is proposed. The magnitude of DC voltage is determined using a new algorithm. Both 7 level and 31 level inverter is simulated in MATLAB/Simulink and THD performance of both is compared.

II. PROPOSED SYSTEM

Fig 1 and 2 shows the proposed system for a seven level and thirty one level inverter. A flyback converter is specially designed to produce multiple output. The flyback converter is a Buck-Boost converter with the inductor of Buck-Boost converter split to form a flyback transformer. A flyback transformer is a multiwinding

coupled inductor, unlike true transformers. A flyback transformer is used as an energy storage device, where energy is stored in the air gap of the core. The inductor transformer should be designed to minimise the leakage inductance, AC winding losses and core losses.

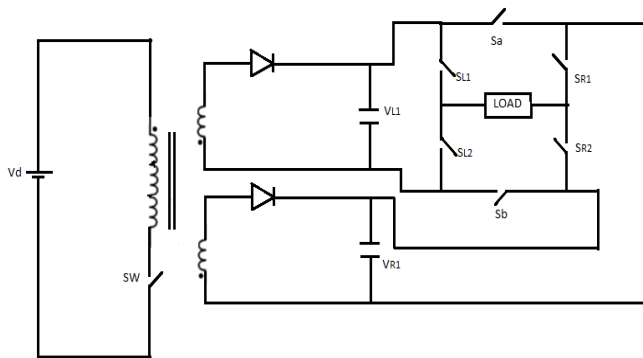


Figure 1. Schematic diagram of seven level drive system.

In recent years, industrial applications have begun to require higher power apparatus. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage. The major section of the drive are the converter, the inverter and control section. Each section of the proposed drive is explained in section II.a, II.b, II.c.

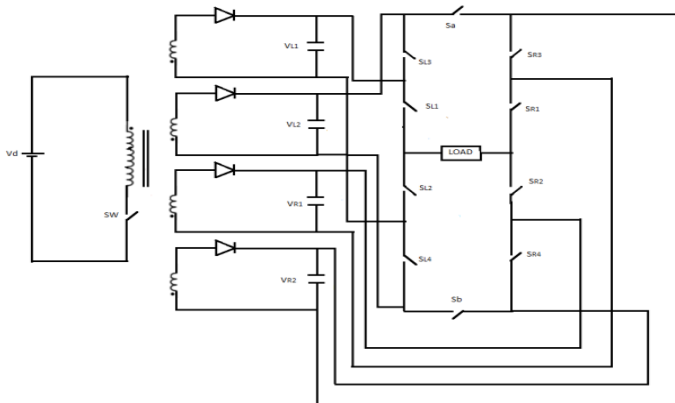


Figure 2. Schematic diagram of 31 level drive system

A. Flyback Converter

The flyback converter is equivalent to Buck-Boost converter with inductor split to form transformer. So the operating principle of both are similar. Fig 3 shows the operation of flyback converter during ON and OFF state.

- **SWITCH ON:** When the switch is closed, input get connected to the source. The primary current and magnetic flux increases storing energy in the transformer. The diode is reverse biased as the voltage induced in secondary winding is negative. During this period output capacitor supplies the load.
- **SWITCH OFF:** When the switch is opened, primary current and magnetic field drops but the secondary voltage becomes positive making the diode forward biased. During this period the energy from the transformer core recharges the capacitor and supplies the load.

The operation of storing energy in the transformer before transferring to the output of the converter allows the topology to easily generate multiple outputs with little additional circuitry.

Transformer can be classified by its primary secondary turns ratio, power size and secondary windings. If the voltage drop across switching MOSFET and output diode is ignored, the volt*second during the on time (T_{on}) should be equal to the volt*second during the off time (T_{off}), in steady state operation:

$$V_{in} \cdot T_{on} = V_{out} \cdot N_{ps} \cdot T_{off} \quad (1)$$

Primary and secondary inductance is calculated by defining maximum secondary ripple current. Secondary inductance is calculated as:

$$L_s = \frac{(V_o - V_{dfw})(1-D)}{\Delta I_s f_{sw}} \quad (2)$$

$$L_s = L_p N_{ps}^2 \quad (3)$$

MOSFET selection is based on:

- The drain to source breakdown of the MOSFET has to be greater than:

$$V_{ds} \geq \frac{N_p}{N_s} (V_o + V_{dfs}) + V_i \quad (4)$$

- Total power loss
- On state source to drain resistance.
- Maximum allowed operating temperature.
- Gate threshold voltage.

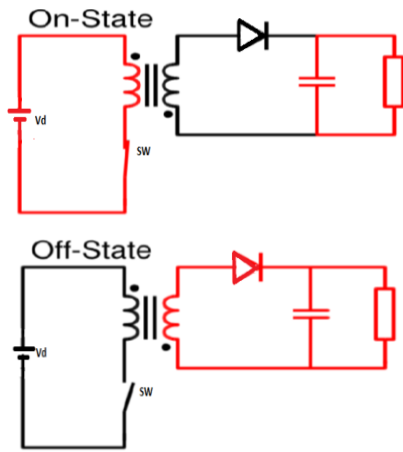


Figure 3. The on state & off state configuration of flyback converter

B. Multilevel Inverter

A new cascaded multilevel inverter topology is developed for proposed system. The seven level inverter is obtained by adding two switches and one dc source to the H-bridge. The proposed topologies are obtained by adding two unidirectional power switches and one dc voltage source to the H-bridge inverter structure. In other words, the proposed inverters are comprised of six unidirectional power switches ($S_a, S_b, S_{L1}, S_{L2}, S_{R1}$ and S_{R2}) and two dc voltage sources (V_{L1} and V_{R1}). This topology is called developed H-bridge.

TABLE 1: Switching Table of seven level inverter

S_{L1}	S_{L2}	S_{R1}	S_{R2}	S_a	S_b	V_o
1	0	0	1	0	1	V_{L1}
1	0	0	1	1	0	$-V_{R1}$
1	0	1	0	0	1	$(V_{L1} + V_{R1})$
1	0	1	0	1	0	0
0	1	1	0	1	0	$-V_{L1}$
0	1	1	0	0	1	V_{R1}
0	1	0	1	1	0	$-(V_{L1} + V_{R1})$

The simultaneous turn-on of S_{L1} and S_{L2} (or S_{R1} and S_{R2}) causes the voltage sources to short-circuit. Therefore, the simultaneous turn-on of S_{L1} and S_{L2} (or S_{R1} and S_{R2}) must be avoided. In addition, S_a and S_b should not turn on, simultaneously. Table 1 shows the switching states

of the six switches for the production of different voltage levels. In this table, 1 and 0 indicate the ON and OFF states of the switches, respectively. From the table it is clear that if the values of the dc voltage sources are equal, the number of voltage levels decreases to three. Therefore, the values of dc voltage sources should be different to generate more voltage levels without increasing the number of switches and dc voltage sources. Using the basic seven level higher level inverters can be developed.

The general topology consists of $2n$ dc voltage sources (n is the number of the dc voltage sources on each leg) and $4n + 2$ unidirectional power switches. In the proposed general topology, the number of output voltage levels (N_{step}), number of switches (N_{switch}), number of dc voltage sources (N_{source}) and the maximum magnitude of the generated voltage ($V_{o,max}$) are calculated as follows:

$$N_{step} = 2^{2n+1} - 1 \quad (5)$$

$$N_{switch} = 4n + 1 \quad (6)$$

$$N_{source} = 2n \quad (7)$$

$$V_{o,max} = V_{Ln} + V_{Rn} \quad (8)$$

The variety of dc voltage sources and the value of blocking voltage of the switches have a significant effect in determining the cost of the inverter. The number of variety of the values of dc voltage sources ($N_{variety}$) and maximum blocking voltage of all the switches of the general topology ($V_{block,n}$) is calculated as follows:

$$N_{variety} = 2n \quad (9)$$

$$V_{block,n} = 4(V_{Ln} + V_{Rn}) \quad (10)$$

An algorithm is applied to determine the magnitude of dc voltage sources. The magnitudes of the dc voltage sources of the proposed general multilevel inverter can be obtained as follows:

$$V_{Lj} = 5^{j-1} V_{dc} \quad (11)$$

$$V_{Rj} = 2 * 5^{j-1} V_{dc} \quad (12)$$

$$V_{o,max} = 3 * 5^{n-1} V_{dc} \quad (13)$$

$$V_{blockn} = 12 * 5^{n-1} V_{dc} \quad (14)$$

C. Control Unit for Multilevel Inverter

The switching is done in such a way that voltage rises from zero to peak and then to zero forming positive half cycle and similarly in the negative half cycle sine wave. The instant of each switching is determined by the equation:

$$t = \sin^{-1} \left(\frac{V_o}{V_m} \right) \quad (15)$$

III. SIMULATION & RESULTS

In order to verify the performance of the proposed system simulation of prototype models of 7 level and 31 level system is done in MATLAB/ Simulink environment. Also the THD performance of 7 level and 31 level system are compared. In the process of simulation load is assumed as R-L load with R = 100 Ω and L = 55mH. The converter voltage is selected as 100V with MOSFET switching frequency 20kHz.

For the seven level inverter $V_{L1} = 5V$ and $V_{R1} = 10V$. The maximum output voltage of the converter will be 15V. Similarly 31 level inverter is also simulated. The simulation diagram and output voltage waveform is given Fig 5 and Fig 6 respectively.

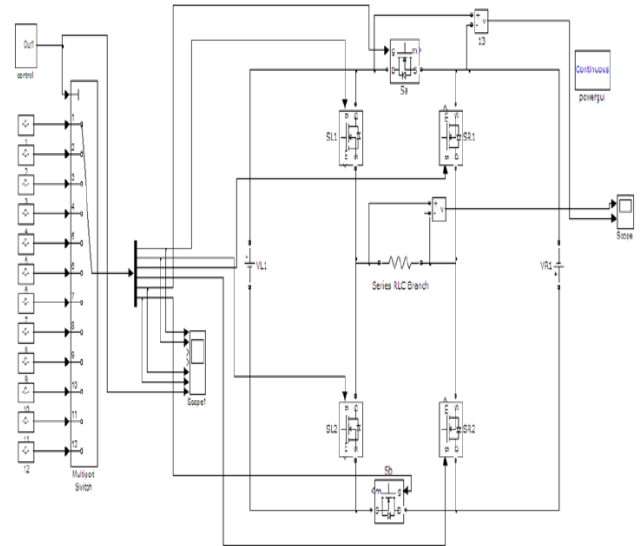


Figure 4. Simulation diagram of seven level inverter

THD analysis of 31 level and 7 level shows lesser THD is present in 31 level. As the level increase the output waveform approaches more and more to the sine. Fig 7 and Fig 8 shows the THD result of seven level and 31 level respectively.

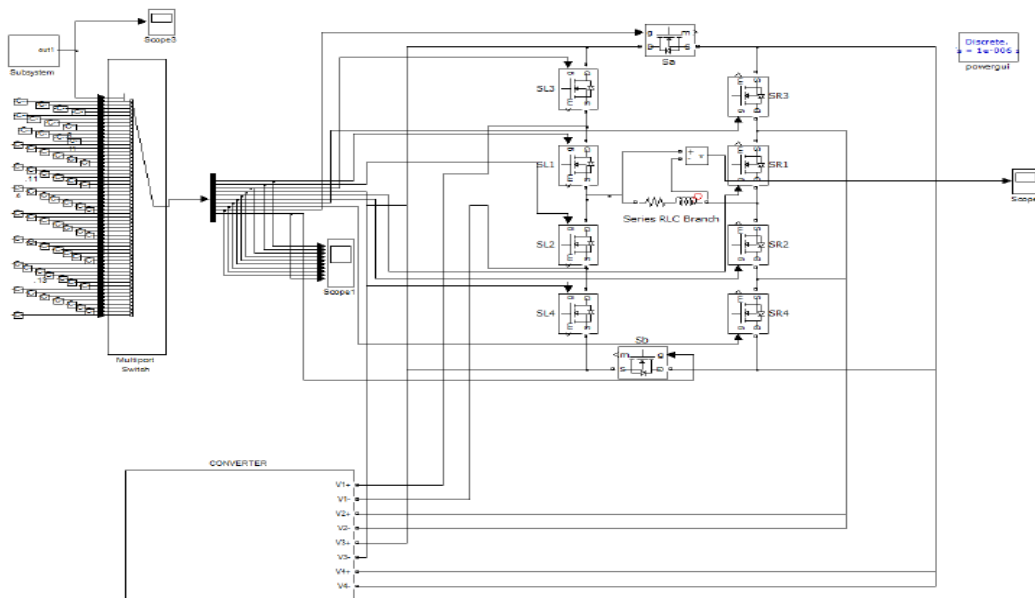


Figure 5 (a). Simulation diagram of 31-level inverter

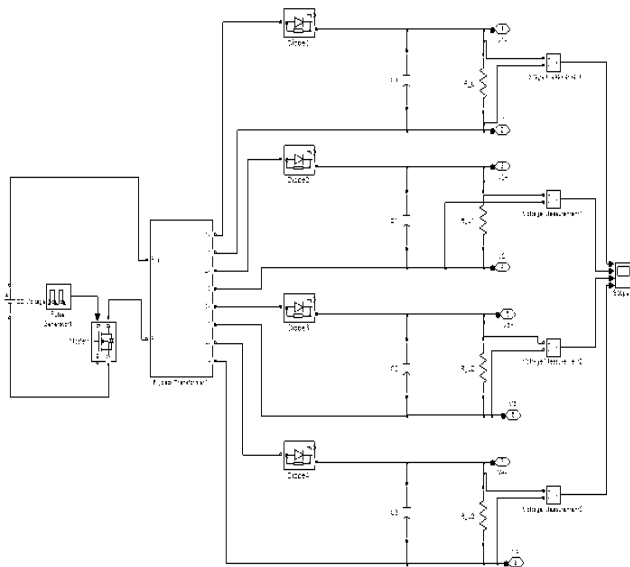


Figure 5(a) : Simulation diagram of flyback converter of 31-level inverter.

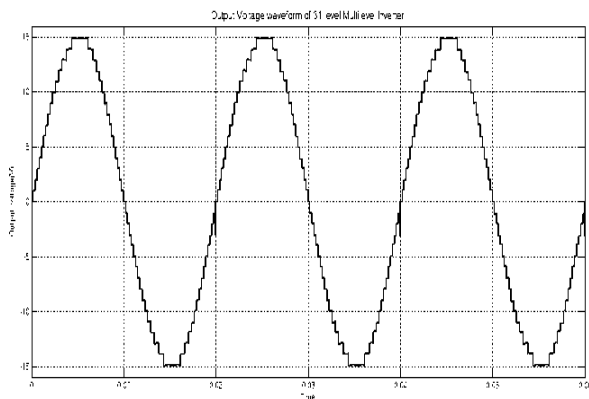


Figure 6: Simulink result of output waveform of 31 level inverter

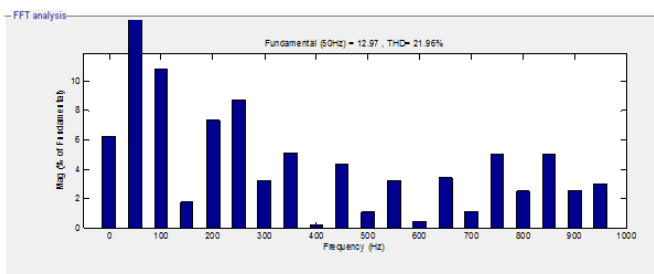


Figure 7: FFT window seven level inverter ,THD = 21.56%.

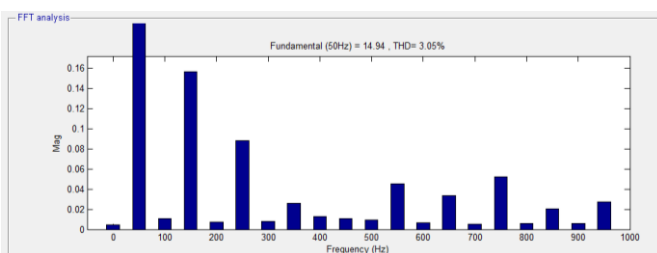


Figure 8: FFT window of thirty one level inverter ,THD = 3.05%

IV CONCLUSIONS

In this paper a drive system is proposed for medium voltage and high power applications in industries. Using the basic seven level higher level inverters can be developed. Here up to 31 level is simulated. The proposed system requires lesser no of switches driver circuits and dc voltage sources. Also the circuit shows THD results :7-level THD = 14.05 % and 31-level of 3.05% which is very important for a industrial application.

IV. REFERENCES

- [1] Ebrahim Babaei and Somayeh Alilu , "A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-Bridge," IEEE Trans.Industrial Electronics,Vol .61, no.8 Aug 2014 .
- [2] K. Wang and Y. Li,"Voltage balancing and fluctuation suppression methods of floating capacitors in a new modular multilevel converter," IEEE Trans.Ind. Electron,vol. 60, no. 5, pp. 1943–1954, May. 2013.
- [3] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, "A new topology of cascaded multilevel converters with reduced number of components for high-voltage applications," IEEE Trans. Power Electron , vol. 26, no. 11, pp. 3109–3118, Nov. 2011.
- [4] M. Narimani and G. Moschopoulos, "A novel single-stage multilevel type full-bridge converter," IEEE Trans. Power Electron.vol. no. 1, pp. 31–42, Jan. 2013.
- [5] M. Farhadi Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters," IEEE Trans. Power. Electron,vol. 28, no. 2, pp. 625–636, Feb. 2013.