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Using VFCB PWM Method Multilevel Inverter Balancing Switching Transitions

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ABSTRACT

A multi-level PWM technique has been developed to reduce the lower order harmonic distortion. The implementation of the existing control strategies has been found to affect the switch utilization and increase the losses. The Variable Frequency Carrier Band (VFCB) has been found to equalize the number of switching at all levels and contributes to reducing the losses besides allowing uniform dissipation of power in the switching devices. The existing SHPWM methods create inferior harmonic spectrum and unequal utilization of devices. Therefore, a new Pulse Width Modulation (PWM) strategy, with the view to ensure that the power devices at all the levels are switched equal number of times is proposed in this paper. The MATLAB-based simulation response and its experimental validation are included to highlight the fact that there is a significant enhancement in harmonic power distribution besides contributing to reduce the switching losses and improve the efficiency.

Keywords : Harmonics, modulation, multilevel inverter, THD, VFCB

I. INTRODUCTION

An "inverter" is a static circuit, which provides ac power from dc source with controllable voltage and frequency. The basic circuit for inversion is the H-bridge, which gives three level output ($+V_{dc}$, 0, $-V_{dc}$) i.e. A square wave and thus it can be named as a square wave inverter. Since the output is a square wave the distortion is very high due to the fact that the harmonic spectrum contained lower order harmonics with higher magnitude. To clear out these harmonics, bulky filters are needed to be designed, whose response is never going to be ideal and thus the purpose remained unfulfilled. Thus the usage of a square wave inverter was restricted for some sophisticated applications.

To enhance the performance of a square wave inverter, the Pulse Width Modulation (PWM) strategy was proposed and it proved its significance in the same. The aim of PWM control is varying the output pulse width such that it is proportional to required output. Thus, the PWM control survives better for the inverter is Sinusoidal-PWM (SPWM). Here, a sine wave is the reference and triangular wave is taken as carrier, and comparison of both the signals gives pulses of varying widths proportional to the reference sine. Since the pulses are proportional to the sine wave, the output also takes the same fashion and thus the distortion is less. Also, the harmonics with high magnitude were shifted to a higher order decided by the number of commutations per cycle, which in turn is directly related to the frequency of the carrier signal.

This eased the filtering since no bulky inductance, capacitances are needed, and the size of the module was considerably reduced. This control method laid a strong base for the three level inverters and thus they are being made useful in some sophisticated applications and dominating in the last three decades.

II. METHODS AND MATERIAL

2. Multilevel Inverter-Prologue

Multilevel inversion is a scheme in which the output voltage is obtained in the form of steps such that the output is closer to a sine wave and thus lowering the distortion in its basic form itself. Multilevel inverters incorporate an array of power semiconductors and

capacitor voltage sources, the output of which generate voltage with stepped waveforms.

The distortion in the output gets lowered still more, if the number of level increases. But this increase in the number of level increases the complexity of the circuit and control. It is possible to achieve the same plane of distortion provided by a higher level inverter, in a lower level inverter, by controlling the switching fashion of the main components.

With the help of control strategies it is possible to achieve lower distortion in multilevel inverters with less number of levels (components). Considering the above statement, this project work is done on a seven level inverter (V_3, V_2, V_1, 0, $-V_1$, $-V_2$, $-V_3$).

The prospect of PWM control in multilevel inverters is very high because the output of a multilevel inverter is closer to a sine wave and thus has lower distortion, the pulses provided by PWM control is proportional to the sine reference, the combined effect of this both will yield better performance.

2.1 Need For Multilevel Inverter

In recent years, industry has begun to demand higher power requirement, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids (2.3, 3.3, 4.16, or 6.9 kV). For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage level.

The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors need to withstand only reduced voltages. With the devices or converter modules in series and balanced voltage sharing among them, the lower voltage-rated switches can be possibly used in high voltage multilevel inverters. Also the dv/dt of a multilevel inverter is not as high as of a three level inverter i.e. it follows the same fashion of a sine wave.

They draw input current with very low distortion and can operate at lower switching frequencies. They can generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings and in addition, with sophisticated modulation methods CM voltages can be eliminated. All these features of a multilevel inverter facilitate its application in highly sophisticated devices. For applications which could allow tolerable distortion, the multilevel inverter is suitable because it gives the required output at fundamental switching whereas a three level inverter need to be PWM controlled and output filtered, which increases the switching losses.

Multilevel inverters helped in the recent developments in the field of electric vehicles, which require lower distortion input. Thus the emergence of multilevel inverters totally ruled out the basic three level inverters for the reasons discussed above and also due to the fact that lower distortion is possible with optimum number of levels and the scope for application specific control strategy.

2.2 Types Of MLI

In recent years, industry has begun to stipulate higher power equipments, which now reach the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network. Today, it is rigid to connect a single power semiconductor switch directly to medium voltage grids (2.3, 3.3, 4.16, or 6.9 kV). For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels.

Cascaded H-bridge multilevel inverter (1975)

(i) Diode clamped multilevel inverter (1982) and
(ii) Flying capacitor multilevel inverter (1990s)

2.2.1 Cascaded H-Bridge Multilevel Inverter

A different converter topology introduced in 1975, which is based on the series connection of single-phase H-bridge inverters with separate dc sources (SDS's).Fig.2.1 shows the basic module of a single phase H-bridge inverter, in which the H-bridge consists of four power devices (which can be MOSFET, IGBT, GTO, etc...) and a dc source. As the output voltage of this H-bridge can be $+V_{DC}$, 0, or $-V_{DC}$. Note that there are two options for generating '0' output voltage. When the two output terminals are

connected either to the positive or the negative dc link, the output voltage equals '0'V. The switching states for the four power devices have the constraints, that the control signal for the device S_1 must be complement to S_2, similarly for S_3 and S_4 in order to prevent short-circuiting. The ac output of different H-bridges can be connected in series to achieve multiple voltage levels in the targeted waveform.

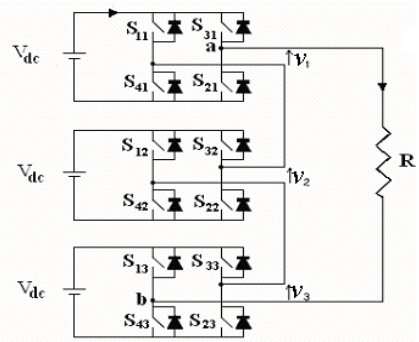


Figure 1. 7-level cascaded H-bridge inverter

Fig 1 shows the power circuit for single phase leg of a seven-level cascaded inverter with three H-bridges. Since the discussion here is about seven level inverter, we need three H-bridges and the seven levels of the output waveform are

$(+3V_{dc})\rightarrow(+2V_{dc})\rightarrow(+V_{dc})\rightarrow 0\rightarrow(-3V_{dc})\rightarrow(-2V_{dc})\rightarrow(-V_{dc}$ each H-bridge is operated for a definite interval of time so as to achieve any of the seven levels.

2.2.2 Diode-Clamped Multilevel Inverter

According to the original invention, the concept can be extended to any number of levels by increasing the number of capacitors. Fig2 shows the seven level diode clamped inverter in which the dc bus consists of three capacitors C_1, C_2, and C_3. For dc bus voltage.

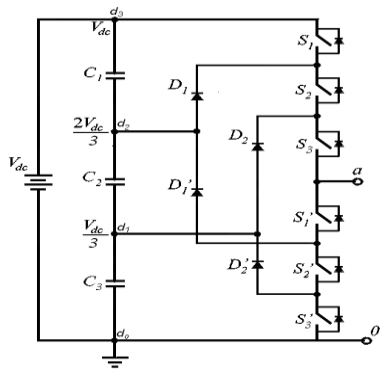


Figure 2. 7-Level Diode Clamped Inverter

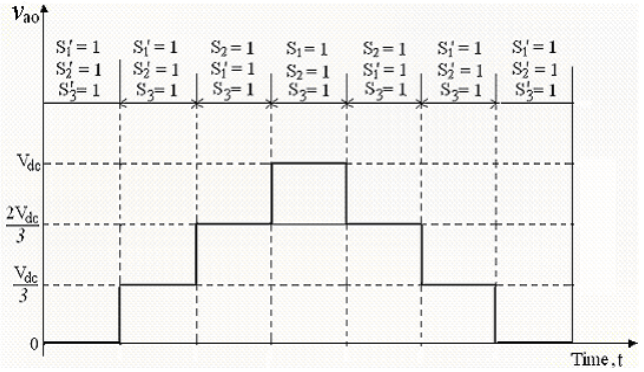


Figure 3. Output voltage and device conduction-seven level

Though each active switching device is only required to block a voltage level of V_{dc}/ (m-1), the clamping diodes must have different voltage ratings for reverse voltage blocking. It is worthwhile to note that diode's clamping action is only for V_{dc}/3 in all cases. Assuming that each blocking diode voltage rating is same as the active device voltage rating, the numbers of diodes required for each phase will be (m-1)x(m-2).

2.2.3 Flying Capacitor Multilevel Inverter

As described earlier the level can be increased by increasing the number of balancing capacitors. Fig.4 shows the seven level flying capacitor inverter which consists of (m-1)/2 dc bus capacitors and (m-1) balancing capacitors. For dc bus voltage V_{dc}, the voltage across each capacitor is V_{dc}/3 and each device voltage stress will be limited to one capacitor voltage level ($2V_{dc}$/ (m-1)).

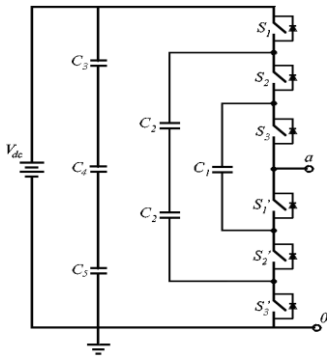


Figure 4. 7-Level Flying Capacitor Inverter

The voltage synthesis in a seven level capacitor clamped inverter has more flexibility than a diode clamped inverter. The voltage of the seven level phase leg a output with respect to the reference point. The

output voltage waveform of five level flying capacitor inverter is given in Fig 6 with device conduction details.

2.3. Multilevel Inverters Control Strategies

The scope of research in the area of circuit configuration is to reduce the number of active switches, clamping diodes; capacitors etc and this may lead to a configuration that gives better efficiency. But the output parameters like THD and fundamental voltage are not enhanced by modifying the configurations (theoretically). The fashion of switching the main components decides the quality of the output and the same is known as control strategy. As per the state of art, there are several control strategies for a multilevel inverter and but there is no evidence of comparison of all the control strategies.

2.3.1 Types Of Control Strategies

Basically the control strategies are classified into two types; they are natural sampling and regular sampling.

Natural Sampling

Natural sampling is a technique in which the switching instants are obtained by direct comparison of two quantities varying with time i.e. For example, a triangular wave is compared directly with a sinusoidal modulating wave to determine the switching instants in analog platform; termed as naturally sampled.

The natural sampling techniques for a multilevel inverter are categorized in two and they are:

(i) Single-Carrier SPWM (SCSPWM) and
(ii) Sub-Harmonic PWM (SHPWM)

Sub-Harmonic PWM is an exclusive control strategy for multilevel inverters and has further classifications. They are:

(i) Phase Disposition (PD)
(ii) Alternative Phase Opposition Disposition (APOD)
(iii) Phase Opposition Disposition (POD)
(iv) Phase Shifted Carriers (PSC)
(v) Carrier Polarity Variation (CPV) and
(vi) Variable Frequency Carrier Bands (VFCB)

Regular Sampling

When the scheming of the pulses is performed in digital platform, then it is termed as regular sampling. Here, the instantaneous values of both, the reference wave and carrier wave are sampled at regular intervals and formed as Look-Up Tables (LUT's) and are compared to get the corresponding pulse-widths. Mostly, the platforms for regular sampling are microprocessors and microcontrollers. The accuracy of regular sampling increases with the increase in number of samples but the same would occupy more memory.

2.3.1.1 Various Natural Sampling Techniques

Single-Carrier SPWM

The scheme in which a modulating sine wave is compared with a single carrier (triangle) is well known as SCSPWM. SPWM is very much successful in three level inverter and most of the high performance PWM methods are modified versions of basic SPWM. As concluded earlier, it is expected to give better results in multilevel inverters.

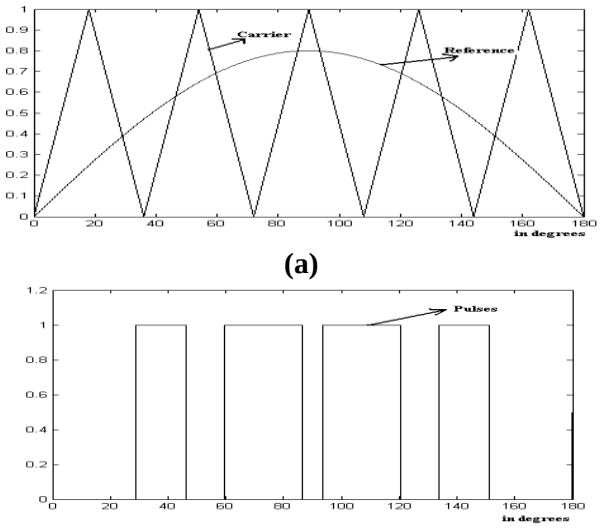


Figure 7. Single-Carrier SPWM- Pulses

Sub-Harmonic PWM

After understanding the problems with the SCSPWM, a completely new control strategy namely, Sub-Harmonic PWM (SHPWM) was evolved. It is also known as Multi-Carrier SPWM (MCSPWM), since a single modulating sine wave is compared with a number of carriers to decide the switching instants. Here, the carrier signals are stacked one over the other and thus the pulses can be easily discriminated for

different levels. The strategy of finding the switching instants can be understood from the Fig. 3.4.From the figure, it can be inferred that all the problems encountered in SCSPWM are ruled out in SHPWM i.e. the problem of discriminating the pulses for different levels is eased out in this case and also the chopping of the output voltage from the present level to zero (reference) level is avoided since the reference become over modulated for Level I and II.

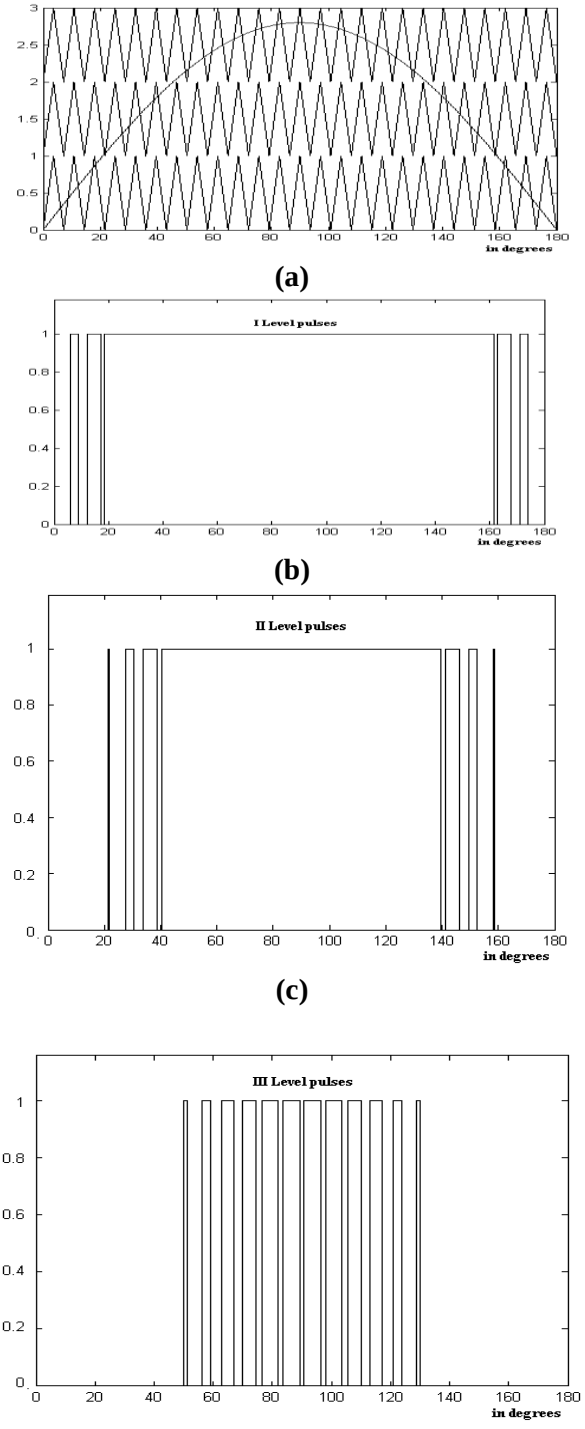


Figure 8. Sub-Harmonic PWM- Pulses

Various SHPWM Techniques

Sub-Harmonic PWM is also known as Multi-Carrier SPWM and thus several combinations of carriers can be made and each becomes a control technique. State-of-art shows that there are several such arrangements of the carriers and they are presented below.

Phase Disposition

This is basic SHPWM technique, in which all the carrier triangles are in-phase. The number of carriers is one less than the number of levels. The arrangement of the carriers is shown in the Fig 9.From the figure, it is clear that the carriers are in-phase and the above shown three carriers are for the positive half cycle and the same is repeated for the negative half cycle also and thus the total number of carriers is six i.e. one less than the number of levels for a seven level inverter.

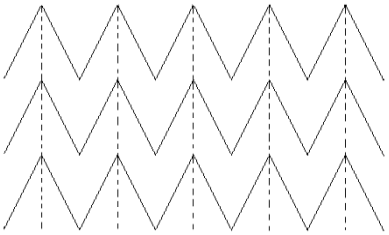


Figure 9. Carriers- PD

Alternative Phase Opposition Disposition

This is one another SHPWM techniques in which the carriers are arranged such that the alternate carriers are displaced from the adjacent by 180^0 i.e. the alternate carriers are phase opposing as shown in Fig 10.

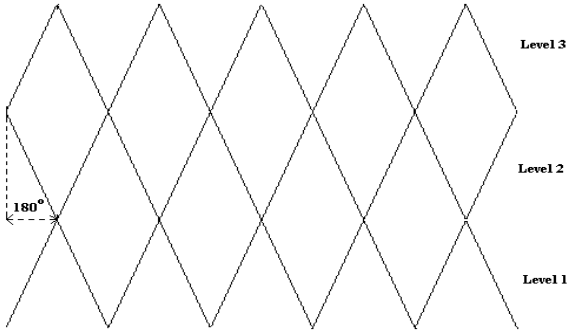
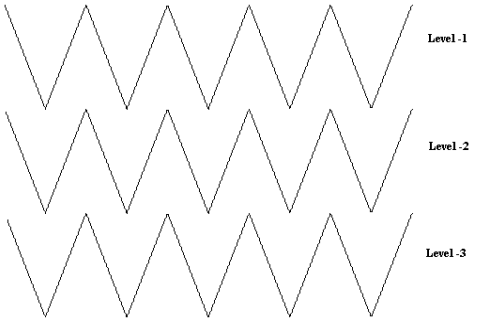


Figure 10. Carriers- APOD

Phase Opposition Disposition (POD)

In phase opposition disposition all negative level carriers and positive level carriers are in phase among their groups, but the negative carrier group is shifted by 180^0 from positive group. The arrangement of the carriers is shown in the Fig 11



(b)

Figure 11. Carriers- POD

Phase Shifted Carriers (PSC)

In this method, each carrier is shifted by an angle from the adjacent band carrier while Level I carrier is synchronized with reference wave. The shift in any negative level carrier is same as the respective positive level carrier.

Carrier Polarity Variation (CPV)

This is again a different arrangement of the carriers with respect to their polarities (180^0 shift). Here, different combination carriers are obtained by changing the polarity of the carriers in different levels and the Table: 3.1 given below, has some combinations with respect to the carriers polarity variations. The assigning of polarity to the carriers is not fixed and is viable to be changed. But, for the purpose of comparing all these combination, the carrier polarity shown in Fig. 3.8 is followed.

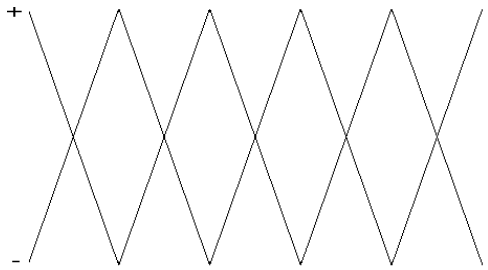


Figure 12. Polarity for carriers

III. RESULTS AND DISCUSSION

All the control methods discussed above where simulated for a seven level inverter with step voltages 100, 200 and 300 V in Matlab 7.0 and the results are presented below. The various techniques with sine as the reference (output frequency) and triangle as the carrier (M_f = 50) was simulated and it gave the result are presented.

The output of the seven level Cascaded Multilevel Inverter is shown in the fig 4.5 and the output voltage is measured as 300V.The Total harmonics are measured by using FFT analysis and the Harmonic spectrum are analysed all the three types of control strategies.

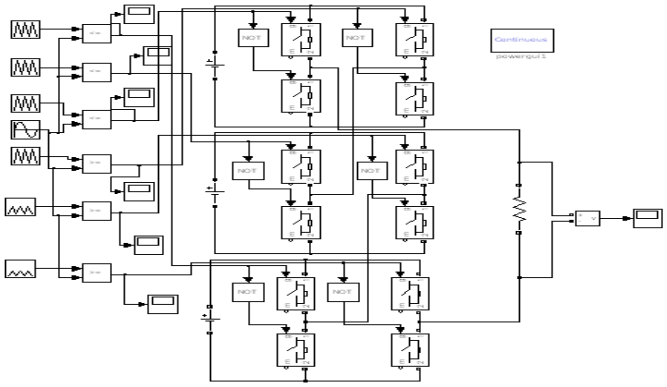


Figure 13. Simulation diagram of Phase Disposition

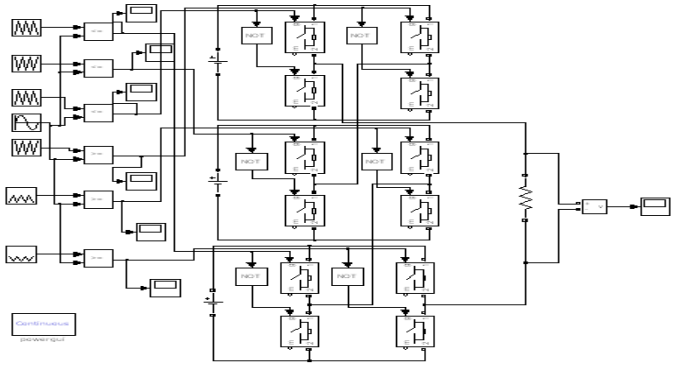


Figure 14. Simulation diagram of Alternate Phase Opposition Disposition

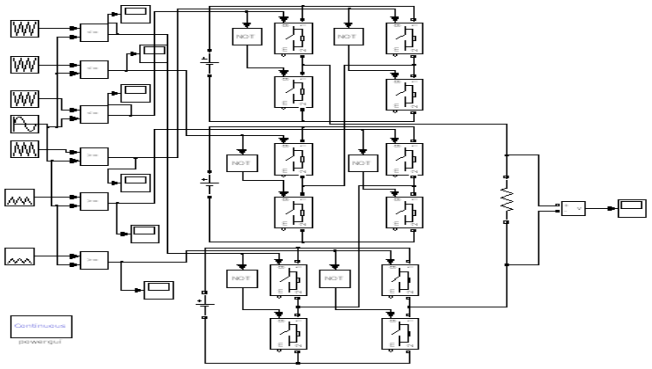


Figure 15. simulation diagram of Phase Opposition Disposition

Table 2. Comparison Result of control strategy

PARAMETER	PD	POD	APOD
Output Voltage	300V	300V	300V
THD	17.95%	19.64%	18.52%

IV. CONCLUSION

From the simulation results of the various SHPWM techniques, it can be inferred that there is no significant difference in the THD and fundamental voltage value. But, the spectral analysis of all these techniques gives various inferences and thus the research on the SHPWM techniques may lead to the betterment of the performance and ease the filtering. Phase Disposition is the basic SHPWM technique. In multilevel PWM, the switching frequency can be less than or greater than the carrier frequency and is a function of the displacement phase angle between the carrier set and the modulation waveform. By adjusting the displacement phase angle in multilevel PWM Switching strategies, switching losses can be minimized for a more efficient multilevel inverter.

V. REFERENCES

[1] Agelidis V. G. and Calais M. (1998) 'Application specific harmonic performance evaluation of multicarrier PWM Techniques', in Proc. IEEE PESC'98, pp. 172–178.

[2] Chen Y., Mwinyiwiwa B., Wolanski Z., and Ooi B. T.(1997) 'Regulating and equalizing DC capacitance voltages in multilevel STATCOM',IEEE Trans. Power Delivery, vol. 12, pp. 901–907.

[3] Corzine K.A. Wielebski M.W. Peng F.Z. and Wang J. (2004) 'Control of cascaded multilevel inverters', IEEE Transactions on Power Electronics, Vol. 19, No. 3, and pp.732–738.

[4] Choi N. S., Cho J. G., and Cho G. H. (1991)'A general circuit topology of multilevel inverter', in Proc. IEEE PESC'91, pp. 96–103.

[5] Choi N. S., Cho G. C., and Cho G. H. (1993) 'Modeling and analysis of a static var compensator using multilevel voltage source inverter', in Conf. Rec. IEEE-IAS Annu. Meeting, pp. 901–908.

[6] Fracchia M., Ghiara T., Marchesoni M., and Mazzucchelli M. (1992)'Optimized modulation techniques for the generalized N-level converter', in Proc. IEEE PESC'92, pp. 1205–1213.

[7] Liu H. L. and Cho G. H.(1994)'Three-level space vector PWM in low index modulation region avoiding narrow pulse problem', IEEE Trans. Power Electron., vol. 9, pp. 481–486.

[8] Menzies.R.W, Steimer P and Steinke J.K.(1994) 'Five-level GTO inverters for large induction motor drives', IEEE Trans. Ind. Applicat., vol. 30, pp. 938–944.

[9] Menzies R. W. and Zhuang Y. (1995) 'Advanced static compensation using a multilevel GTO thyristor inverter', IEEE Trans. Power Delivery, vol. 10, pp. 732–738.

[10] McGrath B.P. and Holmes D.G. (2002) 'Multicarrier PWM strategies for multilevel inverters', IEEE Transactions on Industrial Electronics, Vol. 49, No. 4, pp.858–867.

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