

Power Quality Improvement under Stiff Source Using Multifunctional DSTATCOM

G. Jahnavi^{*1}, K. Nagabhusanam²

^{*1}PG Student, Department of EEE, JNTUA, Ananthapuramu, Andhra Pradesh, India

²Lecturer, Department of EEE, JNTUA, Ananthapuramu, Andhra Pradesh, India

ABSTRACT

With Distribution static compensator (DSTATCOM) loads connected to stiff source cannot be protected from voltage disturbances. This paper provides a new fuzzy based control algorithm for multi-functional DSTATCOM is proposed to operate in voltage control mode which provides fast regulation at load point during disturbances and protects critical loads. During normal operating conditions the generated reference load voltages allow control of source currents. Simulation results are presented to show the efficiency of the proposed fuzzy based control algorithm and multifunctional DSTATCOM.

Keywords: Distribution Static Compensator (DSTATCOM), Fuzzy Controller, Multifunctional, Power Factor, Stiff Source, Voltage Regulation.

I. INTRODUCTION

The proliferation of power electronics devices, nonlinear loads, and unbalanced loads has degraded the power quality in the power distribution network [1]. To improve the quality of power, active power filters have been proposed [2]–[4]. The distribution static compensator (DSTATCOM) is a shunt active filter, which injects currents into the point of common coupling (PCC) (the common point where load, source, and DSTATCOM are connected) such that the harmonic filtering, power factor correction, and load balancing can be achieved.

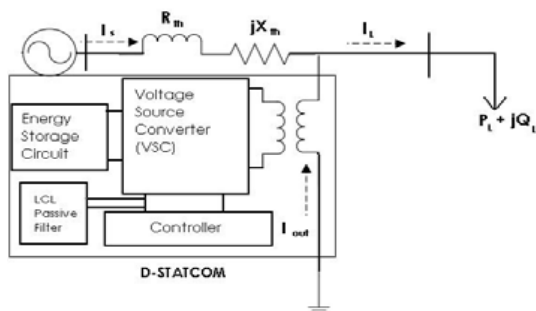


Figure 1. Basic DSTATCOM configurations

In practice, the load is remote from the distribution substation and is associated with feeder impedance. In the presence of feeder impedance, the inverter switchings distort both the PCC voltage and the source currents. In this situation, the source is termed as non-

stiff. If the same control algorithm for the stiff sources is used for the non-stiff sources, the reference currents generated will be erroneous, the load compensation using state feedback control of DSTATCOM can mitigate several power quality (PQ) problems, depending upon the mode of operation the basic configuration of DSTATCOM is shown in figure 1. In current control mode (CCM) [6], it injects harmonic and reactive components of load currents to make source currents balanced, sinusoidal, and in phase with load voltages. In voltage control mode (VCM), to protect sensitive loads from voltage disturbances such as sags, swells, transients and/or fluctuations it regulates load voltage. These two modes are not achieved simultaneously and these two modes objectives are different.

Based upon the distance between source and load, a source is termed as stiff or non-stiff. If the distance is long, then source is termed as non-stiff and has high feeder impedance, whereas if the distance is very small, then source is termed as stiff and has negligible feeder impedance. Generally, a source (stiff or non-stiff) supplies a permissible range of voltage, which is sufficient for satisfactory performance of load [7-10]. In this situation, DSTATCOM should operate in CCM. However, due to grid faults, the source voltage (stiff or non-stiff) will change, and then, the VCM operation is

required. DSTATCOM regulates the load voltage by indirectly regulating the voltage across the feeder impedance

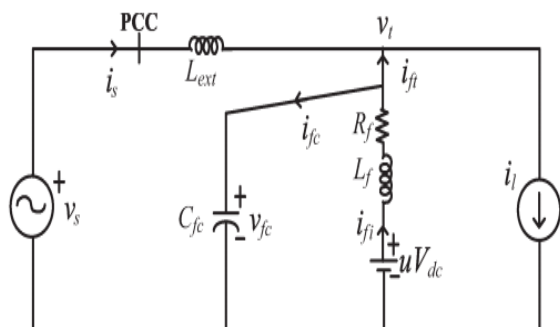


Figure 2. Single-phase equivalent circuit of DSTATCOM in a distribution network

When a load is connected to nearly a stiff source, feeder impedance will be negligible [11], [12]. Under these circumstances, DSTATCOM cannot provide sufficient voltage regulation at the load terminal, as there is lack of literature introducing the feasibility of the VCM operation of DSTATCOM under stiff source. In this paper, this problem is addressed while ensuring that, during normal operation, the advantages of CCM are retained. This paper proposes a new control-algorithm-fuzzy based DSTATCOM topology for voltage regulation even under stiff source. A DSTATCOM connected at the load terminal provides voltage regulation by indirectly regulating the voltage across the external inductor. This can be achieved by including an external inductor in series between the load and the source point at point of common coupling (PCC) point. In proposed control algorithm variable reference load voltages is formulated as a function of desired source current. This voltage indirectly controls the current drawn from the source for a permissible range of source voltage. Therefore, the control algorithm makes source currents balanced, sinusoidal, and in phase with respective to source voltages during normal operation. During voltage disturbances, a constant voltage is maintained at the load terminal. Hence, the proposed topology and the control algorithm make the compensator multifunctional, so that it provides fast voltage regulation at the load terminal and additionally provides advantages of CCM while operating in VCM. Simulation results are presented to show the efficiency of the proposed control algorithm and multifunctional DSTATCOM.

Based on the study situation aforementioned, the rest of this paper is organized as follows. The discussions of DSTATCOM configuration are presented in Section II, selection of external inductor in III. The proposed algorithm is discussed in Section IV. The further enhancement using fuzzy controller is discussed in section V. The performance evaluation accomplished by simulation is described in Section VI followed by concluding remarks.

II. METHODS AND MATERIAL

A. DSTATCOM Configuration And Proposed Algorithm

A neutral-point-clamped (npc) voltage source inverter (VSI) topology is chosen as it provides independent control of each leg of the VSI [7] and is shown in figure 3. A single-phase equivalent circuit of DSTATCOM in a distribution network is shown in Fig. 2. The VSI represented by uV_{dc} is connected to the load terminal through an LC filter ($L_f - C_{fc}$). The load terminal is connected to the PCC through an external series inductance L_{ext} . V_{dc} is the voltage maintained across each dc capacitor, and u is a control variable, which can be +1 or -1, depending upon switching state. i_{fi} , i_{ft} , and i_{fc} are currents through VSI, DSTATCOM, and C_{fc} , respectively. v_s and v_t are source and load voltages, respectively. A load consists of both linear and non-linear elements with balanced or unbalanced features. Load and source currents are represented by i_l and i_s , respectively.

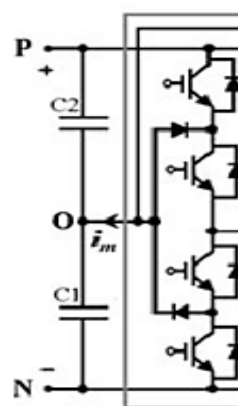


Figure 3. Basic NPC circuit for single-phase

B. Selection of External Inductor

During normal operation, external impedance (Z_{ext}) does not have much importance, but it plays an

important role during voltage disturbances. Based upon the DSTATCOM rating and amount sag to be mitigated will decide the value of external impedance. Assuming balanced source voltage, the source current in any phase at any time is given as

$$\bar{I}_s = \frac{V_s \angle 0 - V_t \angle -\delta}{R_{ext} + jX_{ext}} \dots \dots \dots (1)$$

Where V_s , V_t , R_{ext} , X_{ext} , and δ are the RMS source voltage, RMS load voltage, external resistance, external reactance, and load angle, respectively. For most practical case, $X_{ext} \gg R_{ext}$. As a worst case design, the reactive source current ($Im[\bar{I}_s]$), which is supplied by the compensator, will be maximum when δ is minimum. For this, the source will supply only losses in the VSI. Therefore, δ will be very small. Hence, $Im[\bar{I}_s]$ is given as

$$Im[\bar{I}_s] = \frac{V_t - V_s}{X_{ext}} \dots \dots \dots (2)$$

During voltage disturbances, to protect the sensitive loads, with focus on improving the DSTATCOM capability to mitigate deep sag. Therefore, keeping it into account, the load voltage during voltage sag is taken as 0.9 p.u. (per unit), which is sufficient to protect the load. Assuming that the reactive current that a compensator can inject is 20 A and considering with sag of 40% that the load needs to be protected, the value of external reactance is found to be

$$X_{ext} = \frac{0.9 - 0.6}{20} \times 230 = 3.45\Omega \dots \dots \dots (3)$$

The external reactance of 3.45Ω that corresponds to an inductance of 11mH for a 50-Hz supply system.

C. Proposed Control Algorithm

With proposed control algorithm during voltage disturbances aims to provide fast voltage regulation, while retaining the advantages of CCM during normal operation. First, the currents that must be drawn from the source are computed to get advantages of CCM using these currents, the magnitude of voltages that need to be maintained at the load terminal is computed. If this voltage magnitude lies within a permissible range, then the same voltage is used as reference voltage to provide advantages of CCM. If not in the range, it is a

sign of voltage disturbance, and a fixed voltage magnitude is selected as reference voltage.

A two-loop controller, whose output is load angle δ , is used to extract load power and VSI losses from the source. Finally, a discrete model is derived to obtain switching pulses. All these steps are presented in detail in this section.

i. computation of reference voltage magnitude (V_t^*)

Under normal operation, load voltage must be regulated in such a way that the following advantages provided by CCM operation are achieved.

- 1) Source currents are balanced and sinusoidal.
- 2) Unity power factor (UPF) at PCC.
- 3) Source supplies load average power and VSI losses.

To achieve all aforementioned objectives, the instantaneous symmetrical component theory [15] is used to get reference source currents. DSTATCOM makes the load voltages balanced and sinusoidal, but still may contain some switching harmonics, which will give unacceptable reference source currents when directly used. Therefore, positive sequence components of load voltages (v_{ta1}^+ , v_{tb1}^+ , and v_{tc1}^+) are extracted and used to compute reference source currents (i_{sa}^* , i_{sb}^* , and i_{sc}^*) as follows :

$$\begin{aligned} i_{sa}^* &= \frac{v_{ta1}^+}{\Delta_1^+} (P_{lavg} + P_{loss}) \\ i_{sb}^* &= \frac{v_{tb1}^+}{\Delta_1^+} (P_{lavg} + P_{loss}) \\ i_{sc}^* &= \frac{v_{tc1}^+}{\Delta_1^+} (P_{lavg} + P_{loss}) \dots \dots (4) \end{aligned}$$

Where $\Delta_1^+ = \sum_{j=a,b,c} (v_{tj1}^+)^2$, and P_{lavg} is the average load power that is calculated using a moving average filter (MAF). The total losses in the inverter, i.e., P_{loss} , computed using a fuzzy controller, helps in maintaining the averaged dc-link voltage ($V_{dc1} + V_{dc2}$) at a predefined reference value ($2V_{dcref}$) by drawing a set of balanced currents from the source and is given as

$$P_{loss} \equiv K_{pdc}e + K_{idc} \int e dt \dots \dots \dots (5)$$

Where K_{pdc} , K_{idc} and $e = 2V_{dcref} - (V_{dc1} + V_{dc2})$ are the proportional gain, integral gain, and voltage error of the PI controller, respectively. Once the reference

currents to be drawn from the source are computed using (4), reference voltages at the load terminal can be derived. Applying Kirchhoff's voltage law in the circuit shown in Fig. 2:

$$\bar{V}_s = \bar{I}_s Z_{ext} + V_t \angle -\delta \quad \dots (6)$$

Source voltage and source current will be in phase for the UPF operation. In addition, source voltage is taken as reference.

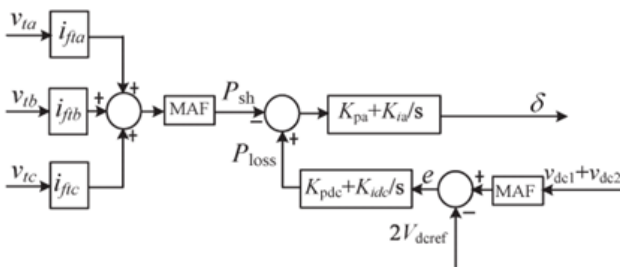


Figure 4. Controller to calculate δ and P_{loss}

\Therefore,

$$V_s = I_s (R_{ext} + jX_{ext}) + V_t \angle -\delta \quad \dots (7)$$

From the previous equation, the load voltage can be computed as follows:

$$V_t = \sqrt{(V_s - I_s R_{ext})^2 + (I_s X_{ext})^2} \quad \dots (8)$$

Based on standards, load voltage has a permissible range of variations between 0.9 and 1.1 p.u.[14]. Therefore, as long as V_t , obtained using (8), lies between 0.9 and 1.1 p.u., it is used as reference load voltage (V_t^*), and the advantages of CCM operation are achieved. Here, V_t is indirectly controlled by the desired source current. During sag and swell, the load voltage magnitude will be between 0.9 and 0.1 p.u. and 1.1 and 1.8 p.u., respectively, for half cycle to 1 min [16]. Therefore, reference load voltage magnitude is set to 0.9 and 1.1 p.u. during sag and swell, respectively. The reason to keep load voltages at these values is to maximize the DSTATCOM disturbance withstanding ability while keeping load voltage at the safe limits for satisfactory operation. Therefore, the following conclusions can be drawn:

$$\begin{aligned} & \text{If } 0.9 \text{ p.u.} \leq V_t \leq 1.1 \text{ p.u. then } V_t^* = V_t \\ & \text{Else if } V_t > 1.10 \text{ p.u. then } V_t^* = 1.1 \text{ p.u.} \\ & \text{Else if } V_t < 0.9 \text{ p.u. then } V_t^* = 0.9 \text{ p.u.} \quad \dots (9) \end{aligned}$$

ii. Computation of load angle (δ)

The block diagram of a controller to compute load angle δ is shown in Fig. 4 It ensures that the load average power and losses in the VSI are supplied by the source [7]. Alternately, P_{loss} responsible for maintaining dc-link voltage must be equal to shunt-link power P_{sh} . Comparing P_{loss} and P_{sh} , an error is generated, which is passed through a PI controller to compute δ as follows.

$$\delta = K_{pa}(P_{loss} - P_{sh}) + K_{ia} \int (P_{loss} - P_{sh})dt \quad \dots (10)$$

Where K_{pa} and K_{ia} are the proportional and integral gains of the inner PI controller, respectively. The value of shunt-link power P_{sh} is computed using a MAF as follows

$$P_{sh} = \frac{1}{T} \int_{t_1}^{t_1+T} (v_{ta} i_{fta} + v_{tb} i_{ftb} + v_{tc} i_{ftc}) dt \quad \dots (11)$$

A positive value of P_{sh} represents power flow from DSTATCOM to load terminal, whereas a negative value of P_{sh} represents power flow from load terminal to DSTATCOM. In steady state, VSI losses are compensated by taking power from the source. Hence, P_{sh} will be negative in steady state. Moreover, capacitor voltage decreases from its reference value in steady state. The deviation of capacitor voltage from reference voltage represents losses in the VSI. Hence, P_{loss} will be negative during steady state. Therefore, at all times, P_{sh} and P_{loss} should be equal. Hence, the difference of P_{sh} and P_{loss} should be minimized. The output of the inner fuzzy controller, as shown in Fig. 4, is delta, which ensures that shunt-link power P_{sh} drawn from the source equals to losses in the capacitor P_{loss} .

iii. Generation of instantaneous reference voltage

By knowing the zero crossing of phase-a source voltage, selecting a suitable reference load voltage magnitude from (9), and computing load angle δ from (10), the three-phase reference voltages are given as follows:

$$\begin{aligned} v_{trefa} &= \sqrt{2} V_t^* \sin(\omega t - \delta) \\ v_{trefb} &= \sqrt{2} V_t^* \sin(\omega t - \frac{2\pi}{3} - \delta) \\ v_{trefc} &= \sqrt{2} V_t^* \sin(\omega t + \frac{2\pi}{3} - \delta) \quad \dots (12) \end{aligned}$$

Where ω is the system frequency.

iv. Generation of Switching Pulses

Each phase of the VSI can be controlled independently, and hence, a discrete model of single phase has been derived to generate switching pulses. The dynamics of filter inductor and capacitor can be presented by the following equations:

$$\frac{dv_{fc}}{dt} = \frac{1}{C_{fc}} i_{fi} - \frac{1}{C_{fc}} i_{ft}$$

$$\frac{di_{fi}}{dt} = -\frac{1}{L_f} v_{fc} - \frac{R_f}{L_f} i_{fi} + \frac{V_{dc}}{L_f} u \dots \dots (13)$$

A matrix representation of (13) is given as follows:

$$\dot{x} = Ax + Bz \dots \dots (14)$$

Where

$$A = \begin{bmatrix} 0 & 1/C_{fc} \\ 1/L_f & -R_f/L_f \end{bmatrix}, \quad B = \begin{bmatrix} 0 & 1/C_{fc} \\ V_{dc}/L_f & 0 \end{bmatrix}$$

$$x = [v_{fc} \quad i_{fi}]^t, \quad z = [u \quad i_{ft}]^t$$

Equation (14), given in continuous form, can be represented in a discrete-time form as follows:

$$x(k+1) = Gx(k) + Hz(k) \dots (15)$$

Where matrices G and H are given as

$$G = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix}, \quad H = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix}.$$

From (15), capacitor voltage will be

$$v_{fc}(k+1) = G_{11}v_{fc}(k) + G_{12}i_{fi}(k) + H_{11}u(k) + H_{12}i_{ft}(k) \dots \dots (16)$$

The reference voltage v_{tref} is maintained at the load terminal. A cost function J is chosen as

$$J = [v_{tref}(k+1) - v_{fc}(k+1)]^2 \dots \dots (17)$$

Cost function is minimum when

$$v_{fc}(k+1) = v_{tref}(k+1) \dots \dots (18)$$

Finally, the reference discrete voltage control law is given as

$$u^*(k) = \frac{v_{tref}(k+1) - G_{11}v_{fc}(k) - G_{12}i_{fi}(k) - H_{12}i_{ft}(k)}{H_{11}} \dots (19)$$

$u^*(k)$ is regulated around a hysteresis band h to generate switching pulses of VSI using hysteresis control.

D. Fuzzy Logic Control

In recent years, the number and variety of applications of fuzzy logic have increased significantly. The applications range from consumer products such as cameras, camcorders, washing machines, and microwave ovens to industrial process control, medical instrumentation, decision-support systems, and portfolio selection.

In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC. The FLC comprises of three parts: fuzzification, interference engine and defuzzification. The FC is characterized as; i. Seven fuzzy sets for each input and output. ii. Triangular membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication using Mamdani's „min“ operator. v. Defuzzification using the „height“ method.

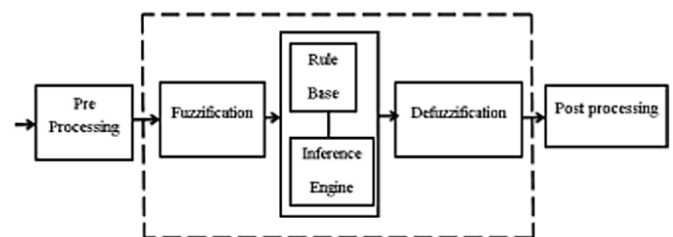


Figure 5. Fuzzy Logic Controller

In fuzzy Logic Toolbox software, fuzzy logic should be interpreted as FL, that is, fuzzy logic in its wide sense. The basic ideas underlying FL are explained very clearly and insightfully in Foundations of Fuzzy Logic. What might be added is that the basic concept underlying FL is that of a linguistic variable, that is, a variable whose values are words rather than numbers.

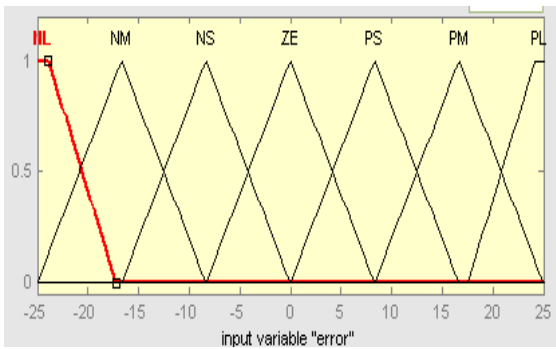


Figure 6. Membership function of voltage

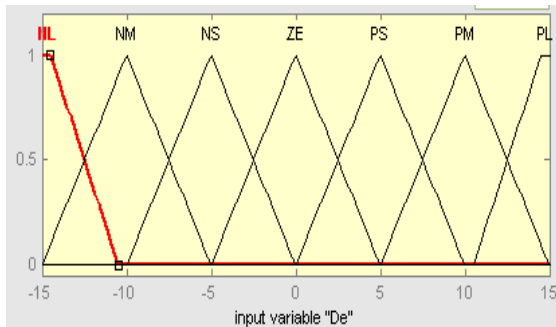


Figure 7. Membership function of voltage error

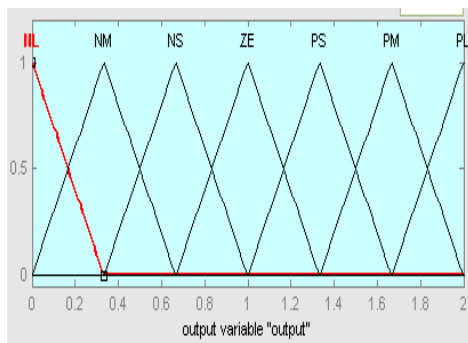


Figure 8. Membership function of output field voltage

In effect, much of FL may be viewed as a methodology for computing with words rather than numbers. Although words are inherently less precise than numbers, their use is closer to human intuition. Furthermore, computing with words exploits the tolerance for imprecision and thereby lowers the cost of solution.

ΔE \ E	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NM	NM	NS	ZE	PS
NS	NB	NM	NS	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PS	PM	PB
PM	NS	ZE	PS	PM	PM	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

Figure 9. Fuzzy Rules

When you save a fuzzy system to disk, you're saving an ASCII text FIS file representation of that system with the file suffix .fis. This text file can be edited and modified and is simple to understand. When you save your fuzzy system to the matlab workspace, you're creating a variable (whose name you choose) that will act as a mat lab structure for the FIS system. FIS files and FIS structures represent the same system.

Fuzzification

Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big). The partition of fuzzy subsets and the shape of membership function adapt the shape up to appropriate system. The value of input error $V_{dcerr(n)}$ and change in error CE (k) are normalized by an input scaling factor.

Fuzzy logic is the part of artificial intelligence or machine learning which interprets the human action. Computers can interpret only true or false values but a human being can reason the degree of truthness or degree of falseness. Fuzzy models interpret the human actions and are also called intelligent systems. Fuzzification is the process of changing a real scalar value into a fuzzy value. This is achieved with the different types of fuzzifiers. Fuzzy logic is a rule-based system. These rules are stored in the knowledge base of the system. The input to the fuzzy system is a scalar value that is fuzzified.

III. RESULTS AND DISCUSSION

Simulation Results

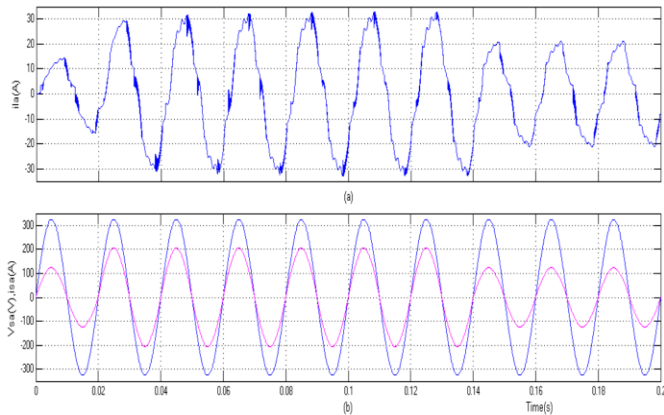


Figure 10. Phase-*a* waveforms before, during, and after load change. (a) Load current. (b) Source voltage and source current (current is scaled up ten times for clear visibility).

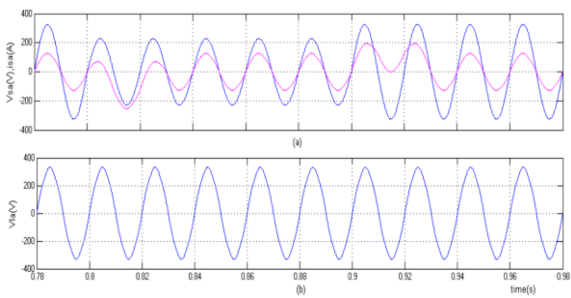


Figure 11. Phase-*a* waveforms before, during, and after sag. (a) Load voltage. (b) Source voltage and source current (current is scaled up ten times for clear visibility).

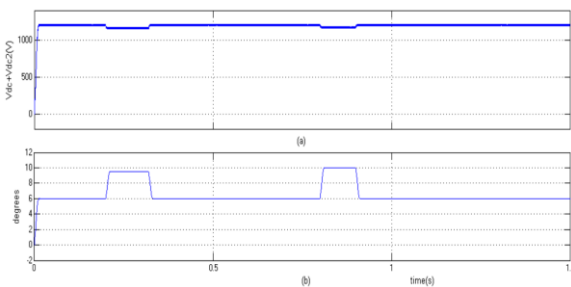


Figure 12. (a) Voltage across dc bus. (b) Load angle δ

The proposed control algorithm and multifunctional DSTATCOM make three-phase source currents balanced, sinusoidal, and in phase with respective source voltages at the PCC, within the permissible range of voltage. In addition, a fast voltage regulation at the load terminal is provided to protect sensitive loads during voltage disturbances. In addition, load harmonic and reactive current components are supplied by the

compensator all the time. All aforementioned advantages are simulated in MATLAB. A three-phase stiff source of 230 V rms per phase (1.0 p.u.) is considered. Filter parameters are $L_f = 20\text{mH}$, $C_f = 10\mu\text{F}$, $V_{dc} = 600\text{V}$, and $C_{dc} = 3000\mu\text{F}$. External inductance $L_{ext} = 11\text{mH}$ is used. Initially, a three-phase unbalanced linear and nonlinear load of 6.9 kW is connected. At $t = 0.2\text{s}$, load is increased to 9.6 kW. The increase in load current in phase-*a* is shown in Fig. 10(a). The source voltage and current waveforms of phase-*a* before and after the load change are shown in Fig. 10(b). It can be seen that both voltage and current are in phase with each other. The load is brought back to its normal value at $t = 0.32\text{s}$. The controller takes one cycle to detect this change and brings back the source current at its normal value. The current is in phase with source voltage. The entire transient is shown in Fig. 10(b).

To show the voltage regulation capability of DSTATCOM, at $t = 0.8\text{s}$, a sag is created by lowering the source voltage by 30%, as shown in Fig. 11(a). A fast voltage regulation is provided at the load terminal to protect sensitive loads, while maintaining a voltage of 0.9p.u. and is shown in Fig. 11(b). During sag period, source current will increase, as shown in Fig. 11(a). Voltage sag is cleared at $t = 0.9\text{s}$, and then, load voltage starts following the source voltage. Consequently, the source current and the source voltage slowly come in phase with each other as illustrated in Fig. 11(a). Fig. 12(a) shows the load angle δ , which is regulated by a controller to ensure that the average load power and inverter losses are taken from the source during normal operation, load change, and voltage disturbances. Fig. 12(b) shows the voltage at dc bus, which is regulated around 1200 V during the entire operation.

IV. CONCLUSION

In this paper, to protect the load from voltage disturbances under stiff source a new fuzzy based control algorithm for multifunctional DSTATCOM has been proposed. This has been achieved by placing an external series inductance of suitable value between the source and the load. In addition, instantaneous reference voltage is controlled in such a way that the source currents are indirectly controlled, and the advantages of CCM operation are achieved while operating in VCM for a permissible range of source voltage. The proposed algorithm and multifunctional DSTATCOM are able to

mitigate voltage- and current-related PQ issues, and simulation results have been presented.

V. REFERENCES

- [1]. A. Bhattacharya and C. Chakraborty, "A shunt active power filter with enhanced performance using ANN-based predictive and adaptive controllers," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 421–428, Feb. 2011.
- [2]. S. Rahmani, A. Hamadi, and K. Al-Haddad, "A Lyapunov-function-based control for a three-phase shunt hybrid active filter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1418–1429, Mar. 2012.
- [3]. M. K. Mishra and K. Karthikeyan, "An investigation on design and switching dynamics of a voltage source inverter to compensate unbalanced and nonlinear loads," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 2802–2810, Aug. 2009.
- [4]. J. Liu, P. Zanchetta, M. Degano, and E. Lavopa, "Control design and implementation for high performance shunt active filters in aircraft power grids," *IEEE Trans. Ind. Electron.*, vol. 59, no. 9, pp. 3604–3613, Sep. 2012.
- [5]. A. Bhattacharya, C. Chakraborty, and S. Bhattacharya, "Parallelconnected shunt hybrid active power filters operating at different switching frequencies for improved performance," *IEEE Trans. Ind. Electron.*, vol. 59, no. 11, pp. 4007–4019, Nov. 2012.
- [6]. Q.-N. Trinh and H.-H. Lee, "An advanced current control strategy for three-phase shunt active power filters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5400–5410, Dec. 2013.
- [7]. M. K. Mishra, A. Ghosh, and A. Joshi, "Operation of a DSTATCOM in voltage control mode," *IEEE Trans. Power Del.*, vol. 18, no. 1, pp. 258–264, Jan. 2003.
- [8]. H. Fujita and H. Akagi, "Voltage-regulation performance of a shunt active filter intended for installation on a power distribution system," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 1046–1053, May 2007.
- [9]. R. Gupta, A. Ghosh, and A. Joshi, "Performance comparison of VSC based shunt and series compensators used for load voltage control in distribution systems," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 268–278, Jan. 2011.
- [10]. F. Gao and M. Iravani, "A control strategy for a distributed generation unit in grid-connected and autonomous modes of operation," *IEEE Trans. Power Del.*, vol. 23, no. 2, pp. 850–859, Apr. 2008.
- [11]. Y.-R. Mohamed, "Mitigation of dynamic, unbalanced, and harmonic voltage disturbances using grid-connected inverters with LCL filter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 3914–3924, Sep. 2011.
- [12]. R. Gupta, A. Ghosh, and A. Joshi, "Multiband hysteresis modulation and switching characterization for sliding-mode-controlled cascaded multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2344–2353, Jul. 2010.
- [13]. A. Camacho, M. Castilla, J. Miret, J. Vasquez, and E. Alarcon-Gallo, "Flexible voltage support control for three-phase distributed generation inverters under grid fault," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1429–1441, Apr. 2013.
- [14]. M. Moradlou and H. Karshenas, "Design strategy for optimum rating selection of interline DVR," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 242–249, Jan. 2011.
- [15]. S. Srikanthan and M. K. Mishra, "DC capacitor voltage equalization in neutral clamped inverters for DSTATCOM application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2768–2775, Aug. 2010.
- [16]. J. Barros and J. Silva, "Multilevel optimal predictive dynamic voltage restorer," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2747–2760, Aug. 2010.