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Power Efficient Memory Design using MTCMOS Technique in 30nm Technology

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ABSTRACT

Sense amplifiers play an important role in memories like Dynamic Random Access and Static Random Access memories. A sense amplifier compares the bit line voltage and its complement amplifies it to rail to rail output voltages. This paper mainly concentrated on the design of low power sense amplifier. An analytical model of different sense amplifier has been derived and simulated using 30nm CMOS (Complementary metal oxide semiconductor) technology with variable supply voltage using MTCMOS (Multi Threshold CMOS) technique. MTCMOS is an effective circuit level technique that improves the performance and design low power cell by utilizing both low and high threshold voltage transistors. The conventional voltage latch sense amplifier designed using MTCMOS technique to perform better in terms of power dissipation is proposed in this paper using SYNOPSYS EDA tool.

Keywords : Memory, Sense Amplifier, Low Power, MTCMOS.

I. INTRODUCTION

On the modern trends quick memories are highly required with low power consumption. The low power and low voltage CMOS techniques were applied extensively in analog and mixed mode circuits for the compatibility with the present IC (Integrated Circuit) technologies [1].

There are several sources for the leakage currents: (i)sub threshold leakage current due to very low threshold voltage(VT), (ii) gate leakage current due to very thin gate oxide(TOX), As a result of an exponential dependency on the reduction of the threshold voltage, sub-threshold leakage has the potential to become the dominant factor in sub-100nm generations.

Power consumption of CMOS consists of dynamic and static components. Dynamic power is consumed when transistors are switching or active and static power is consumed regardless of transistor switching.

Low power consumption can be achieved by using sense Amplifiers which are main part of CMOS memory. Parasitic capacitance is much higher if memory is of high density [2]. To achieve a faster memory and less power dissipation to design sense amplifiers as, increase in number of cells per bit line which will increase the parasitic capacitance. Minimize supply voltage lead to short noise margin that affects the sense amplifier reliability.

The general CMOS and MTCMOS circuit [3] for the Conventional Voltage Latch Sense Amplifiers (CVLSA) and Current Mirror Sense Amplifier (CMSA) is designed using 30nm technology. The design of Low Power Conventional Voltage Latch Sense Amplifier is proposed in this paper.

This paper is organize as follows section II discusses the existing design and MTCMOS design of conventional voltage latch sense amplifier ,current mirror sense amplifier and Proposed design of conventional voltage latch sense amplifier. Section III describes the Simulation Part of the proposed design. Section IV concludes the paper.

II. SENSE AMPLIFIER DESIGNS

Sense amplifiers are commonly used in the read path of Cache memories [3]. Basically, the purpose of the sense amplifier circuit is to sense and then amplify a small voltage difference between the two input nodes, which prevents a full swing discharge on the aforesaid interconnects, and hence improves the cache access latency.

A. Conventional Voltage Latch Sense Amplifier

A commonly used latch sense amplifiers is conventional voltage latch type sense amplifier shown in Figure 1, is commonly used due to its advantages of low power dissipation and high speed.

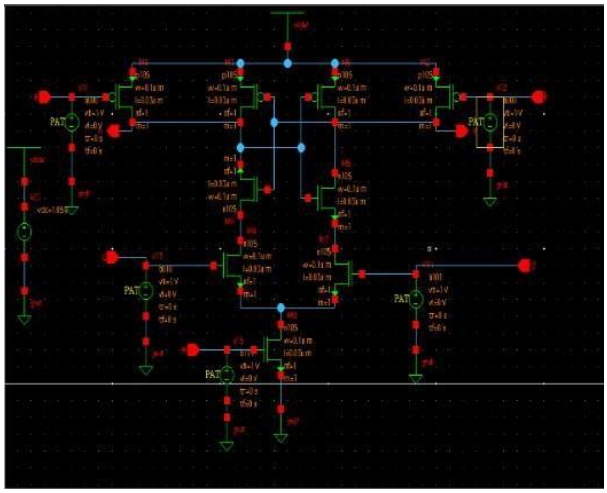

Figure 1: Design of Conventional Voltage Latch Sense Amplifier under 30nm technology

The internal nodes of this design are pre-charged through the bit-lines. The circuit design operates directly based on the voltage differential developed on its internal nodes by the input bit-lines[4].

B. Current Mirror Sense Amplifier

The Current Mirror Sense Amplifier is designed for high speed static random access memory applications [1].The CMSA can directly sense the current of memory cell and only needs two transistor stages cascaded from VDD to GND for achieving the low voltage operation.

The conventional current-mirror sense amplifier is easy to control with the sense-amplifier activation timing signal, SE and the speed of the current-mirror sense amplifier can be easily accelerated by increasing the operating current.

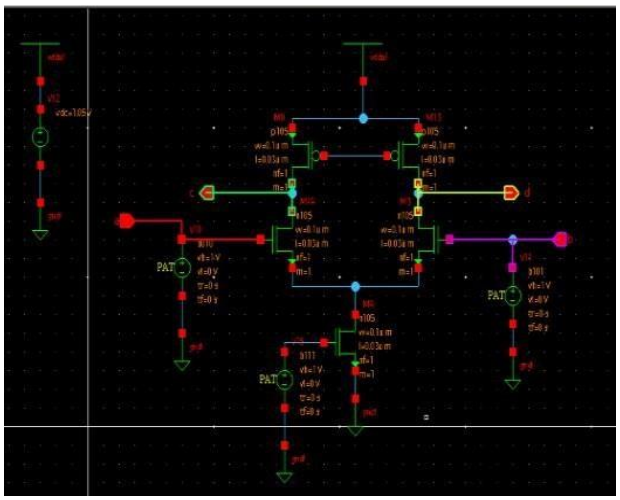

Figure 2 : Design of Current Mirror Sense Amplifier under 30nm technology.

Thus, memories frequently use this type of sense amplifier. However, the static current flows through the transistor connected to ground to accelerate the sense speed which needs more power. based on the voltage differential developed on its internal nodes by the input bit-lines[4].

C. Current Mirror Sense Amplifier using MTCMOS Technique

The current mirror sense amplifier circuit is designed using MTCMOS Technique using SYNOPSYS custom designer tool. The power consumed by the circuit designed using MTCMOS consumes less power than the general CMOS logic circuits for various supply voltages [9].

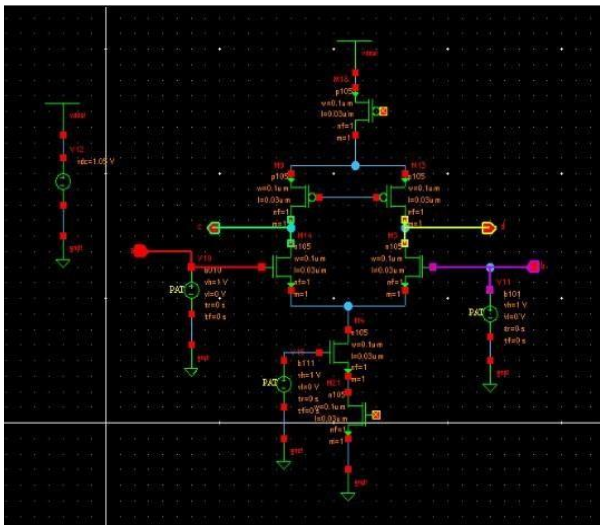

Figure 3 : Design of Current Mirror Sense Amplifier using MTCMOS technique under 30nm technology.

D. Proposed Design-Conventional Voltage Latch Sense Amplifier using MTCMOS Technique

The proposed design is conventional voltage latch sense amplifier circuit under MTCMOS Technique consumes less power than the other sense amplifier and holds good results. The design of proposed sense amplifier is designed using custom designer of SYNOPSYS tool under 30nm technology is shown in Figure 4.The proposed design is simulated for different supply voltages and examined for the power consumption.

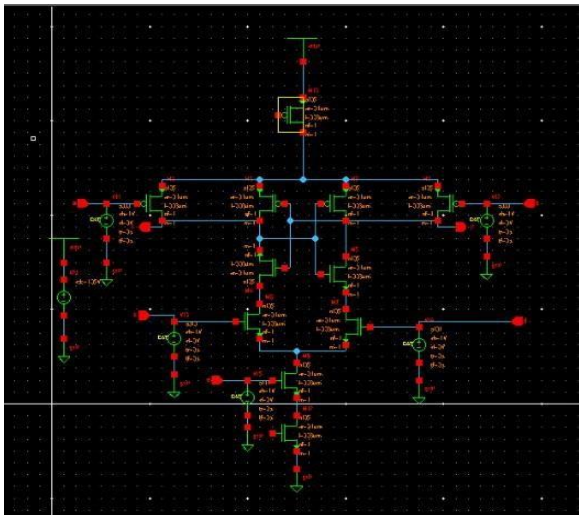

Figure 4 : Design of Conventional Voltage Latch Sense amplifier Using MTCMOS technique Under 30nm Technology.

The above proposed system is designed using MTCMOS technique, mainly used to reduce the power consumption of the circuit. The power reduction is mainly due to the low and high threshold voltage transistors used in the design. The low and high threshold voltage transistors used in the design are responsible for the power reduction in the design. The conventional voltage latch sense amplifier designed without low and high threshold voltage transistors holds high power while comparing to the proposed system (Conventional voltage latch sense amplifier using MTCMOS technique).

E. Multi Threshold Technique

MTCMOS is a very attractive technique for reducing sub threshold leakage currents during standby modes because existing designs (especially combinational logic blocks) can easily be modified into MTCMOS blocks by simply adding high power supply switches [3]. Furthermore, the processing required providing an extra threshold voltage involves only an additional implant processing step.

MTCMOS is a dual-voltage technology that is very effective at reducing leakage currents in the standby mode [5]. This technique involves using high-voltage transistors to gate the power supplies of a low-voltage logic block [6].When the high- transistors are turned on, the low-voltage logic is connected to virtual ground and power and switching is performed through fast devices.

III. SIMULATION RESULTS & PERFORMANCE EVALUATION

Power is considered as the most important parameter for designing circuits in VLSI. The power consumption of the general and MTCMOS circuits for Conventional Latch Sense Amplifier and Current Mirror Sense Amplifier circuits is considered. So the Proposed Low power Conventional Latch Sense Amplifier designed using MTCMOS technique has an optimized power for various supply voltage.

TABLE I
COMPARISON OF POWER CONSUMED BY VARIOUS DESIGN OF SENSE AMPLIFIER UNDER 30nm TECHNOLOGY

Design/Supply Voltage	**1.05 V**	**2V**	**3V**	**4V**	**5V**
CVLSA	13.6 µw	41.9 µw	76.8 µw	118 µw	418 µw
CMSA	6.84 µw	36.8 µw	74.4 µw	116 µw	159 µw
CMSA MTCMOS	16.8 nw	1.08 µw	3.02 µw	4.89 µw	7.23 µw
CVLSA MTCMOS (PROPOSED DESIGN)	12.1 nw	729 nw	2.74 µw	4.49 µw	6.82 µw

Figure 5: Output waveform of the conventional voltage latch sense amplifier with supply voltage 5V

Figure 5 illustrate the output waveform of the conventional voltage latch sense amplifier with supply voltage 5V and also describe the power consumed by the input and output terminals. The Average power consumed by the design is about is 418µw.

Figure 6: Output waveform of the current mirror sense amplifier with supply voltage 5V

Figure 6 illustrate the output waveform of the current mirror sense amplifier with supply voltage 5V and also describe the power consumed by the input and output terminals. The Average power consumed by the design is about is 159µw.

Figure 7: Output waveform of the current mirror sense amplifier (MTCMOS) with supply voltage 5V.

Figure 7 illustrate the output waveform of the current mirror sense amplifier using MTCMOS technique with supply voltage 5V and also describe the power consumed by the input and output terminals. The Average power consumed by thedesign is about is 7.23µw.

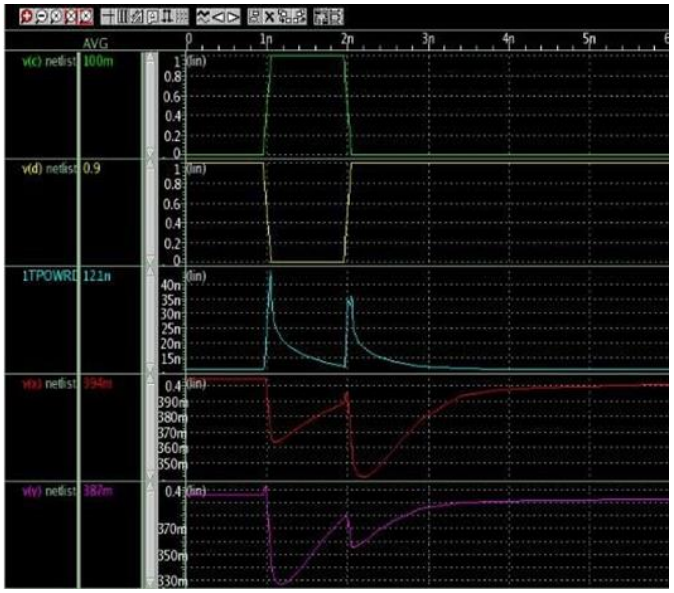

Figure 8 : Output waveform of the PROPOSED SYSTEM (conventional voltage latch sense amplifier-MTCMOS) with supply voltage 5V

Figure 8 illustrate the output waveform of PROPOSED SYSTEM (conventional latch voltage sense amplifier-MTCMOS) with supply voltage 5V and also describe the power consumed by the input and output terminals. The Average power consumed by the design is about is 6.82µw.Where the proposed design holds good power efficiency.

IV. CONCLUSION

The power consumption for conventional voltage latch type sense amplifier, current mirror sense amplifier and the power consumption for the MTCMOS design for the above sense amplifier is been analyzed using 30nm CMOS technology for various supply voltages. While calculating the percentage of power reduction for the supply voltage of 5V for the conventional voltage latch sense amplifier the power is reduced by 89.2% when MTCMOS technique is used in the conventional voltage latch sense amplifier circuit. From that conventional voltage latch sense amplifier designed using MTCMOS technique has optimized power. It can be concluded that conventional voltage latch sense amplifier is suited for low power application.

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