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# A Study on Conventional SRAM and Adiabatic SRAM

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## ABSTRACT

Semiconductor memory is an electronic data storage device, often used as computer memory, implemented on a semiconductor-based integrated circuit. It is made in many different types and technologies. Most modern semiconductor memory devices are implemented allowing random access, which means that it takes the same amount of time to access any memory location, so data can be efficiently accessed in any random order. Static random-access memory (SRAM) is a type of semiconductor memory that uses bistable latching circuitry (flip-flop) to store each bit. It consists of 6 Transistors in the form of cross coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. In CMOS circuits there is short circuit power dissipation so there exist path directly from $V_{DD}$ to ground, hence leading to short circuit current. This drawback can be overcome by adiabatic technique. The tool used to obtain the results is Tanner EDA tool. The power obtained for the conventional SRAM is 2.2mW and for proposed adiabatic technique is 0.3mW

**Keywords: -** Complementary Metal–Oxide–Semiconductor (CMOS), Static Random Access Memory (SRAM).

## I. INTRODUCTION

SRAM exhibits data eminence but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. The term static differentiates SRAM from DRAM (dynamic random-access memory) which must be periodically refreshed. SRAM is faster and more expensive than DRAM; it is typically used for CPU cache while DRAM is used for a computer's main memory. Static Random Access memory (SRAM).Static random access memory (SRAM) is a lot faster and does not require refreshing like dynamic RAM.SRAM is best suited for secondary operations like the CPU's fast cache memory and storing registers. SRAM is most often found in hard drives as disc cache. It is also found in compact discs (CD's), printers, modem routers, digital versatile discs (DVD's) and digital cameras.

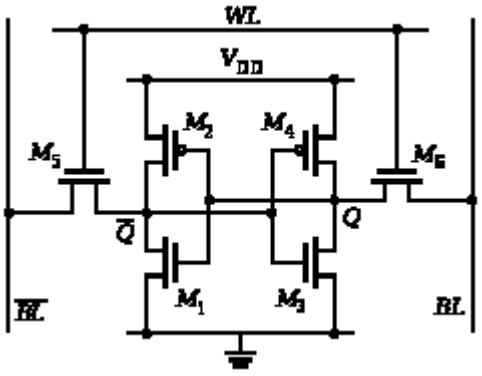



**Figure 1.** Structure of 6-T SRAM Cell

A typical SRAM cell is made up of six MOSFETs as shown in fig 1. Each bit in an SRAM is stored on four transistors (M1, M2, M3, and M4) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write

operations. In addition to such six-transistor (6T) SRAM, other kinds of SRAM chips use 4, 8, 10 (4T, 8T, 10T SRAM), or more transistors per bit. Four-transistor SRAM is quite common in stand-alone SRAM devices which is shown in fig 2 (as opposed to SRAM used for CPU caches), implemented in special processes with an extra layer of poly-silicon, allowing for very high-resistance pull-up resistors. The principal drawback of using 4T SRAM is increased static power due to the constant current flow through one of the pull-down transistors.

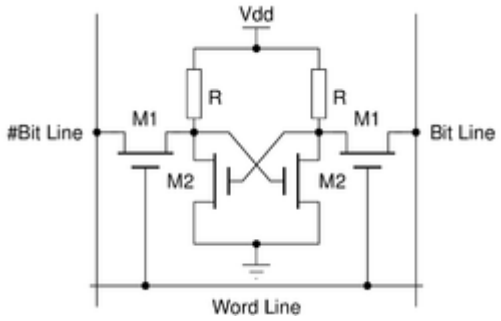



**Figure 2.** 4-T SRAM Cell

Four transistors SRAM provides advantages in density at the cost of manufacturing complexity. The resistors must have small dimensions and large values.

This is sometimes used to implement more than one (read and/or write) port, which may be useful in certain types of video memory and register files implemented with multi-ported SRAM circuitry.

Generally, the fewer transistors needed per cell, the smaller each cell can be. Since the cost of processing silicon wafer is relatively fixed, using smaller cells and so packing more bits on one wafer reduces the cost per bit of memory.

Memory cells that use fewer than four transistors are possible – but, such 3T or 1T cells are DRAM, not SRAM (even the so-called 1T-SRAM). Access to the cell is enabled by the word line (WL in figure) which controls the two access transistors M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BL and BL. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margins. During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell. This improves SRAM bandwidth compared to DRAMs – in a DRAM, the bit line is connected to storage capacitors and charge sharing causes the bit line to swing upwards or downwards. The symmetric structure of SRAMs also allows for differential signaling, which makes small voltage swings more easily detectable. Another difference with DRAM that contributes to making SRAM faster is that commercial chips accept all address bits at a time. By comparison, commodity DRAMs have the address multiplexed in two halves, i.e. higher bits followed by lower bits, over the same package pins in order to keep their size and cost down. The size of an SRAM with m address lines and n data lines is 2m words, or 2m × n bits. The most common word size is 8 bits, meaning that a single byte can be read or written to each of 2m different words within the SRAM chip.

SRAM cell has three different states: standby (the circuit is idle), reading (the data has been requested) or writing (updating the contents). SRAM operating in read mode and write modes should have "readability" and "write stability", respectively. The three different states work as follows:

Standby:- If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross-coupled inverters formed by M1 – M4 will continue to reinforce each other as long as they are connected to the supply.

Reading:-In theory, reading only requires asserting the word line WL and reading the SRAM cell state by a single access transistor and bit line, e.g. M6, BL. Nevertheless bit lines are relatively long and have large parasitic capacitance. To speed-up reading, a more complex process is used in practice:

The read cycle is started by recharging both bit lines BL and BL, i.e. driving the bit lines to a threshold voltage (midrange voltage between logical 1 and 0) by an external module (not shown in the figures). Then asserting the word line WL, enabling both the access transistors M5 and M6 which causes the bit line BL voltage to either slightly drop (bottom NMOS transistor M3 is ON and top PMOS transistor M4 is off) or rise (top PMOS transistor M4 is on). It should be noted that if BL voltage rises, the BL voltage drops, and vice versa. Then the BL and BL lines will have a small voltage difference between them. A sense amplifier will sense which line has the higher voltage and thus determine whether there was 1 or 0 stored. The higher the sensitivity of the sense amplifier, the faster the read operation.

**Writing**

The write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL to 1 and BL to 0. This is similar to applying a reset pulse to an SR-latch, which causes the flip flop to change state. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. This works because the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself so they can easily override the previous state of the cross-coupled inverters. In practice, access NMOS transistors M5 and M6 have to be stronger than either bottom NMOS (M1, M3) or top PMOS (M2, M4) transistors. This is easily obtained as PMOS transistors are much weaker than NMOS when same sized. Consequently when one transistor pair (e.g. M3 and M4) is only slightly overriden by the write process, the opposite transistors pair (M1and M2) gate voltage is also changed. This means that the M1 and M2 transistors can be easier over ridden, and so on. Thus, cross-coupled inverters magnify the writing process.

## II. METHODS AND MATERIAL

**Proposed Adiabatic SRAM Structure and its working**

Adiabatic circuits are low power circuits which use "reversible logic" to conserve energy. Unlike traditional CMOS circuits, which dissipate energy during switching, adiabatic circuits reduce dissipation by following two key rules:

1. Never turn on a transistor when there is a voltage potential between the source and drain.
2. Never turn off a transistor when current is flowing through it.

There are some classical approaches to reduce the dynamic power such as reducing supply voltage, decreasing physical capacitance and reducing switching activity. These techniques are not fit enough to meet today's power requirement. However, most research has focused on building adiabatic logic, which is a promising design for low power applications.

Adiabatic logic works with the concept of switching activities which reduces the power by giving stored energy back to the supply. Thus, the term adiabatic logic is used in low-power VLSI circuits which implements reversible logic. In this, the main design changes are focused in power clock which plays the vital role in the principle of operation. Each phase of the power clock gives user to achieve the two major design rules for the adiabatic circuit design.

- Never turn on a transistor if there is a voltage across it ($VDS > 0$)
- Never turn off a transistor if there is a current through it ($IDS \neq 0$)
- Never pass current through a diode

If these conditions with regard to the inputs, in all the four phases of power clock, recovery phase will restore the energy to the power clock, resulting considerable energy saving. Yet some complexities in adiabatic logic design perpetuate. Two such complexities, for instance, are circuit implementation for time-varying power sources needs to be done and computational implementation by low overhead circuit structures needs to be followed.

There are two big challenges of energy recovering circuits; first, slowness in terms of today's standards, second it requires ~50% of more area than conventional CMOS, and simple circuit designs get complicated.
The basic concepts of adiabatic logic will be introduced. "Adiabatic" is a term of Greek origin that has spent most of its history associated with classical thermodynamics. It refers to a system in which a transition occurs without energy (usually in the form of heat) being either lost to or gained from the system. Etymology of the term "adiabatic logic". Because of the Second Law of Thermodynamics, it is not possible to completely convert energy into useful work. However, the term "Adiabatic Logic" is used to describe logic families that could theoretically operate without losses. The term "Quasi-Adiabatic Logic" is used to describe logic that operates with a lower power than static CMOS logic, but which still has some theoretical non-adiabatic losses. In both cases, the nomenclature is used to indicate that these systems are capable of operating with substantially less power dissipation than traditional static CMOS circuits.

There are several important principles that are shared by all of these low-power adiabatic systems. These include only turning switches on when there is no potential difference across them, only turning switches off when no current is flowing through them, and using a power supply that is capable of recovering or recycling energy in the form of electric charge. To achieve this, in general, the power supplies of adiabatic logic circuits have used constant current charging (or an approximation thereto), in contrast to more traditional non-adiabatic systems that have generally used constant voltage charging from a fixed-voltage power supply.

The power supplies of adiabatic logic circuits have also used circuit elements capable of storing energy. This is often done using inductors, which store the energy by converting it to magnetic flux. There are a number of synonyms that have been used by other authors to refer to adiabatic logic type systems, these include: "Charge recovery logic", "Charge recycling logic", "Clock-powered logic", "Energy recovery logic" and "Energy recycling logic". Because of the reversibility requirements for a system to be fully adiabatic, most of these synonyms actually refer to, and can be used inter-changeably, to describe quasi-adiabatic systems. These terms are succinct and self-explanatory, so the only term that warrants further explanation is "Clock-Powered Logic". This has been used because many adiabatic circuits use a combined power supply and clock, or a "power-clock". This variable, usually multi-phase, power-supply which controls the operation of the logic by supplying energy to it, and subsequently recovering energy from it.

Because high-Q inductors are not available in CMOS, inductors must be off-chip, so adiabatic switching with inductors are limited to designs which use only a few inductors. Quasi-adiabatic stepwise charging avoids inductors entirely by storing recovered energy in capacitors. Stepwise charging (SWC) can use on-chip capacitors.

In this adiabatic circuit one can ensure that both the bit lines are charged to the same voltages before reading. The various steps involved in writing, reading and hold operations in the new circuit. In both the conventional SRAM and the proposed adiabatic SRAM, the data which has to be written is first obtained with its complement using two inverting buffers as shown in Fig.3

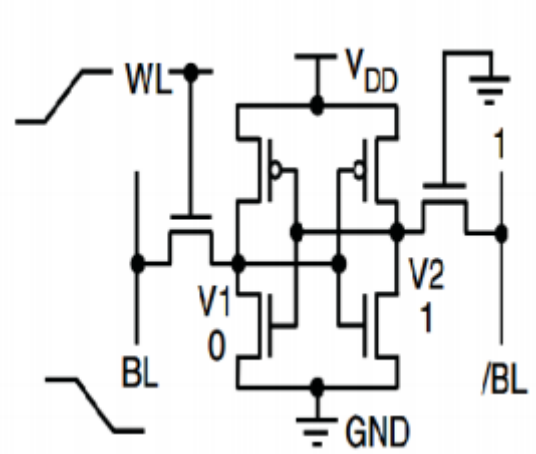



**Figure 3.** Adiabatic 6 Transistor SRAM Structure

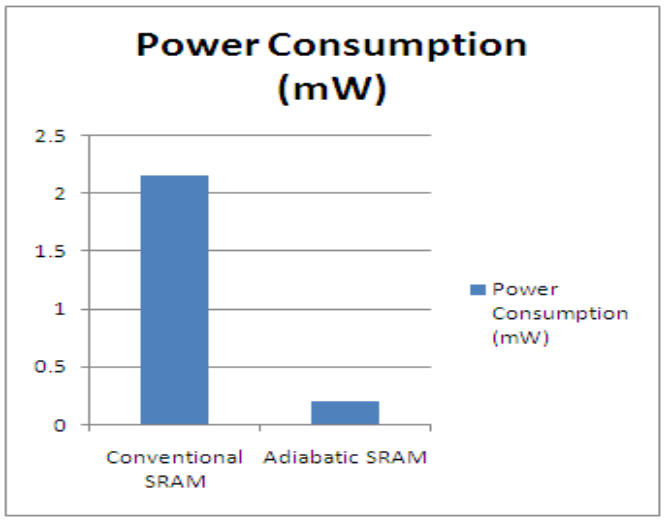
A low power RAM device including a bit line pre charge circuit which selectively pre charges only those bit lines which will be read in an effort to minimize pre charge and overall RAM power consumption. The preferred RAM pre charge circuit uses a pre charge device in the sense amplifier as the primary bit line pre charge device to selectively connect and pre charge the selected bit line through a column MUX. The preferred RAM pre charge also includes secondary bit line pre charge devices for each bit line to enable trickle charging thereof to prevent hazardous RAM data corruption. Since RAM corruption occurs only after

several clock cycles, the secondary pre charge devices comprise small transistors having only 1/20 the size of normal pre charge device to conserve pre charge power requirements.

The RAM device includes a carefully controlled timing sequence of pre charge signal, column-select signals, and word-line signals, to selective pre charge the selected bit line and to remove the hazardous power consuming DC current path to further reduce power consumption.

## III. RESULTS AND DISCUSSION

Simulation of conventional 6-T SRAM and adiabatic 6-T SRAM are done using Tanner software and power analysis are obtained and the comparison between both the structures are shown below




## IV. CONCLUSION

In this paper 6T conventional SRAM and 6T adiabatic SRAM technique are simulated. Simulation has been done using 180nm CMOS technology. Different operations of conventional and adiabatic have been studied. Using adiabatic technique, average power dissipation is reduced up to 89% during write operation, power dissipation is reduced up to 65% during write and hold operation and power dissipation is reduced up to 87% during write and read operation. On the other hand, average power dissipation is reduced up to 55% during write operation, power dissipation is reduced to 9% during write and hold operation and power dissipation is reduced up to 43% during write and read operation. The power comparison between conventional SRAM and Conventional SRAM is shown below is shown below.

**Table 1.** Power Comparison

| Parameter | Conventional SRAM | Adiabatic SRAM |
|---|---|---|
| Power(mW) | 2.2 | 0.3 |

The simulation results show that there is a significant reduction in power in adiabatic logic. The same Adiabatic 6 Transistor logic can be implemented in memristor technology, thereby reducing the power consumption.

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