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Design of Delay Lock Loop with Dual Control Using LT-Spice

K. Ragupathi, J. Imran Khan, M. Karthik, S. Rajan, D. Vignesh Kumar
Department of ECE, Velammal Institute of Technology, Chennai, Tamilnadu, India

ABSTRACT

The paper presents "A CMOS Delay Lock Loop with Dual Control". Positron emission tomography (PET) with time-of-flight (TOF) capability has been shown to provide a better reconstructed image compared to conventional positron tomography. Resolution is the biggest problem in PET. To achieve such resolution, time interpolations and multiphase sampling techniques are the mostly used methods. A precise multiphase clock generator should be required. Generally, the timing generator is realized by using a delay-locked loop (DLL) due to its good performances on low jitter and easier integration implemented in CMOS process.
Keywords: CMOS, time-of-flight, delay-locked loop, Positron emission tomography, CDR, VCDL, LPF

I. INTRODUCTION

In electronics, a **delay-locked loop** (DLL) is a digital circuit similar to a phase-locked loop (PLL), with the main difference being the absence of an internal voltage-controlled oscillator. A DLL can be used to change the phase of a clock signal (a signal with a periodic waveform), and usually to enhance the clock rise-to-data output valid timing characteristics of integrated circuits (such as DRAM devices). DLLs can also be used for clock recovery (CDR). From the outside, a DLL can be seen as a negative-delay gate placed in the clock path of a digital circuit. DLLs are negative feedback control systems that try to adjust the propagation delay of an internal circuit so that it matches the period of a reference signal.

DLLs should be integrated with digital circuits on a single chip for portable devices. All battery-powered devices are now being designed to include low-power techniques to prolong the battery life. Similarly, DLLs need low-power architecture or a low-power technique. Low-voltage operation is one of the difficult challenges in the mixed-signal Ics. The down-scaling of the minimum channel length to 0.65 nm results in the reduction of the power supply voltage to 0.7 V.

Motivation

The main motivation for this project is to design a DLL that will allow on-chip direct digitization of a wideband RF signal. We also want to replace analog designs with full-digital implementations. To do this, a suitable DLLs architecture, concentrating on low jitter and power, for the complete SoC should be devised.

To increase the accuracy and reduce power consumption, both phase-locked loops (PLLs) and Delay locked loops (DLLs) are used in many timing circuits. When either a DLL or a PLL can be used, a DLL is always preferred in many cases because of its better stability and faster locking time compared to a PLL. Therefore, in our research, we have identified that the best circuit to generate stable time delays on chip is a DLL. A DLL is widely used as a timing circuit in many systems for the purpose of clock generation, signal synchronization, and others.

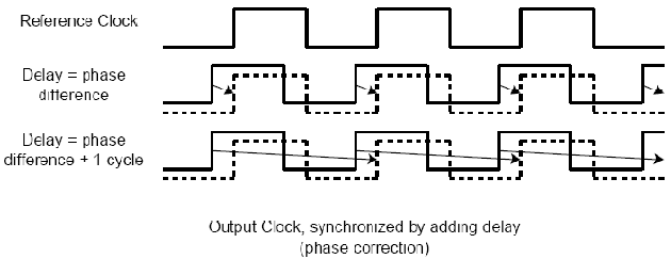

Figure 1: Dll timing

II. METHODS AND MATERIAL

A. CMOS DLL

A delay-locked loop (DLL) is a digital circuit similar to a phase-locked loop (PLL), with the main difference

being the presence of a voltage controlled delay line in place of voltage controlled oscillator. The primary function of a DLL is to achieve phase alignment between the input clock and the output clock from the final stage of the VCDL. When the phase alignment is achieved, each VCDL delay stage is able to provide a stable clock signal which is phase shifted from the input clock. However, the rising clock speeds and integration levels of digital circuits have made the phase alignment task increasingly difficult [4].

The application areas of DLL include clock distribution, clock synthesis, memory, microprocessors, clock and data recovery, and communication ICs in order to reduce on chip clock buffering delays and improve I/O timing margins. They can also be used to generate multiple clock signals on chip for applications such as for Built in Self-Test (BIST) circuits. Thus, a thorough study of previous work in DLL design and analysis is required to accomplish the design goals of wide lock range, less static error, and fast locking. In the subsequent sections of this chapter different architecture of DLL design, operating principle, closed loop dynamics and analysis is shown in an elaborated manner.

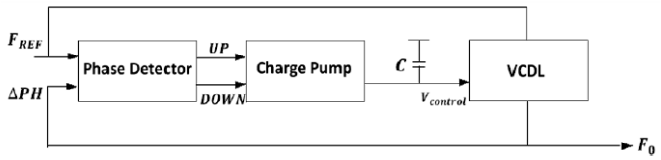

Figure 2: Block Diagram

B. PERFORMANCE PARAMETERS OF DLL

The DLL performance basically depends on some of the parameters evaluation and these parameters are explained below in brief.

STATIC PHASE ERROR

Static phase error refers to the phase difference between the output signals of the last stage of the VCDL and the input reference signal. In the ideal case, after a DLL is locked, the phases of these two signals should be perfectly matched. However, due to the limited resolution of the PD and CP some static phase error may exist.

LOCK TIME

Locking time refers to the time interval a DLL takes to achieve a stable locking state from an initial state. Generally, locking time is related to the speed of the PD, the magnitude of the charging or discharging current in the CP, and the overall delay loop bandwidth.

LOCK RANGE

Lock range refers to the frequency range in which a DLL is able to achieve lock. Although it is often desired to have lock range as wide as possible, the lock range of a particular DLL is usually designed for a specific application.

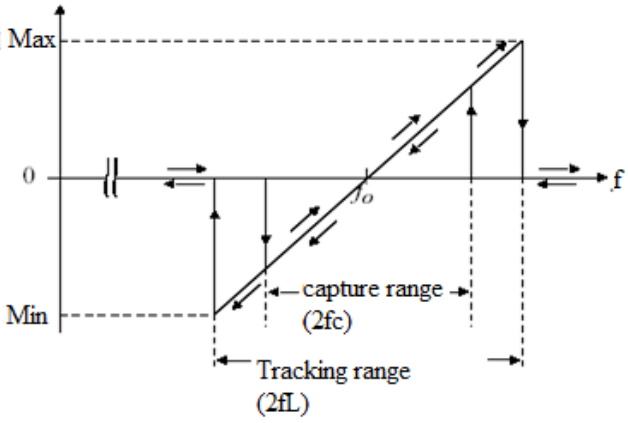

Figure 3: Tracking Characteristics

C. INTEGRATED DLL

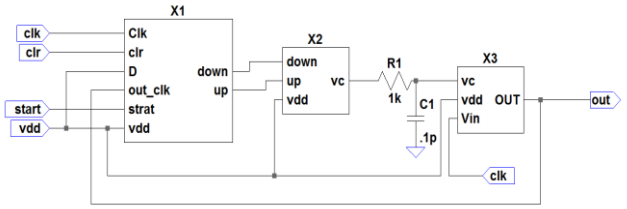

Figure 4: main block diagram

i. Start Control PFD

The proposed start-controlled circuit and the proposed PFD comprise one resettable dynamic DFF and two NAND-resettable dynamic DFFs, respectively. Compared to [13], the MR0 of Figure 3.5 (a) is added to make the DFF resettable and the MR0–MR3 of Figure 3.5 (b) are added to make it NAND-resettable. Figure 3.5 (b) shows how an inverter chain is used to eliminate the low gain region near delay locked. The inverter chain is composed of three cascaded inverters. Eliminating the dead zone is accomplished by producing an "up" current pulse and a "down" current pulse during each cycle. Therefore, both currents have an equal amplitude and duration, and the net effect on the output

voltage of the charge pump circuit is zero [14], [15]. This design reduces the number of transistors in the proposed start-controlled PFD circuit from 120 to 52, and the gate delay of the reset path is also reduced from 9 to 5.

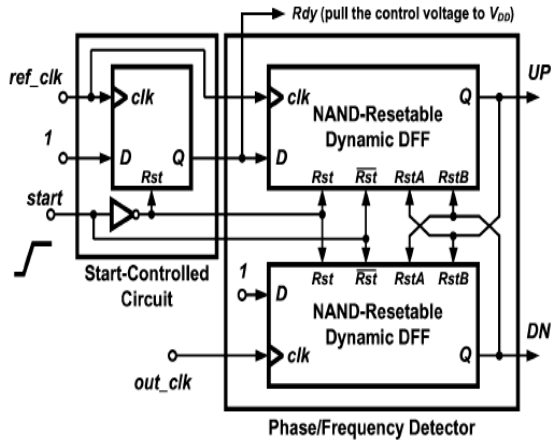

Figure 5: Block Diagram of Start Control PFD

ii. Charge Pump

A charge pump consists of two switched current sources that pump charge into or out according to two logical inputs Architecture consist of current generator and charge pump circuit.

Reference current is generated by external resistor and transferred by a high output impedance current mirror. Feedback circuit is added to minimize the mismatch problem

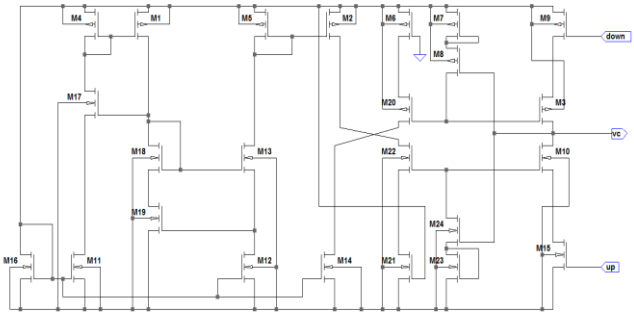

Figure 6: Charge Pump Architecture

iii. Low Pass Filter

It is a normal RC filter. It reduces unwanted glitches from the circuit.

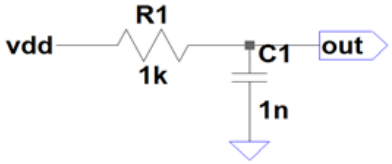

Figure 7: RC Filter

iv. Voltage Control Delay Line

The Voltage controlled Delay Line is made up of two current starved inverters. Addition with the biasing circuits is used to bias the VCDL. Bias circuit is used to give constant current depending on $V_{control}$Bias circuit is also used to make the system stable.

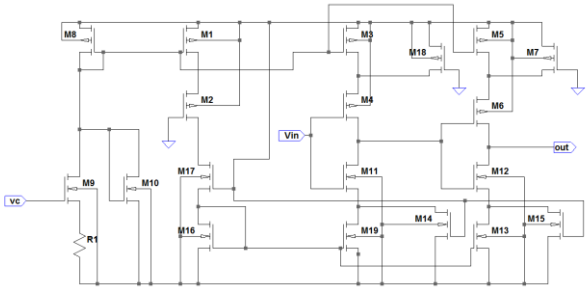

Figure 8: VCDL Architecture

III. RESULTS AND DISCUSSION

A. Simulation of Start control Phase and Frequency Detector

The simulated output of the Phase Frequency Detector (PFD) is shown in the figure. The first component in our DLL is the phase and frequency detector. The output of the PFD depends on both the phase and frequency of the inputs. This type of phase detector is also termed a sequential phase detector.

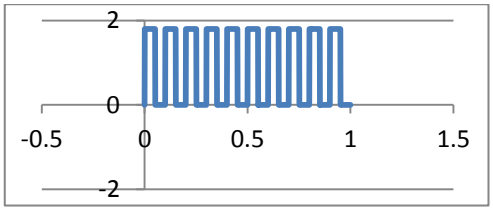

Figure 9.1: Input of phase detector

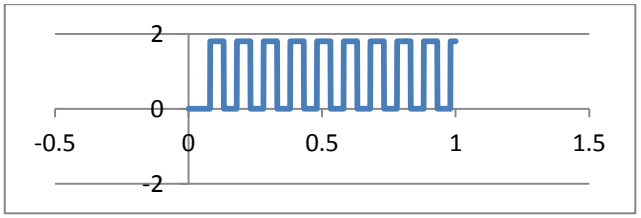

Figure 9.2: Delayed Input of phase detector

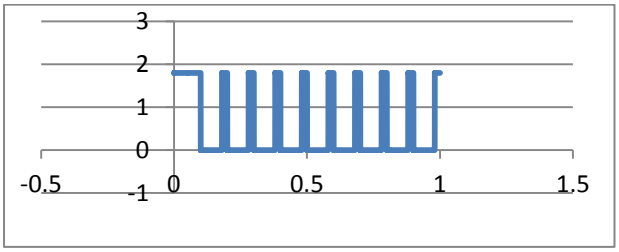

Figure 9.3: Phase up Detector Output

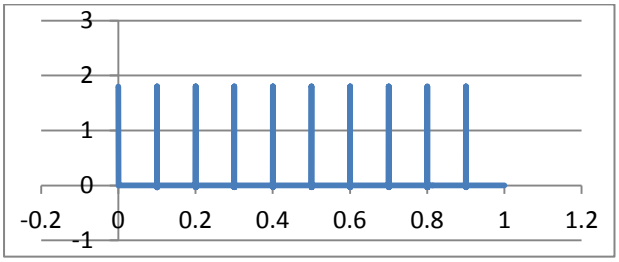

Figure 9.4: Phase down Detector Output

B. Simulation of Charge Pump

Charge pump consists of two PMOS and two NMOS, which are connected serially. Both of the NMOS are in the pull down section and both of the PMOS are in the pull up section. The gate of uppermost PMOS is connected to GND. The gate of lowermost NMOS is connected to VDD. The gates of the remaining NMOS and PMOS are connected to the "DOWN" pin and "UP" pin of the output of PFD

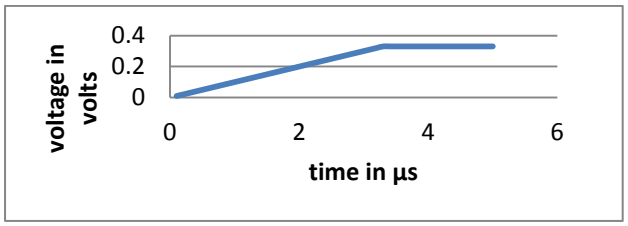

Figure 9.5: Charge Pump Output

The above diagram shows the output of the charge pump. The inputs to the CP are UP and DOWN value. Depending on the UP and DOWN value CP will decide to increase the control voltage of VCDL or to decrease the control voltage of VCDL. In the graph condition, VCDL value is leading so the output is to decrease the voltage of VCDL.

C. Simulation of Low Pass Filter

In low pass filter the resistance and capacitance are connected in parallel, which is used to reduce the noise in the output. Output of the charge pump is given as the input for low pass filter. And the output of the low pass filter is given as input to VCDL

(a)-Input of Low pass filter.

(b)-Output of Low pass filter

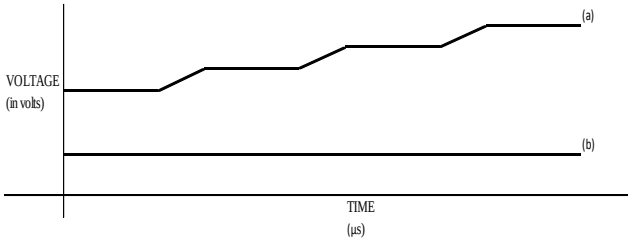

Figure 9.6: Low Pass Filter Output

The above graph is the output of Low pass filter. Here the input to the LPF is Charge pump output. LPF will neglect the high pass signals from the charge pump and send low pass signals to the VCO.

D. Simulation of Voltage Controlled Delay Line

The Voltage controlled Delay Line is made of series of Current starved inverters Current starving the inverter with additional transistor based loads in the paths towards Vdd and Gnd, it is possible to vary the delay by biasing the transistors M13, M14 and M15. This delay stage is built with a Current starved inverter (buffer) topology. In order to minimize the sensitivity to supply and substrate noise and to achieve a wide tuning range, the delay stage in is used in the proposed DLL. In the DLL clock generator, the accuracy of the generated setup clock and hold clock signals relies on the matching between the delay stages.

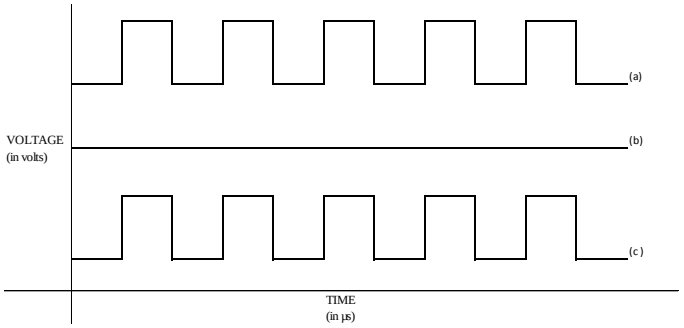

Figure 9.7: VCDL Output

E. Simulation of Delay Lock Loop

The charge pump output is given to VCDL; the output clock pulse varies along with frequency due to delay element in VCDL circuit.

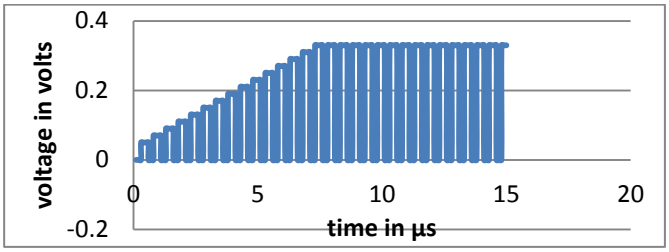

Figure 9.8: DLL Output

Output from the charge pump is given as control voltage to the VCDL. Control voltage is used to control the differences between the input and output of the Delay locked loop. The output is gradually increases and stable at one state, that particular state is called lock in range.

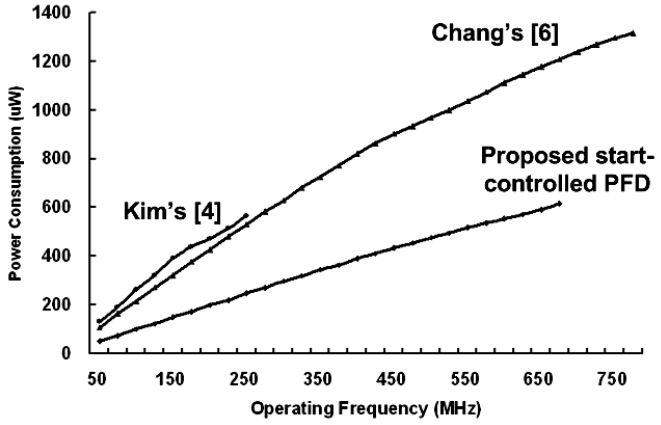

Figure 10: Power Consumption and Speed Comparison

IV. CONCLUSION

In this paper, the new architecture of a timing generator has been designed. With the aid of Single DLLs, the timing generator can provide precise sub-gate resolution with close-loop delay control and instantaneous switching capability. This circuit is implemented and simulated using LT-SPICE. The main advantage of this DLL is Phase and Frequency Detector using TANNER implementation which reduces the power consumption due to reduced transistors. And the operating frequency is also increased with synchronous structure and single loop cycle. A conventional single loop design of a Low Power CMOS Delay Locked Loop with lowest power consumption has been implemented. Various circuit and architecture parameter trade-offs are evaluated. This new architecture output performs comparable designs in performance of the parameters. This architecture has a large degree of flexibility in design. The simulation results show that the Low Power CMOS Delay Locked Loop is preferable for the next generation deep sub-micron low voltage CMOS DLL. In future dual delay locked loop will be proposed and simulated with layout implementation

V. ACKNOWLEDGEMENT

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