© 2017 IJSRSET | Volume 3 | Issue 3| Print ISSN: 2395-1990 | Online ISSN : 2394-4099
Themed Section: Engineering and Technology

Design and Analysis of Johnson Counter Based on DFAL Technique

Veena Battula,Vishal Moyal
Department of Electronics & Telecommunication, Shri Shankaracharya Technical Campus, SSITM, Bhilai, India

ABSTRACT

In VLSI design, low power dissipation and high speed are the prime concern now a days. This paper presents a diode free adiabatic logic (DFAL) based Johnson Counter. The performance parameters in terms of power dissipation, time delay and PDP of the DFAL based circuit are compared with its conventional CMOS counterpart which shows improved performance, without adding circuit complexity and energy saving upto 30% is achieved. The design has been carried out on CADENCE VIRTUOSO SPECTRE simulator and is implemented at 90nm CMOS technology.

Keywords: DFAL, Johnson Counter, CADENCE VIRTUOSO, CMOS

I. INTRODUCTION

In recent times, researchers have focused on high speed and low power consumption in order to enhance the performance of digital devices; hence, it has become important to design digital circuits in order to achieve high energy efficiency.In digital circuit, counters and registers are the main sequential circuits that are used frequently. Sequential circuits are basically combinational circuits with memory. In the digital systems, different data sequences are generated by different counters.

A Johnson counter is one of the type of counter, which will generate a particular data sequence.Inorder to design low power sequential circuits, it involves use of minimum CMOS logic gates,hence by avoiding unnecessary clock pulse[1].

In conventional CMOS circuit,the power consumption is proportional to the square of the voltage being supplied; therefore,voltage scaling is used to minimize power consumption and thereby improving the circuit performance. However, on scaling down the transistor threshold voltage V_t results in the subthreshold leakage current to rise [2,3].

Thus the capacitive load can be minimized but driving ability of the circuit can be affected[4].From the above limitations,adiabatic logic circuits have been introduced for power saving. Several adiabatic logic are being considered for power efficient circuit[5-9].

The adiabatic technique reduces energy being dissipated through PMOS transistor during charging phase and during the discharging phase it reuses energy which is stored in the capacitive load. The challenges involved in the previous adiabatic families has been explained and their solution is suggested through diode free adiabatic logic (DFAL) circuit[10],which provides low power dissipation.

This paper presents a new design for Johnson counter which is constructed by using D flip-flop with the help of DFAL technique[11] which is more energy efficient than conventional CMOS circuit.

The paper is organized as follows : Section II include discussion of conventional Johnson counter.Section III include the logic of the DFAL based Johnson counter.Section IV shows illustration of simulation results of the proposed circuits alongwith their comparison.Section V draws conclusion.

II. JOHNSON COUNTER

In digital design, counter is designed through a number of flip-flops connected in cascade. In digital circuit, counters are usually used, it is a sequential circuit. Counter is a device which is used for a counting pulses in the digital circuit. It is a group of flip-flops with a clock signal applied. Johnson counter well known as twisted ring counter or modified ring counter.

Figure 1 shows the conventional Johnson counter. Johnson counter is a type of counter where complemented output of the last stage D flip-flop is given back to the input of the first stage D flip-flop.

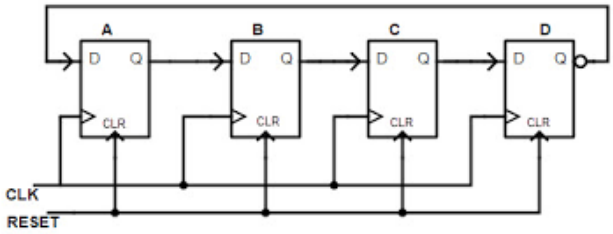

Figure 1: Conventional Johnson Counter

A. Working of Johnson Counter

Initially all the flip flops are set to 0(i.e.clear), so that the complemented output of last flip flop is high i.e. 1.This high logic is fed back to the input of 1st flip-flop. When the first clock pulse is applied to the 1st flip-flop, this logic 1 is transferred to its output. Thus the overall output of Johnson counter is 1000.

This high logic 1 appears at the input of the 1st and 2nd flip-flop and when the second clock pulse is applied, these inputs appear at the outputs of 1st and 2nd flip flop. So that the overall output is 1100. Again,high logic 1 appearing at the input of 1st, 2nd and 3rd flip-flop and when the third clock pulse is applied to the 3rd flip-flop these inputs appear at the outputs of 1st, 2nd and 3rd flip flop. So that the overall output is 1110.

Similarly for the next clock pulse, the overall output will be 1111.During this state, the complemented output of the last flip-flop is logic 0. This logic 0 is fed back to the 1st flip flop. Then the logic 0 will get circulate throughout the flip-flops as 0111,0011,0001,0000 as discussed for high logic 1.

Table 1. Truth Table for Johnson Counter

Q_A	Q_B	Q_C	Q_D	STATES
0	0	0	0	STATE0
1	0	0	0	STATE1
1	1	0	0	STATE2
1	1	1	0	STATE3
1	1	1	1	STATE4
0	1	1	1	STATE5
0	0	1	1	STATE6
0	0	0	1	STATE7

After state 5, the circuit goes to state 0 and this will repeat. So to design Johnson counter, cascade connection of D flip-flop is required, which is described in the next section.

III. PROPOSED JOHNSON COUNTER

A new design for Johnson counter has been suggested using DFAL technique. In this, DFAL based D flip-flop is designed which is then used in Johnson counter.

A. Proposed D flip-flop

The proposed D flip-flop is designed by using inverter based on DFAL technique. The proposed inverter is connected in the form of a loop.D flip-flop is a circuit in which output signal follows input signal till clock pulse is high otherwise output signal follows the previous state when the clock pulse is low. D flip-flop is constructed by connecting inverters in the form of a loop. Schematic diagram of DFAL based D flip-flop is shown below.

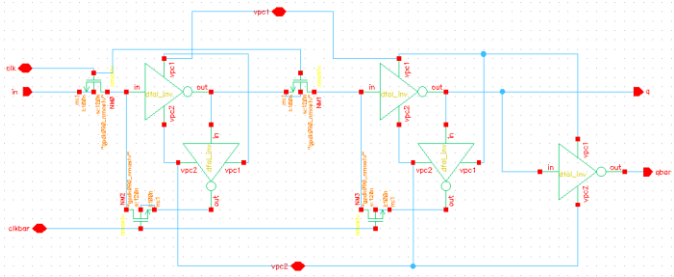

Figure 2: Schematic diagram of DFAL based D Flip-flop

B. Proposed Johnson Counter:

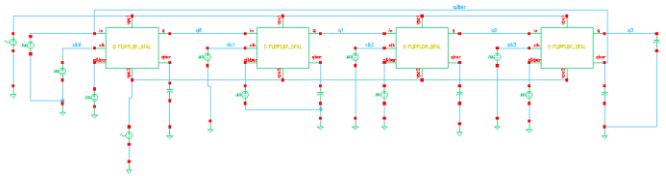

Figure 3: Schematic diagram of DFAL based Johnson counter

In the proposed Johnson counter, DFAL based D flip-flop is connected in cascade,the inverted output of the last flip-flop is given back to the input of the first flip-flop. Schematic diagram of DFAL based Johnson counter is shown in figure 3.

IV. SIMULATION RESULTS

The Proposed Johnson counter has been simulated in CADENCE VIRTUOSO SPECTRE simulator at 90nm CMOS Technology at a supply voltage of 3V. Following is the simulation result of the DFAL based Johnson Counter.

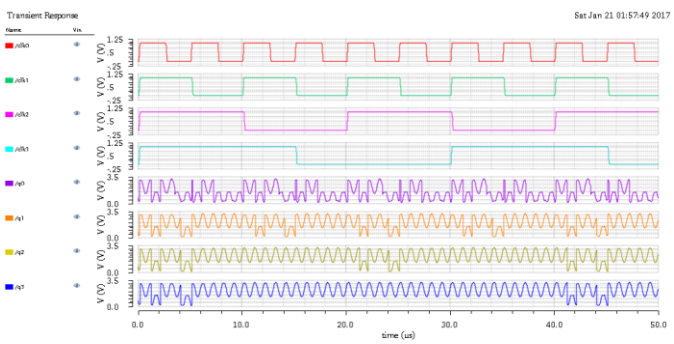

Figure 4: Simulation result of DFAL based Johnson Counter

A. Power dissipation and Delay with varying Load Capacitance

The input frequency and clock frequency are kept constant at 100MHz and 200MHz respectively. Further capacitive load has been added one by one at the output node from 18fF to 35fF to justify the driving ability of the proposed counter against the conventional Johnson counter.

Then, the power and delay are calculated for 10 clock cycles of charging and discharging and are shown in table 2.

Initially delay in the proposed Johnson counter is larger than the conventional. But as the frequency reaches 50MHz the difference between their delay is reduced.

Thus from the above analysis it can be estimated that both power and delay is improved thus overall performance parameter including PDP is improved in comparison to conventional Johnson counter.

B. Power dissipation and Delay with varying Frequency

To justify the performance of the proposed counter, both the proposed DFAL based counter and the conventional counter has been simulated and their performance parameter are calculated and compared with changing frequency.

The input frequency and clock frequency are varied simultaneously from 50MHZ to 100MHz and the load capacitance is stable at 20fF.The power dissipation and delay are calculated for 10 clock cycles of charging and discharging and are shown in table 3.

It may be observed that at 20fF capacitive load the delay is larger in conventional Johnson counter than proposed design at input frequency 50MHz but as the frequency reaches to 100MHz the power dissipation as well as delay decreases, which estimates that DFAL based Johnson counter is efficient than the conventional design.

The performance parameter such as energy saving and adiabatic gain is calculated for both conventional and proposed Johnson counter, is presented in the tabular form.

The overall performance of the CMOS based Johnson counter and proposed Johnson counter as shown in figure 5 and 6 with varying load capacitance and frequency respectively.

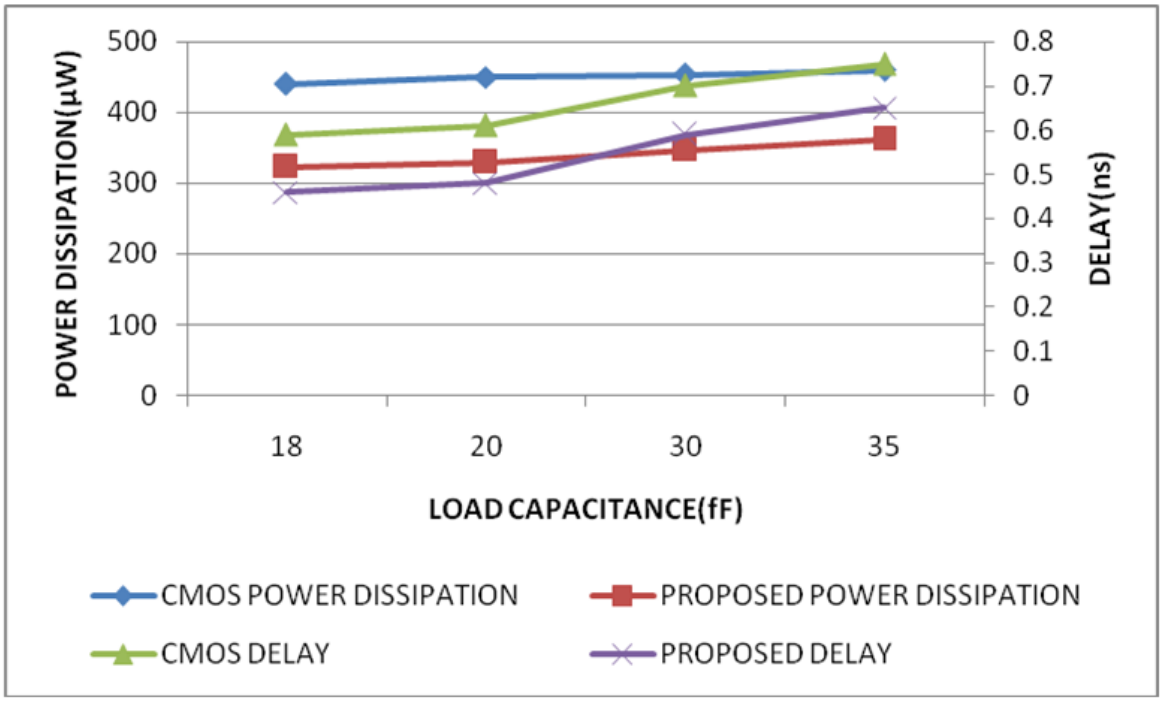

Figure 5: Power dissipation and delay of Johnson Counter with load capacitance

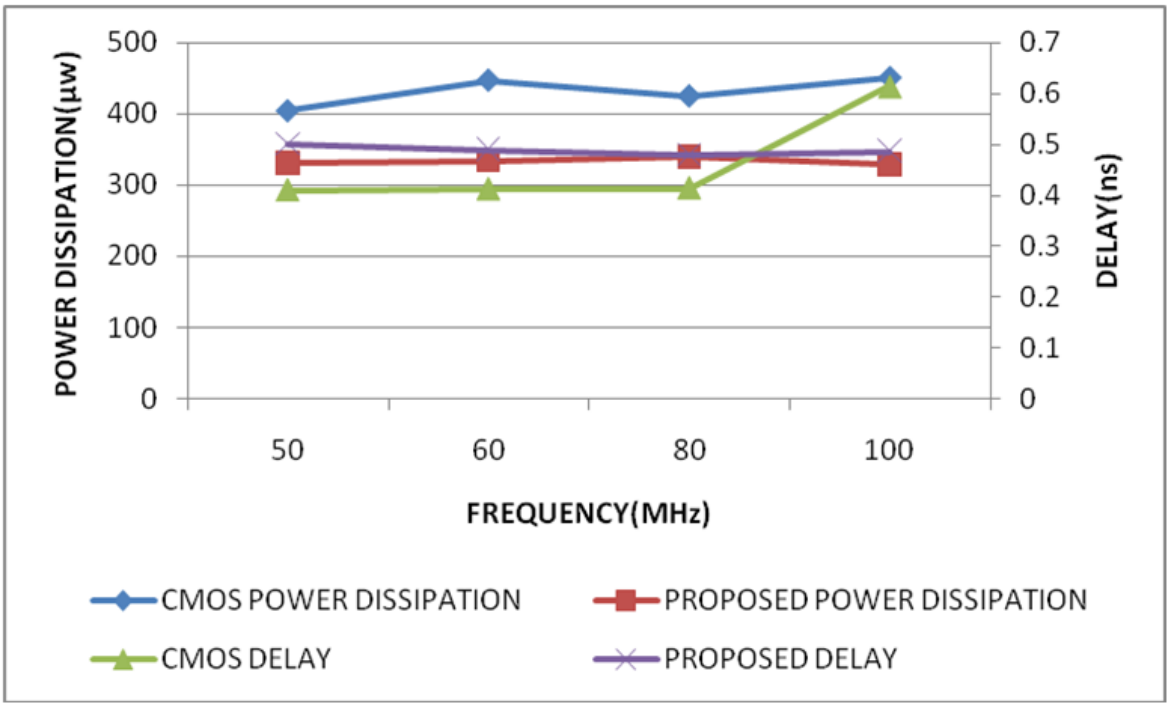

Figure 6: Power dissipation and delay of Johnson Counter with frequency

Table.2. Comparison of Power Dissipation, Delay and Power Delay Product (PDP) with varying load capacitance at input frequency= 100MHz and clock frequency= 200 MHz in 10 clock cycles of charging and discharging

Johnson Counter	18fF	20Ff	30fF	35Ff
Power Dissipation (μW)				
Conventional	439.8	450.3	453.3	459.3
Proposed	322.3	329.2	346.2	362.4
Delay (ns)				
Conventional	0.59	0.61	0.7	0.75
Proposed	0.46	0.48	0.59	0.65
PDP (fJ)				
Conventional	259.4	274.68	317.3	344.4
Proposed	148.2	158.01	204.2	235.5
Adiabatic Gain				
	1.75	1.73	1.55	1.46
Energy Saving(%)				
	42.8	42.4	35.6	31.6

Table.3. Comparisonof Power Dissipation, Delay and Power Delay Product (PDP)with varying frequency at 20fF in 10 clock cycles of charging and discharging

Johnson Counter	50MHz	60MHz	80MHz	100MHz
Power Dissipation (μW)				
Conventional	403.9	446.8	424.7	450.3
Proposed	330.7	334.7	340.2	329.2
Delay (ns)				
Conventional	0.41	0.412	0.413	0.614
Proposed	0.5	0.49	0.48	0.48
PDP (fJ)				
Conventional	165.599	184.08	175.40	276.4
Proposed	165.35	164.003	163.296	158.01
Adiabatic Gain				
	1.00	1.12	1.07	1.74
Energy Saving(%)				
	42.8	10.9	6.9	42.8

V. CONCLUSION

This paper presents a DFAL based Johnson counter. The analysis of both the proposed Johnson counterand conventional design has been done. The performance of the proposed Johnson counter is more power efficient than the conventional design. Also, the delay and PDP of the proposed comparator are considerably lower as compared to the conventional design.

VI.REFERENCES

[1] BhimaVenkataSujatha and V.T. Venkateswarlu, "An Efficient Design for Reduction of Power Dissipation in Johnson Counter using Clock Gating", International Journal of Science and Research (IJSR), Volume 4 Issue 1, January 2015.

[2] D. A. Hodges, H. G. Jackson, and R. A. Saleh, "Analysis and Design of Digital Integrated Circuits", McGraw-Hill, New York,NY, USA, 3rd edition, 2003.

[3] N. H. E. Weste and D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", Addison-Wesley, Reading, Mass, USA,3rd edition, 2004.

[4] K. V. De and D. J. Meindl, "Opportunities for non-dissipative computation," in Proceedings of the 9th Annual IEEE International ASIC Conference and Exhibit, pp. 297–300, Rochester,NY,USA, September 1996.

[5] A.Vetuli,S.DiPascoli, and L.M. Reyneri,"Positive Feedback in adiabatic logic",Electronics Letters,Vol.32 Issue 20,pp.1867-1869,September 1996.

[6] Y. Moon and D. K. Jeong, "An efficient charge recovery logic circuit",IEEE Journal of solid-state circuits,vol.31 Issue 4,pp.514-522,April 1996.

[7] N.SivSankaraReddy,M.SatyamandK.LalKishore,"Glitch free and Cascadable Adiabatic Logic for Low Power Applications",Adiabatic Logic for Low Power Applications Asian Journal of Scientific Research , Vol. 1 ,Issue 4, pp. 464-469 ,2008.

[8] A. Kramer, J.S. Denker, B. Flower and J. Moroney, "2nd order adiabatic computation with 2N-2P and 2N-2N2P logic circuits", in proceedings of International Symposium on low power Design,pp 191-196,1995.

[9] Shipra Upadhyay, R. A. Mishra, R. K. Nagaria, and S. P. Singh,"Low-Power Adiabatic Computing with Improved Quasistatic Energy Recovery Logic" Vol.2013, Article No. 15 January 2013.

[10] Shipra Upadhyay, R. A. Mishra, R. K. Nagaria, and S. P. Singh, "DFAL: Diode-Free Adiabatic Logic Circuits", Hindawi Publishing Corporation ISRN Electronics Volume2013, Article ID 673601, December 2012.

[11] Veena Battula, Vishal Moyal, "Low Power Dissipation in Johnson Counter using DFAL Technique", January 17 Volume 5 Issue 1 , International Journal on Recent and Innovation Trends in Computing and Communication (IJRITCC), ISSN: 2321-8169, PP: 244 – 247.