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Evolution of Multigate MOSFETs

Sushmita Jaiswal[1], Dr. Sarvesh Dubey[2]

[1]Department of Electronics and Communication Engineering, ShriRamswaroop Memorial University (SRMU, UGC Affiliated), Lucknow

[2]Associate Professor Electronics and Communication Engineering, ShriRamswaroop Memorial University (SRMU, UGC Affiliated), Lucknow

ABSTRACT

Undoped cylindrical gate all around (GAA) MOSFET is a radical invention and a potential candidate to replace conventional MOSFET, as it introduces new direction for transistor scaling. In this work, the sensitivity of process parameters like channel length (Lg), channel thickness (t_{Si}), and gate work function (φ_M) on various performance metrics of an undoped cylindrical GAA to nanowire MOSFET are systematically analyzed. The electrical characteristics such as on current (I_{on}), subthreshold leakage current (I_{off}), threshold voltage (V_{th}) and similarly analog/RF performances like transconductance (g_m), total gate capacitance (C_{gg}), and cut-off frequency (f_T) are evaluated and studied with the variation of device design parameters. The discussion give direction towards low standby operating power (LSTP) devices as improvement in I_{off} is approaching 90% in nanowire MOSFET. All the device performances of undoped GAA MOSFET are investigated through Sentaurus device simulator from Synopsis Inc.This paper presents the various device structure of MOSFETs like SOI-MOSFET, Double gate Mosfet, Trigate mosfet, Multigate mosfet ,Nanowire Mosfets,High -K Mosfets& their deserves. To grasp during a easy means , mathematical ideas of device physics skipped

Keywords : SINGLE-GATE- SOI MOSFET, DOUBLE-GATE SOI MOSFETs, GAA, FinFETs.

I. INTRODUCTION

To get low cost, high operational speed and better performance, the dimension of the conventional transistors need to be downscaled to sub-nanometer region. The reduction of MOSFET dimensions will degrade the gate control over the channel due to the close proximity between the source and drain. This leads to increase various short channel effects (SCEs) like hot carrier effect, threshold voltage roll-off, and substrate bias effect [1], [2]. Many new devices have been introduced in beyond Moore's era [3]–[5] to suppress the SCEs and enable further scaling down the device. Similarly, some multi-gate silicon on insulator (SOI) technology has also been proposed to replace the conventional Over the past decades, the Metal Oxide Semiconductor (MOSFET) has repeatedly been scaled down in size[1]; classic MOSFET channel lengths were once manymicrometers, however fashionable integrated circuits square measure incorporating MOSFETs with channel lengths of tens of nanometers. Henry Martyn Robert Dennard's work on scaling theory was polar in recognizing that this in progress reduction was potential. Intel began production of a method that includes a thirty two nm feature size (with the channel being even shorter) in late 2009. The semiconductor trade maintains a "roadmap", the ITRS,[2] that sets the pace for MOSFET development. Historically, the difficulties with decreasing the scale of the MOSFET . Are related to the semiconductor fabrication method, the necessity to use terribly low voltages, and with poorer electrical performance necessitating circuit planand innovation.

II. SINGLE-GATE SOI MOSFETs

Figure 2 shows the "Family Tree" of SOI MOSFETs and shows the evolution from partially depleted, single-gate devices to multi-gate, fully depleted structures. Partially depleted silicon MOSFETs are the successors of earlier SOS (Silicon-On-Sapphire) devices. PDSOI MOSFETs were first used for niche applications such as radiation-hardened or high temperature electronics. At the turn of the century PDSOI technology became mainstream as major semiconductor manufacturers started to use it to fabricate high-performance microprocessors. The low-voltage performance of

PDSOI devices can be enhanced by creating a contact between the gate electrode and the floating body of the device. Such a contact improves the subthreshold slope, body factor and current drive, but limits the device operation to sub-1V supply voltages. [15-23] Fully depleted SOI devices have a better electrostatic coupling between the gate and the channel. This results in a better linearity, subthreshold slope, body coefficient and current drive. FDSOI technology is used in a number of applications ranging from low-voltage, low-power to RF integrated.

1. $\Phi(x,0) = \Phi_f(x) = c_o(x)$ where $\Phi_f(x)$ is the front surface potential;
2. $\left.\frac{d\Phi(x,y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\Phi_f(x) - \Phi_{gs}}{t_{ox}} = c_1(x)$ where $\Phi_{gs} = V_{gs} - V_{FBF}$ is the front gate voltage, V_{gs}, minus the front-gate flat-band voltage, V_{FBF}.
3. If we assume that the buried oxide is very thick the potential difference across any finite distance in the BOX is negligible in the y direction we can write $\frac{d\Phi(x,y)}{dy} \cong 0$ in the BOX. Therefore, we have: $\left.\frac{d\Phi(x,y)}{dy}\right|_{y=t_{si}} = c_1(x) + 2t_{si}c_2(x) \cong 0$ and thus $c_2(x) \cong -\frac{c_1(x)}{2t_{si}}$.

Fig 1: SINGLE-GATE SOI MOSFETs

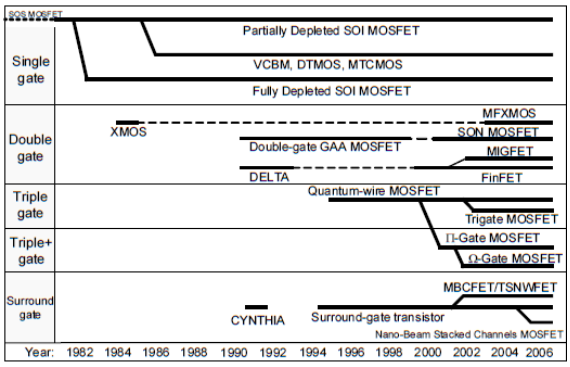

Fig 2: "Family tree" of SOI and multigate MOSFETs

III. DOUBLE-GATE SOI MOSFETs

The first article on the double-gate MOS (DGMOS) transistor was published by T. Sekigawa and Y. Hayashi 1984.[30] That paper shows that one can obtain significant reduction of short-channel effects by sandwiching a fully depleted SOI device between two gate electrodes connected together. The device was called XMOS because its cross section looks like the Greek letter Ξ (Xi). Using this configuration, a better control of the channel depletion region is obtained than in a "regular" SOI MOSFET, and, in particular, the influence of the drain electric field on the channel is reduced, which reduces short-channel.[31] A more complete modeling that includes Monte-Carlo simulations, was published by Frank, Laux and Fischetti in 1992 in a paper that explores the ultimate scaling of the silicon MOSFET.[32] According to that article, the ultimate silicon device is a double-gate SOI MOSFET with a gate length of 30 nm, an oxide thickness of 3 nm, and a silicon film thickness of 5 to 20 nm. Such a (simulated) device shows no short-channel effects for gate lengths larger than 70 nm, and provides transconductance values up to 2300 mS/mm. The first fabricated double-gate SOI MOSFET was the "fully Depleted Lean-channel TrAnsistor (DELTA, 1989)",[33] where the device is made in a tall and narrow silicon island called "finger", "leg" or "fin" (Figure 2). The FinFET structure is similar to DELTA, except for the presence of a dielectric layer called the "hard mask" on top of the silicon fin.

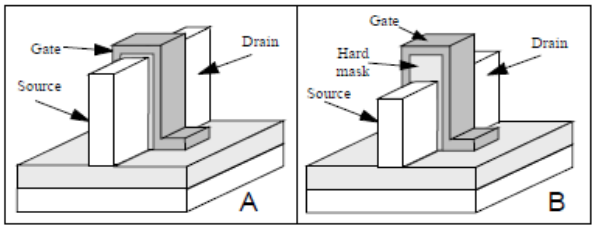

Fig 3: Examples of double-gate MOS structure: A: DELTA MOSFET; B:FinFET

Other implementations of vertical-channel, double-gate SOI MOSFETs with the gate electrode wrapped around the channel region (Figure of the channel depletion region is obtained than in a "regular" SOI The first fabricated double-gate SOI MOSFET was the "fully Depleted Lean-channel TrAnsistor (DELTA, 1989)",[3] where the device is made in a tall and narrow silicon island called "finger", "leg" or "fin" (Figure a dielectric layer called the "hard mask" on top of the silicon fin. [4-8] include the "Gate-All-Around device" (GAA), which is a planar MOSFET

1. $\Phi(x,0) = \Phi(x,t_{si}) = \Phi_f(x) = c_o(x)$ where $\Phi_f(x)$ is the front surface potential;
2. $\left.\frac{d\Phi(x,y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\Phi_f(x) - \Phi_{gs}}{t_{ox}} = c_1(x)$ where $\Phi_{gs} = V_{gs} - V_{FBF}$ is the front gate voltage, V_{gs}, minus the front gate flat-band voltage, V_{FBF}.
3. $\left.\frac{d\Phi(x,y)}{dy}\right|_{y=t_{si}} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\Phi_f(x) - \Phi_{gs}}{t_{ox}} = c_1(x) + 2t_{si}c_2(x) = -c_1(x)$ and thus $c_2(x) = \frac{-c_1(x)}{t_{si}}$.

Fig 4: DOUBLE-GATE SOI MOSFETs

IV. FinFETs

In a FinFET, if the height of the fin is greater than its thickness and the dielectric thickness on the upper side is greater than that on the lateral
sides, the FinFET can be analyzed as a vertical Double-gate MOSFET (Figure 3). Otherwise, carriers are quantized in two dimensions and therefore the approach developed in Section 2 would have to be considered. Several authors have claimed that volume inversion presents a significant number of advantages, such as: i) enhancement of the number of minority carriers; ii) increase in carrier mobility and velocity due to the reduced influence of scattering associated with oxide and interface charges and surface roughness; iii) as a consequence of the latter, an increase in drain current and transconductance; iv) a decrease in low-frequency noise, and v) a large reduction in hot-carrier effects.[11] In addition, like other dual-gated devices, DGMOSFETs are claimed to be more immune to short channel effects (SCE) than bulk silicon MOSFETs or even than single gate.

However, if the Si thickness is reduced, the whole silicon film is depleted and an important interaction occurs between the two potential wells. In such conditions the inversion layer is formed not only at the top and bottom of the silicon slab (i.e., near the two silicon-oxide interfaces) but throughout the entire silicon film thickness. It is then said that the at the Si/SiO2 interface, but distributed throughout the entire silicon volume.

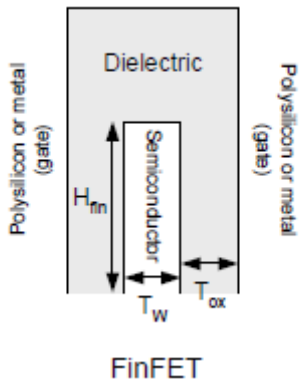

Fig. 5: Schematic representation of a FINFET

A 25 - nm electronic transistor operative on Simply zero .7 V was confirmed in Dec 2002 by Taiwan Semiconductor producing Company. The "Omega FinFET" style is called when the similarity between the Greek letter omega (Ω) and also the type during which the gate wraps round the source/drain structure. it's a gate delay of simply zero .39 time unit(ps) for the N
-type electronic transistor and zero .88 annotation for the P-type. FinFET may have 2 electrically freelance gates, which provides circuit designers a lot of suppleness to style with
economical, low- power gates.[8]In 2012, Intel started mi streatment FinFETs for its forthcoming business devices. Hot leaks suggest that Intel's FinFET form features an uncommon form of a triangle instead of parallelogram and it's speculated that this can be either as a result of a triangle features a higher structural strength and may be a lot of faithfully factory-made or as a result of a prism has a higher space to volume magnitude relation than an oblong prism therefore increasing switch performance.[9] Sept 2012, international Foundries declared plans to supply a 14-nanometer method technology that includes FinFET three -dimensional transistors in 2014. Ensuing month, the contestant company TSMC, declared begin early or "risk" fabrication of sixteen nm FinFETS in Gregorian calendar month 2013.

V. TRI-GATE MOSFET ALGORITHM

The fabrication flow of a Tri-gate MOSFET on an SOI substrate is shown in Figure 6. The SOI silicon top layer (Tsi) thickness defines the fin height (FinHEIGHT). The fin pattern and the critical dimension of fin width (FinWIDTH) can be defined by optical lithography or by spacer image transfer (SIT) [9-10], followed by plasma etching. After fin etch, the fin sidewall surfaces are rough. Therefore, oxidation and H2 annealing are often used to smooth the sidewalls.[10-11] Next, the gate dielectric is grown and metal gate is deposited. It is suitable to tune the threshold voltage (Vth) of the MOSFET by using a gate material that has the appropriate effective workfunction rather than by doping the channel. Sections 3 will show that it is highly desirable to have intrinsic or lightly doped channels. Since the gate stack is over the fin topography, a planarization step is desirable to flatten the gate surface, which reduces the burden on photolithography and gate etch. Significant overetch of the gate material is required to clear the bottom of the fins. As a result, the gate etch must have a high selectivity to the gate dielectric on top of the fin, if one wants to avoid damage to the fin during gate etch. Source and drain (S/D) extensions are formed after gate patterning using low-energy and large-tilt angled implants.[3] Next, S/D

offset spacers are formed along the sidewalls of the gate and fin. The sidewall spacers on the fins are subsequently removed to expose the fin to grow raised source and drain using selective epitaxy.[5] The raised source and drain structure helps to reduce the parasitic resistance associated with thin fins.[6] The rest of this chapter is divided into sections according to multi-gate device fabrication sequences. Section 3 covers fin formation, Section 3 describes gate stack structures, Section 3 describes source and drain formation and Section 3 highlights mobility and strain engineering.

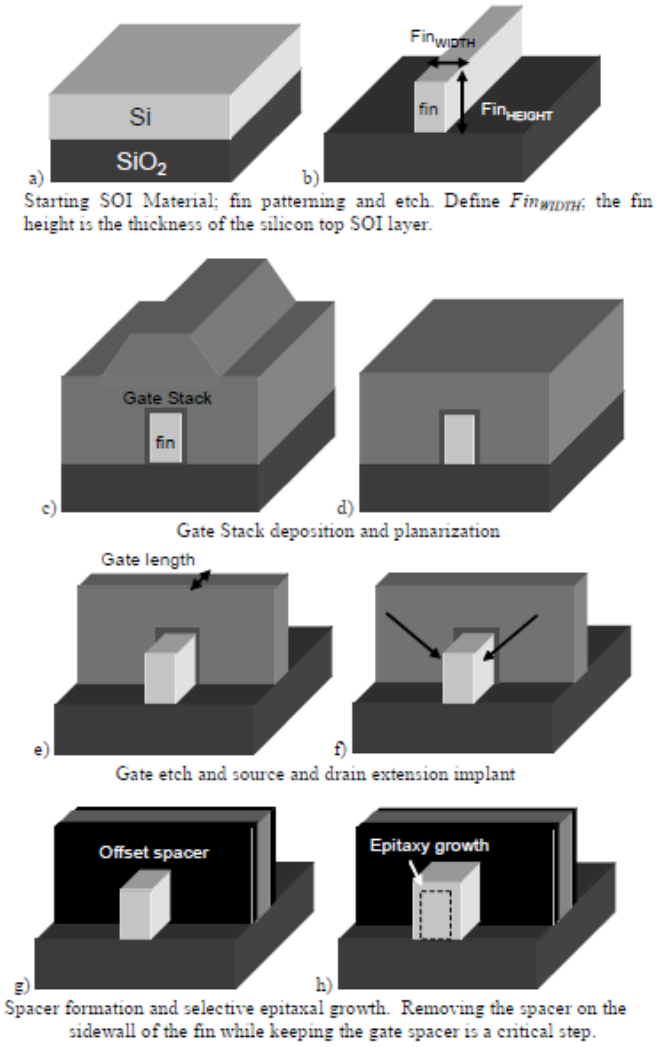

Fig 6: General Fabrication Sequence of a Tri-gate MOSFET.

VI. GATE ALL AROUND MOSFET

A cylindrical gate all around (GAA) with gate engineering, i.e., single gate material (SM) and two different gate electrode (DM) is explored and the performance evaluation is carried out with extensive device simulation by SentaurusTM simulator. The sensitivity of device parameters like *t*Si, *φ*M, and *L*g on various DC performances are systematically presented. Improvement in device performance for low standby operating power (LSTP) applications can be achieved with reduced in body thickness and *higher gate work function*. The subthreshold leakage current is significantly improved when the device approaches to the nanowire, i.e., *t*Si=10 nm, and for higher *φ*M values. Similarly, continuous miniaturization of *L*g is required for getting high *I*on and *g*m. The DM-CGAA shows a higher drive current as compared to SM counterpart with little compromise in off state leakage current. Hence, an appropriate selection of the silicon thickness, and metal gate work function give rise to an optimum threshold voltage at a given channel length and drain bias.

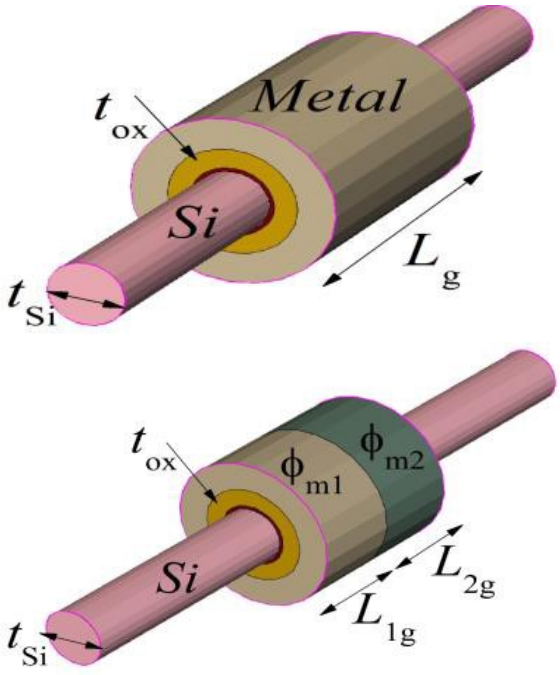

Fig 7: GATE ALL AROUND MOSFET

VII. MULTIGATE MOSFET MEMOREY DEVICES

SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) devices are non-volatile flash memory devices. They are essentially used in mobile applications.

Flash devices have a small form factor, high storage density and low power consumption. For logic applications FinFET type devices are known to have good scalability down to 10-nm gate length. The

FinFET device architecture combined with an ONO trapping layer as gate dielectric enables memory cells with feature sizes well below 50-nm. SONOS FinFET cells are programmed and erased using Fowler–Nordheim tunneling. SONOS FinFET memory devices show excellent functionality down to 20 nm channel length. [9] As an alternative to the ONO layer, nanocrystals embedded within the gate dielectric can be used to trap charges and achieve a similar memory effect. FinFET flash memory devices with a VTH window larger than 1 volt have been demonstrated using silicon nanocrystals embedded in the gate oxide.[9]

VIII. CONCLUSION

This paper summarizes the most recent trends within the style of MOSFET so as to mitigate the short channel effects & quantum effects. The multigate structures like metric weight unit , Trigate, and GAA mosfets have mentioned . The trend towards the necessity of other insulator materials additionally mentioned.

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X. AUTHOR'S PROFILE

Sushmita Jaiswal pursuing M.tech in Electronics and Communication Engineering from Shri Ramswaroop Memorial University (SRMU, UGC Affiliated) . Completed B.tech in Electronics and Communication Engineering from Hindustan Institute of Technology and Management, Agra (Affiliated with AKTU).. My area of interest is Nanoelectronics