© 2015 IJSRSET | Volume 1 | Issue 3 | Print ISSN : 2395-1990 | Online ISSN : 2394-4099
Themed Section: Engineering and Technology

Onboard Digital Receiver Architecture and Design of the Phase Radio-Navigation System for Aircraft Blind Landing

Saed Sasi*[1], Nasar Aldian Shashoa[2], Sulaiman Khalifa Yakhlef[3]
*[1] Department of electrical and computer engineering, Libyan Academy, Tripoli, Libya
[2,3] Electrical and Electronics Engineering Department, Azzaytuna University , Tarhuna, Tripoli, Libya

ABSTRACT

This work describes the architecture and design of an onboard digital receiver of the phase radio-navigation system for aircraft blind landing proposed in [1]. The proposed onboard digital receiver is a special case of a multi-channel narrowband digital receiver concept. The purpose of this receiver is to receive eight different RF frequencies (in four pairs) range from 960 MHz to 963.003749941 MHz, carry on them the required analogue and digital signal processing techniques to evaluate their phase shifts and then the difference phase shifts between each pair of them. The phase measurements lead to determination of the location of the aircraft with respect to the touch point on the runway with accuracy in millimetres.

Keywords: Radio-Navigation, Blind Landing, Analogue Front-End, Phase Shifts.

I. INTRODUCTION

Digital receivers represent the fundamental building block of the software radio industry. Digital receivers accept digitized samples of intermediate frequency (IF) or radio frequency (RF) signals typically derived from a radio antenna. They utilize digital signal processing techniques to translate a desired signal at certain frequency down to DC, and then remove all other signals by low pass filtering [3]. Authors in [2], proposed a method of measurement of a phase of complex radio signals, which allows determining the location of the plane with respect to the runway with sufficient accuracy. Where, they use four pairs of sinusoidal signals with different frequencies but with the same initial phase shifts at the ground transmitters, as;

f_1 =960000000 Hz, f_2 =960003749.941 Hz, then $f_2 - f_1$ = 3749.941 Hz.
f_3 = 961000000 Hz, f_4 = 961003749.941 Hz, then $f_3 - f_4$ = 3749.941 Hz.
f_5 = 962000000 Hz, f_6 = 962003749.941 Hz, then $f_5 - f_6$ = 3749.941 Hz.
f_7 = 963000000 Hz, f_8 = 963003749.941 Hz, then $f_7 - f_8$ = 3749.941 Hz.

However, the sinusoids of very close frequencies are used; they must be filtered and separated from each other using long filters. In this work, proposed an architecture of an onboard digital receiver, accepts eight (in four pairs) different RF frequencies range from 960 MHz to 963.003749941 MHz, carry on them the required analogue and digital signal processing to evaluate their phase shifts.

II. OVERVIEW OF SYSTEM ARCHITECTURE

A Fig. 1 shows the block diagram of the proposed onboard digital receiver. It consists of the following main parts: analogue front-end, digital local oscillator, digital mixers, bank of multi rate digital filters, and phase measurements algorithm.

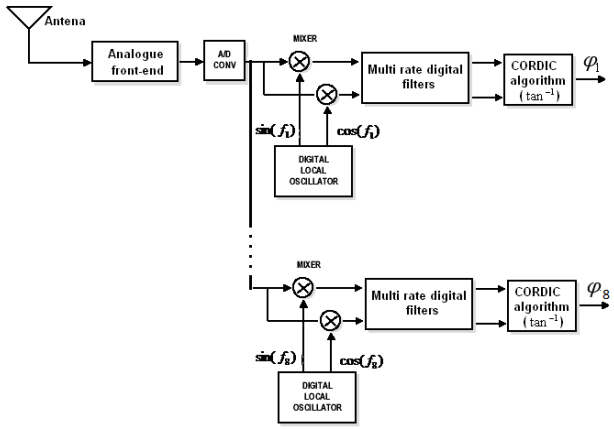

Figure 1: Onboard digital receiver architecture

III. ANALOGUE FRONT-END

An antenna and an analog front-end always needed Because of the analog nature of the air interface. Generally, the analog front-end will contain an amplifier, band-pass filter and an analog mixer to convert the received signal to a suitable intermediate frequency (IF) or baseband. In this stage of onboard digital receiver design, this part of the system will be seen as a black box receiving eight different RF frequencies range from 960 MHz to 963.003749941 MHz, and outputting IF frequencies range from 5 MHz to 8.003749941MHz.

In order to sample the IF spectrum (5 to 8.003749941MHz), an Analog to Digital Converter (ADC) would require a sample rate greater than 24 MSPS in order to meet the Nyquist criterion. Fig. 2 shows the analog front-end output (IF spectrum). This spectrum represents eight received channels shifted from RF to a much lower intermediate frequency.

$$f_1 = 5000000\,\text{Hz}\ ;\ f_2 = 5003749.941\ \text{Hz}\ ;$$
$$f_3 = 6000000\,\text{Hz}\ ;\ f_4 = 6003749.941\ \text{Hz}\ ;$$
$$f_5 = 7000000\,\text{Hz}\ ;\ f_6 = 7003749.941\ \text{Hz}\ ;$$
$$f_7 = 8000000\,\text{Hz}\ ;\ f_8 = 7003749.941\ \text{Hz}$$

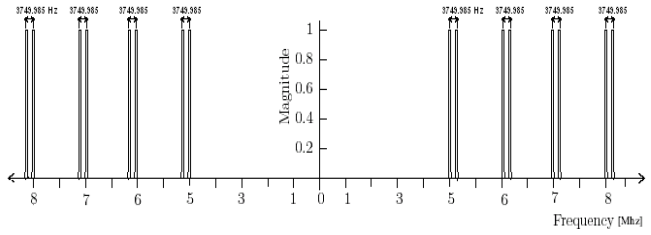

Figure 2: Analog front-end output (IF spectrum)

IV. DIGITAL LOCAL OSCILLATOR (LO)

In terms of system performance, the critical component in digital down-conversion is the Digital Local Oscillator (LO). This component generates a sampled digital sinusoid, which when mixed with the incoming signal, shifts the signal's spectrum. In order to shift the targeted signals to DC (0 Hz), the LOs should generate frequencies that are identical to the incoming signals, and they are as follows

$$f_{LO_1} = 5000000\,\text{Hz}\ ;\ f_{LO2} = 5003749.941\ \text{Hz}\ ;$$
$$f_{LO3} = 6000000\,\text{Hz}\ ;\ f_{LO4} = 6003749.941\ \text{Hz}\ ;$$
$$f_{LO5} = 7000000\,\text{Hz}\ ;\ f_{LO6} = 7003749.941\ \text{Hz}\ ;$$
$$f_{LO7} = 8000000\,\text{Hz}\ ;\ f_{LO8} = 7003749.941\ \text{Hz}$$

The LO is actually a direct digital frequency synthesizer delivering sampled sine and cosine waveforms at a programmable frequency. The LO is driven by the A/D sampling clock. Direct digital frequency synthesis, or DDFS, is a digital technique for generating sinusoids. The DDFS consists of a phase accumulator (an adder and a register) and a sine/cosine generator to generate digital quadrature sine and cosine signals. The sine/cosine generator in the DDFS architecture generally assumes one of the two forms: a ROM table for lookup-table or an arithmetic unit to actually evaluate the function. The former can be found in most of the early implementation [4] [10] [11] [12]. The major difficulty with this approach is that the size of the ROM table increases exponentially with the width (i.e., the resolution) of the output. Even though there have been several techniques proposed to mitigate this problem [4] [5] [6], which partition the ROM table to reduce the size. Using an arithmetic unit is an alternative to the ROM table approach that has been getting attention recently. Especially, the CORDIC algorithm [7] has been dominant in this approach because it only requires shift-and-add operations, while other approaches based on functional approximations involve more complicated arithmetic operations such as multiplication [8]. One last point to mention, that the onboard LOs should work simultaneously, in other words the initial phase shift in all of them should be equal.

V. DIGITAL MIXERS

One of major components of the digital receiver is the Mixer as shown in Fig. (1). The Mixer actually consists of two digital multipliers. Digital input samples from the A/D are mathematically multiplied by the digital sine and cosine samples from the local oscillator. Note that the input A/D data samples and the sine and cosine samples from the local oscillator are being generated at the same rate, namely, once every A/D sample clock. Since the data rates into both inputs of the mixers are the A/D sampling rate, f_s = 24 MHz, the multipliers also operate at that same rate and produce multiplied output product samples at 24 MHz. The sine and cosine inputs from the local oscillator create **I** and **Q** (in-phase and quadrature) outputs that are important for maintaining

phase information contained in the input signal. From a signal standpoint, the mixing produces a single-sideband complex translation of the real input. Unlike analog mixers, which also generate many unwanted mixer products, the digital mixer is nearly ideal and produces only two outputs: the sum and difference frequency signals. Fig. (3) shows the mixer product in the frequency domain. At the output of the mixer, the high frequency signal f_1 in the A/D input has been translated down to DC. In this onboard digital receiver, eight digital mixers are needed, each consists of two digital multipliers, one multiplier for the sine and the other for the cosine.

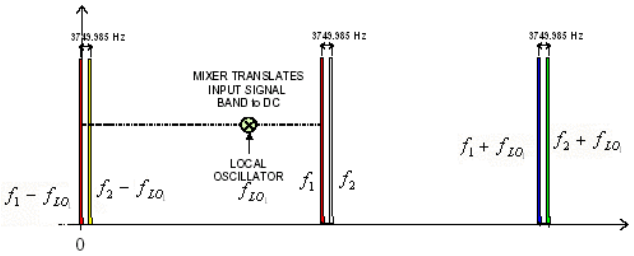

Figure 3: Digital mixer output

VI. MULTI RATE DIGITAL FILTERS

In this blind landing system design, superimposed sinusoids were chosen for implementation, as mentioned in [2]. The price paid while separating the close two sinusoids. For example, when the received signal converted to the base-band the result is a signal (tone) at the frequency $\Delta f = f_2 - f_{LO_1}$ and the expected DC term, as shown in Fig.(4). In addition to filtering the terms at $f_1 + f_{LO_1}$, $f_2 + f_{LO_1}$ frequencies, and the difference and the summation results from process of mixing the local oscillator frequency f_{LO_1} with the frequencies f_3, f_4, f_5, f_6, f_7, and f_8, the low pass filters should be sharp enough to filter out the Δf frequency. To separate $f_1 - f_{LO_1}$ (DC) from a $\Delta f = 3749.985$Hz signal at a sampling rate of 24 MHz, it is clearly seen that the low pass filter should have a null before

$$f_c = \frac{3749.985}{24*10^6} = 0.00015624$$

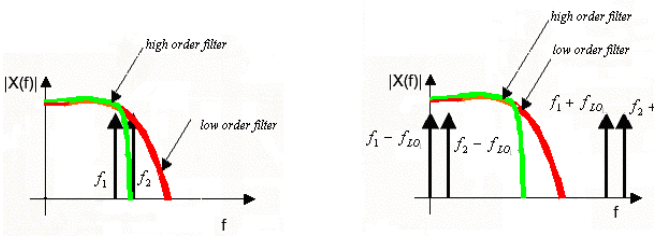

Figure 4 : Two superimposed signals before and after mixing down respectively

VII. DOWN SAMPLING USING CIC MULTI-RATE FILTER

Cascaded integrator-comb (CIC) are multi-rate filter that provide a practical approach to designing and implementing finite response (FIR) filters with narrow spectral constraints. By changing the input data rate at one or more intermediate points the filter lengths and computational rates can be greatly reduced when compared to a standard single-rate filter implementation.

Since the desired sampling rate is around 10 KHz, and decimation factor of $f_{out} = \frac{24*10^6}{2048} = 11718.75$ Hz, output sample rate of 11718.75 Hz is a good fit. Then, the multi-rate filtering stages will be a cascaded integrator-comb (CIC1) filter (D=64), (CIC2) filter (D=8), FIR_1 (D=2), FIR_2 (D=2) for an overall sample rate reduction of 64*8*2*2=2048. The last filter (D=2) determines the ultimate frequency response characteristics. Fig. 5 shows the Cascaded Integrator-Comb (CIC) filter architecture.

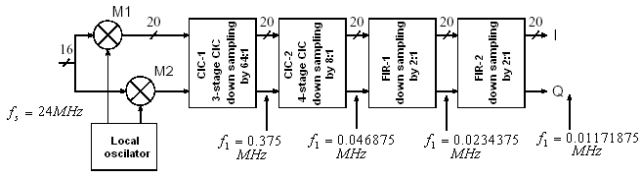

Figure 5: Cascaded Integrator-Comb (CIC) filter architecture

VIII. PHASE MEASUREMENT

Before starting the discussion about the phase wrapping algorithms, One last point to consider is that the measured phases do not only include the phase shift φ, which is due to distance travelled, but also terms due to the arbitrary initial phases of the transmitter oscillator ρ_0 and the receiver local oscillator ρ_{LO}. As was mentioned in [2], if ρ_0 and ρ_{LO} are equal for both frequencies, these initial phases can be easily cancelled. The Direct Digital Frequency Synthesizers (DDFS), is one main way to control the initial phases precisely. This way the initial phases at both frequencies can easily be set equal. Phase wrapping is the process of determining the phase values of the fringe patterns in the range of zero to 2π. Traditional phase-wrapping algorithms involve the calculation of an arctangent function. Generally, the trigonometric functions like arctangent evaluated using;

- Table lookup
- Polynomial approximations
- CORDIC algorithm

Compared to other approaches, CORDIC is a clear winner when a hardware multiplier is unavailable (e.g. in a microcontroller) or when you want to save the gates required to implement one (e.g. in an FPGA). On the other hand, when a hardware multiplier is available (e.g. in a DSP microprocessor), table-lookup methods and good old-fashioned power series are generally faster than CORDIC.

IX. CONCLUSION

In this work, proposed onboard digital receiver architecture of the phase radio-navigation system for aircraft blind landing proposed in [1]. The proposed onboard digital receiver receives eight (in four pairs) different RF signals range from 960 MHz to 963.003749941 MHz; these signals are received by the analog front-end section of the receiver. The analog front-end section converts the received signals to an IF with frequencies range from 5 MHz to 8.003749941MHz. In order to meet the Nyquist criterion, the IF spectrum (5 to 8.003749941MHz) sampled using an Analog to Digital Converter (ADC) with a sample rate of 24 MSPS. To bring (translate) down the IF frequency signals to DC, a suitable digital mixer and local oscillator were proposed. However, the sinusoids of very close frequencies are used, they must be filtered and separated from each other using long filters, To overcome the problem of using long FIR filters in the implementation of the design, a four stage Cascaded Integrator Comb proposed.

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