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VSC HVDC System Implementation Using Hybrid Simulation Model

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ABSTRACT

The extensive scale presentation of high voltage direct current (HVDC) systems requires tackling various complex assignments went for guaranteeing the reliability and stability of new consolidated HVDC/AC systems. In this paper, we are enlarging the level for enhancing the efficiency and decrease the losses. The renovation of their supervision assurance and exploration of common impact of HVDC and HVAC parts is proposed. To make a satisfactory model of HVDC it is relevant to provide completeness and exactness of the procedure portrayal in steady-state and transient operating conditions. This paper displays the particular idea of hybrid simulation for progressivemolding of VSC HVDC. To affirm the ampleness of simulation procedure, the exploration of created 5-level VSC HVDC demonstrates attributes in static modes on a model of two-machine has been given. The multilevel inverter has many focal points, for example, immense Power quality, minor order harmonics, minor switching losses, and better electromagnetic impedance. By expanding inverter with 5-level then we realize an unadulterated sinusoidal waveform and furthermore decrease the losses. This paper displays the hybrid simulation innovation and approach permitting blending hybrid models of power hardware, including the components of HVDC systems, whose point is to maximally meet present day necessities for demonstrating and simulation instruments.

Keywords: HVAC, HVDC, RES, VSC, LCC, IGBT, GTO, EPS, IGBT, Specialized Hybrid Processor, RES

I. INTRODUCTION

These days, multilevel inverters have gotten more consideration for their capacity on immense-power and moderate voltage operation and subsequently different points of pursuit, for example, immense power quality, minor order harmonics, minor switching losses, and better electromagnetic obstruction [1], [2]. These inverters yield a stepped voltage waveform by utilizing various dc voltage sources as the info and a proper course of action of power semiconductor-based gadgets. In late year if we take a view at the expanding in multifaceted nature in power systems which delivers to new difficulties for guaranteeing their reliability and manageability [1]. Along with that to accomplish advance at power electronics which guarantees the new prospects of utilizing HVDC systems, we had as of now enhance and accomplished their viability in arrangement of regular undertakings, for example, asynchronous interconnection and long distance transmission, and simultaneouslyof generally new difficulties identified with allianceof distributed renewable energy sources (RES) into AC grids.

Power electronic converters depend on power semiconductors which is the primary component of this innovation. HVDC is relying on two sorts of converters. They are line commutated converter (LCC) and voltage-source converter (VSC), which are broadly utilized as a part of EPS [2]. VSC relies on completely controlled immense-speed power switches (IGBT, GTO) which might be distinctive sorts of favorable circumstances when contrast and the LCC, for example,

- Control of active (P) and reactive (Q) power;
- Provision of reverse of power flow without changing polarityof voltage.

Be that as it may, rise and vast scale establishment of recent HVDC gear and plans, for example, VSC based systems and multi-terminal connections both open new chances to enhance controllability of power systems and

increment the extent of operational and research tasks.The uttermost unpredictable and earnest of those assignments include:

- Analysis of shared impact of HVDC and HVAC systems, including their control and security upon each other and power framework all in all, particularly in transient conditions;
- Development, testing and acclimationof local and generalized control and protection systems.

An answer of these errands requires full-scale explores in a real power framework, which can't be abetted. Along these lines, simulation remains the primary apparatus for breaking down HVDC systems inconfiguration of extensive power systems.

However, the immense prerequisites to power framework test systems are abetted by the multifaceted nature of undertakings adding to a complete exploration of procedures happening in power systems, and also by convertors qualities.

Currently, digital test systems are generally utilized for power framework investigation. The confinements of digital test systems are notable and are foruttermost part dictated by the used numerical integration strategies, which force some noteworthy disentanglements and presumptions on power gear models. This leads disintegration of power framework errands, exertion of different numerical strategies and absence of model's points of pursuit.

A hybrid simulation innovation can fill in as a grant for purely digital simulation. This innovation isbuild upon blend of simulation devices and models of power framework components as indicated by the prerequisites ofexploration errands [3]. Be that as it may, exertion in said hybrid simulation innovation convolutes advancement in models and applies some extra necessities to them. This paper proposes an approach and exhibits aftereffects ofprogressof hybrid model of HVDC framework that totally meet the necessities to the propelled power framework simulation.

II. OPERATION OF VSC

To make a sufficient model of HVDC it is relevant to give fulfillment and exactness of procedure depiction in steady-state and transient operating conditions, controlled by demonstrating execution mistakes at all the said digital, analog, and physical levels of simulation. Digital simulation is done just for control arrangement of HVDC.

When displaying the mistakes at physical model level prompt a deviation of misfortune level, mutilation of voltage and current waveforms on both the DC and AC side in critical recurrence range of EPS. In view of this, simulation of process at physical model level is basic to the demonstrating comes about, particularly for pulse method of VSC. Mistakes at this level can be caused by inaccurate qualities in power semiconductors or parameters of DC circuit. The last issue is effectively settled by arbitratingsegments [4]. The qualities of physical models in power semiconductors require extra exploration and will be tended to in future works.

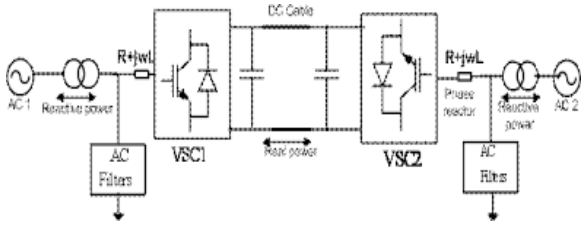

Figure 1: Block diagram of VSC HVDC model

III. 5-LEVEL INVERTER

Various industrial exercises have started to craveimmense power contraption lately. Some moderate voltage motor drives and utility exercisescravemoderate voltage and megawatt power level. For a moderate voltage grid, it is messy to associate just a single power semiconductor switch straightforwardly. Consequently, a multilevel power converter design isconferred as a grant in immense power and moderate voltage circumstances. A multilevel converter consummateimmense power estimates, conjointlylegitimatesexertion in RES. RES, for example, photovoltaic, wind, and fuel cells might be effectively merged to a multilevel converter framework for a powerful application. The idea of multilevel converters is conferred by NABE-EL Since 1975 .The different focal points of multilevel inverter are, they can produce yield voltages with to a great degree low bending and minor dv/dt, they draw input current with low mutilation, they create littler common-mode (cm) voltage, hence decreasing the worry in motor orientation, they can work with a minor switching frequency. The

diode clamped multilevel inverter was likewise termedas neutral point clamped (NPC) inverter. When it was initiallyexploited as a part of a three level inverter in which the mid voltage level was characterized as neutral point in light of fact that the NPC inverter successfully copies the gadget voltage levels without requiring exact voltage coordinating.

Number of DC bus capacitor in a multi level inverter is chosen by (n-1), Number of switches in Multilevel inverter is chosen by2*(n-1), Voltage source is chosen by Vdc/(n-1) and clasping diode is inured by (n-1)*(n-2). Where 'n' is number of level ofan inverter. For a five level inverter appeared in "fig.2".

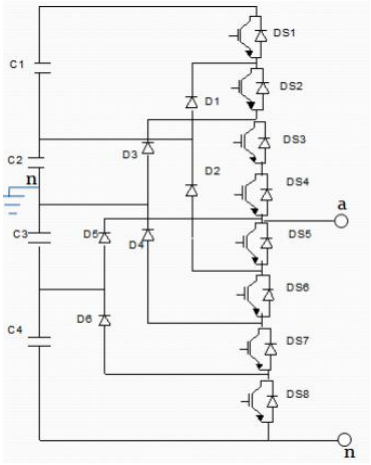

Figure 2: Five level Inverter

In this circuit, the DC bus voltage is part up in to 3 levels as appeared. Five-level diode-clamped converter in it DC bus comprise of 4 capacitor C1,C2,C3,C4 for DC bus voltage Vdc, the voltage over every capacitor is Vdc/4 and every gadget voltage stress is constrained to 1 capacitor voltage levels Vdc/4 through clipping diodes, For voltage levels Van= Vdc/2 turn on every upper switches S1-S4, For voltage level Van= Vdc/4, turn on 3 upper switches S2-S4 and bottom switch S5,For voltage level Van=0, turn on 2 upper switches S3 and S4 and 2 bottom switches S5 and S6, For voltage levels Van= - Vdc/4, turn on 1upper switch S4 and 3 bottom switches S5-S7 and for voltage levels Van=-Vdc/2, turn on all bottom switches S5-S8 NPC inverter which is broadly exploitedpresently in industrial drives, footing and simultaneously FACT's framework Based on idea of utilizing diodes to restrict power gadgets voltage push Output stage voltage can expect any voltage level by choosing any of hubs.

Switching states	Output voltages	DS1	DS2	DS3	DS4	DS5	DS6	DS7	DS8
+1	Vdc/2	1	1	1	1	0	0	0	0
+2	Vdc/4	0	1	1	1	1	0	0	0
0	0	0	0	1	1	1	1	0	0
-2	-Vdc/4	0	0	0	1	1	1	1	0
-1	-Vdc/2	0	0	0	0	1	1	1	1

Table 1. Switching States Diode Clamped five Level Inverter

DCMI is considered as a kind of multiplexer that joins the yield to one of accessible hubs. Albeit principle diodes have same voltage rating as primary power gadgets, much minor current rating is permissible For three-stage DCMI, the capacitors need to channel just the immense-arrange harmonics of clasping diodes currents, low-arrange segments naturally scratch off each other. Each power gadget squares just a capacitor voltage Clamping diodes piece switch voltage.

IV. SIMULATION CHALLENGES

To enhance issue in reliability and ampleness of simulation forms in a real VSC HVDC the demonstrating framework should consider the specifics of operation of these gadgets, specifically:

- Phase-Phase operation of VSC;
- Use of immense-speed fully controlled power semiconductors;
- Continuous immense-speed operation in all conceivable typical, crisis and post-crisis operating states of EPS.

Besides, to realize previously mentioned issues, simulation systems should meet the accompanying prerequisites.

- Models of EPS elements ought to be3-phase (or more) to recital properly for all unbalanced conditions;
- Simulatorought to becompetent (scalable) to apply an EPS model of any size;
- Simulation of EPS must reject the disintegration of procedures and constraints on their span (without division of electromagnetic and electromechanical transient procedures demonstrating in power hardware and EPS all in all);
- Real-Time Simulation and prospect of interconnection with external devices and systems.

As of late digital demonstrating buildings are highly exploitedfor exploration of EPS. This edifices have been appeared to be fruitful in electromagnetic transients and shut circle testing of ACS in simulation [5], yet in digital simulation apparatuses the numerical integration techniques don't empower to perform real time simulations of EPS without procedures of decay over a boundless timeframe on account of integration time step issue.

Along with that the digital simulation of extensive EPS is influenced by issues related along with the constraints ondepth of a model settled by a solitary processor. At that point the model apportioning and use of voyaging wave transmission line models to associate the parts of a power framework show distributed between a few processors is required[6]. A trap of use of voyaging wave show is that a voyaging time of a transmission line ought to be more prominent or equivalent to an integration time step which is not generally open and consequently may require constrained acclimation of inductance and capacitance estimations of a transmission line display.

The dispersion of EPS demonstrate limits the extent of processors, that can be afilliated with one hub, and prompts constrained rearrangements and equal portrayals of power hardware and EPS models. These impediments of digital demonstrating buildings are appeared in simulation of short transmission line (in consecutive HVDC framework), or simulation of Multiterminal HVDC ventures with a short DC (direct current) connect.

Along with that issue of reproducing in real time expansive EPS with no division of electromagnetic and electromechanical transient procedures have been not made strides. From this statement is affirmed by watched inclines in innovative work of hybrid simulation instruments, in light of exertion of different numerical simulation strategies

Simultaneously, after the point by point exploration of some said and hybrid edifices clearly that required definite and far reaching demonstrating of EPS is not completely accomplished [7]. Along these lines, to dissect the procedures caused by deficiencies in HVDC convertors creators utilized simulation time venture around 50 μs, while switching time of Gate side road thyristors is around 30 μs, for IGBT 5 μs. Other than the information trade between the utilized edifices is done with greater simulation time venture than simulation time venture of electromagnetic transients demonstrating.

To enhance the said issue of real time simulation of HVDC systems and EPS all in all, the hybrid simulation innovation rely onexertion of digital, analog and physical displaying approaches and realized in Hybrid Real-time Simulator of EPS (HRTSim), created in Tomsk Polytechnic University, which is proposed. The aftereffects ofprogress and research of VSC demonstrate, realized in HRTSim and are appeared in this article.

Ideas of Hybrid Simulation of EPS

Here, the idea of hybrid simulation is relying onexertion of three displaying approaches: physical, analog and digital, each of which consummateuttermost extreme efficiency in comprehending individual subtasks. A definite portrayal of ideas and devices is introduced. The essential intentof ideas is:

- Power Equipment of EPS is described via complete systems of differential equations adequately representing the whole significant range of quasi-steady and transient courses in this apparatus and conceivingcatholic mathematical models of interrelated types of simulated apparatus;
- Vocationallystrict with affirmed instrumental error explication of differential equation systems in real time and over an limitless period of time are effectuated by virtueof continuous latent integration method;
- Types Of Commutation of power apparatus, including power semiconductors, are effectuated on a model physical level;
- Interconnection between a physical model and mathematical simulation levels is yielded by virtue of appropriate voltage-current converters;
- Mutual conversion of mathematical and model physical variables in alliance with simulation on physical model level of commutation of power apparatusserves the competency of limitless scalability of simulated EPS;
- Informational and control functions, conjointlymolding control and protection systems are implemented on a digital level using a digital-to-analog, analog-to-digital conversion and specialized local and server software.

Specialized hybrid processor (SHP) is the fundamental component of measured configurationof HRTSim and gives a satisfactory extensive simulation in real-time of power hardware models, and simultaneously control and insurance systems.

As indicated by this idea, the arrangement of complete numerical models of reproduced hardware is done through the hybrid coprocessors (HCP). The consequence of arrangement is imparted to the MPU (chip unit) through the PADC (processors of analog-to-digital converter). The entire scope of information changes required to supervise the procedure of simulation, and additionally real-time control of parameters of demonstrated power gear, contingent upon the coveted arrangement speed of a control calculation, are executed in MPU.

The all inclusiveness of idea and particular configurationofHTRSim permit the progress of a model of any component of EPS, including gadgets and HVDC, and to coordinate them into the HTRSim, and simultaneously furnish interconnection with different outside programming and equipment instruments: operational data systems, SCADA framework and so forth.

Simulation of Commutation Process

As specified over, physical model level is especially critical, on grounds that at this level an operation of power switches is demonstrated by means of integrated microelectronic digitally controlled analog switches (DCAS).

In this section the IGBT switch is modeled in physical model and the complete commutation process of real IGBT is verified to check the completeness of simulation process and for the reliability of the devices operation.

The current and voltage wave forms of the real IGBT verifies the time of operation of the switch. Here IGBT (type no 5SNR) is used and its switching time is about 5 micro seconds.

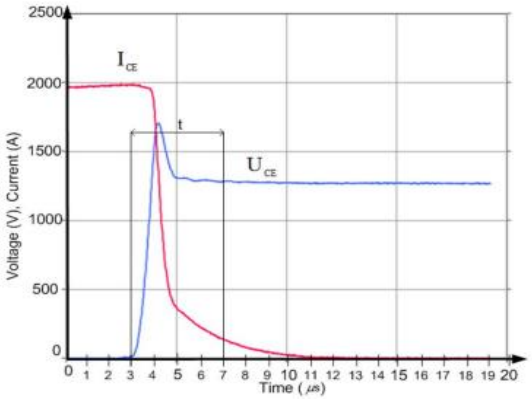

Figure 3: The current and voltage waveforms of real IGBT (type 5SNR).

In this section the simulation of real IGBT with snubber and without snubber is verified. Thus the adequate representation of simulation process of the devices used in VSC HVDC is realized. Which defines the completeness of simulation of the devices and their reliability of operation?

Simulation of VSC HVDC

In simulation of VSC HVDC,including the frequency characteristics of HCP of basic equipment of HVDC and static modes at different levels of power consumption/generation and voltage of VSC HVDC were considered.

The pattern of simulation research of SHP of VSC HVDC in EPS is delineated in Fig5.

The parameters of study system pattern are represented in[23].

The obtained waveforms of voltage UA(t),current iA(t),conjointly calculated values of apparent S(t), real P(t) and reactive Q(t) powers are delineated in Fig 6-7.

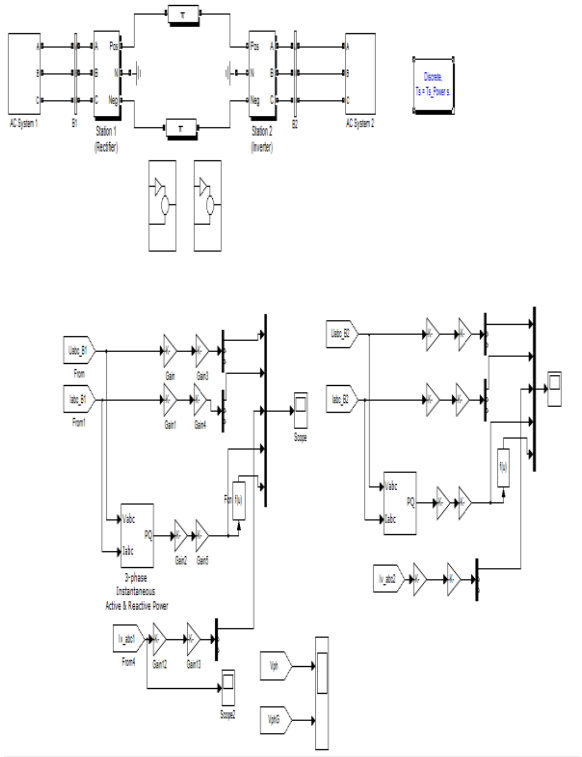

Figure 4: The pattern of simulationresearch of VSC HVDC model: Tr- transformer, F- filter, C- capacitor bank.

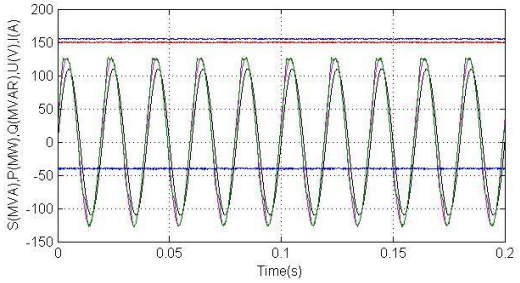

Figure 5: The mode of consumption of P(t) and generation of Q(t).

Here the sinusoidal wave forms are currents i(t) and voltage v(t), s(t) and p(t) is on positive side and Q(t) is on negative side.

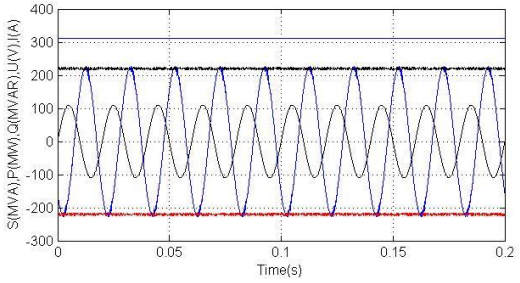

Figure 6: The mode of generation of P(t) and consumption of Q(t).

Here i1A(t), i2A(t) and U(t) are sinusoidal waveforms and current is the leading quantity and s(t), Q(t) are on positive side and p(t) is on negative side.

Oscillograms of voltage U1(t) (see Fig. 12) on AC side of VSC obtained by a digital oscilloscope are delineated in Figures 7-8.

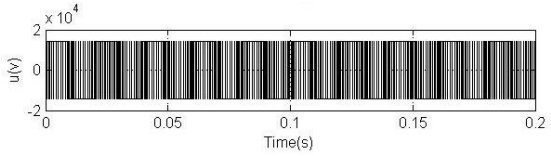

Figure 7 : The oscillogram of phase voltage of VSC HVDC model.

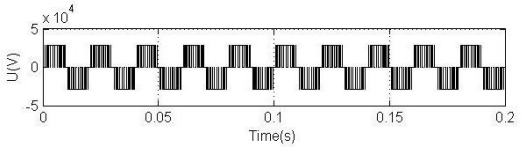

Figure 8 : The oscillogram of phase-to-phase voltage of VSC HVDC model.

V. CONCLUSION

This paper introduces the specific idea of hybrid simulation for cutting edge displaying of VSC HVDC. The multilevel inverter has a few points of pursuit, for example, immense power quality, minor order harmonics;minor switching losses, and better electromagnetic impedance. The idea of hybrid simulation realization will indicate plausibility and efficiency of proposed way to handle the progressof models in power semiconductors and VSC which is built up on it, along with that it will Satisfy the whole arrangement of necessities for cutting edge simulation set by the advancing power framework operating assignments; Develop an adaptable, adaptable and real-time client configurable model of HVDC framework. To affirm the efficiencyof simulation procedure, the exploration of created 5-level VSC HVDC demonstrates qualities in static modes on a model of two-machine has been given. In this paper, we are expanding the level for enhancing the efficiency and decrease the losses. The outcomes which is utilized to permit complete the itemized portrayal of commutation procedure of IGBT and sufficient demonstrating of unearthly exploration of VSC, in meantime it will thorough real-time simulation forms in HVDC and EPS in general with no constraint and disintegration on their term By utilizing simulation aftereffects of specific hybrid processor of VSC HVDC show affirm the adequacy of proposed strategy.

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