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Brief Introduction about VHDL Implementation of CVSD Codec

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ABSTRACT

In order for the signal to have good quality, the slope-overload error desires to be as small as possible. Adaptive delta modulation reduces the slope over load error to a greater extent. One of the algorithms of ADM is CVSD algorithm. CVSD (continuous variable slope delta) modulation is an effective scheme for audio signal. CVSD is best coding technique for improving receiver sensitivity with low transmission rate as compare to PCM. Here in this paper, we discuss the implementation of CVSD codec system using VHDL (Very High Speed Integrated Circuit Hardware Description Language). VHDL provides structure to be modelled and simulated before synthesis tools (XST tools). It allows the description of a concurrent system. It is portable and multipurpose. These paper is also describes the various RTL schematic of each module of the CVSD codec and the connections of all RTL blocks in Top level design.

Keywords: Register Transfer Level (RTL), DM, ADM, VHDL, Verilog, PIPO, SIPO.

I. INTRODUCTION

Design of CVSD codec algorithm using VHDL (Very High Speed Integrated Circuit Hardware Description Language) VHDL is commonly used to model the digital system.

Continuously variable slope delta modulation (CVSD or CVSDM) is an audio encoding method. It is a delta modulation with variable step size [3]. Because of variation in step size slope overload error is reduces as compare to delta modulation [6]. The CVSD modulation is a method of digitizing a band-limited audio signal. The CVSD modulator is many to one bit compression technique, which compresses the 8 bit into 1 bit or 16 bit into 1 bit or 12 bit data into one single bit. It is a lossy compression technique. The output of this 1-bit encoder is a serial bit stream, where each bit represents an incremental increase or decrease in signal steps amplitude level. The continuously variable slope delta (CVSD) modulation is a nonlinear [1], sampled data, closed loop system which accepts a band-limited analog signal and encodes it into binary form for transmission in a digital channel. At the receiver, the binary signal is decoded into a close approximation of the original amplitude level. Continuously Variable slope Delta Modulation is a simple syllabically step adaptive DM scheme offering low hardware complexity, improved noise performance and minimum transmission Bandwidth [2]. It is an attractive alternative to more complex conventional analog to digital signal conversion techniques used in telecommunication and signal processing. To implement CVSD, There are few CVSD chip sets such as MC34115 from Motorola [1-4] but it works only at 16 kbps and it does not allow adding encryption to the algorithm, which is very important in defence systems for security purposes. CVSD is used in both commercial and military communications where "toll quality" or "communications quality" is required, yet low computation complexity and low memory requirements are desirable. Two examples of this technique are U.S. MIL-STD-188-113 (16 kbps and 32kbps CVSD) and U.S. Federal Standard 1023 (12 kbs CVSD) [5]. In addition, encoded CVSD data can be encrypted and made more secure (because of adaptive in nature), which is desirable for many wireless communications applications including speech and general-purpose audio coding. Furthermore, to implement such algorithms with encryption possible, software (i.e. programming in DSP/GPP) and hardware (i.e. programming in FPGA or ASIC i.e. programming in VHDL or Verilog) approaches are available.

II. Various Modules and RTL Schematics

A. 8 bit comparator design

Data comparisons are mostly needed in digital systems while performing arithmetic and logical operations. The comparison determines whether one number is greater than equal to, or less than the other number. A digital comparator is widely used in combinational system and is specially designed to compare the relative magnitudes (decimal equivalent of binary numbers). These are also available in IC form with different bit comparing configurations such as 2-bit, 4-bit, 8-bit, etc. More than one comparator can also be connected in cascading arrangement to perform comparison of numbers of longer lengths like 8 bit or more. Whenever we want to compare the two binary numbers, first we have to compare the MSB of the inputs. Here, two binary variables are used to indicate the outcome of the comparison as a ≥ b or a < b ('a' and 'b' are 8 bit input array). The below figure shows the RTL Schematic of 8 bit comparator Module which is Created by VHDL code in Xilinx.

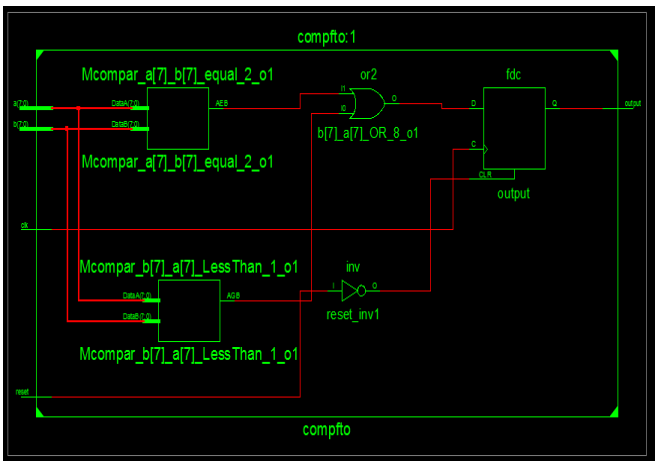


Figure 1. 8 bit Comparator RTL Schematic view in Xilinx

Here in above RTL schematic two block connected to one OR gate. If a>b the output of block one is high otherwise low. If a=b then output of second block is high otherwise low. So if a<b then output of the OR gate is low otherwise output of OR gate us high. The output of OR gate is connected to D flip-flop. The D flip- flop output is the output of the 8 bit comparator. The Flip- flop is connected to the clock (clk), and Reset input. If the reset is low then output of the comparator is always 0. For every positive edge of the clock, the comparator gives the output.

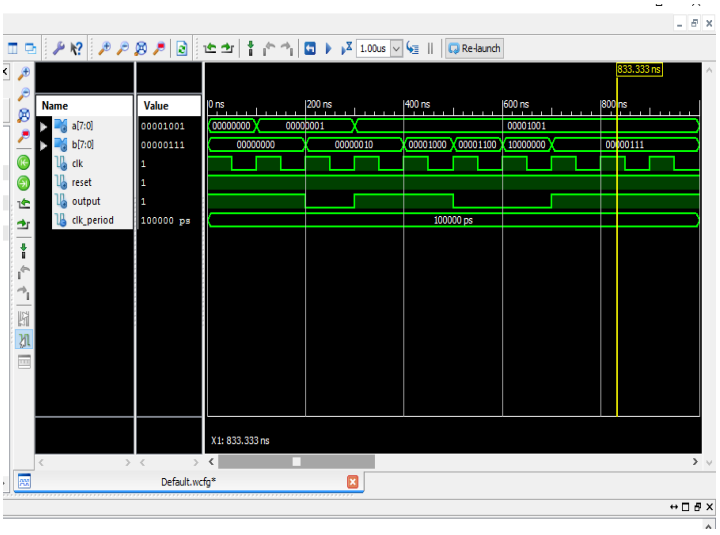


Figure 2. Test-bench simulation of 8 bit comparator created in Xilinx

B. 8 bit PIPO register

Parallel in Parallel out (PIPO) shift registers are the type of storage device, which holds the data for 1 clock cycle. Here PIPO register is used as an buffer to provide 1 clock cycle delay for providing comparison between present input and previously selected output.

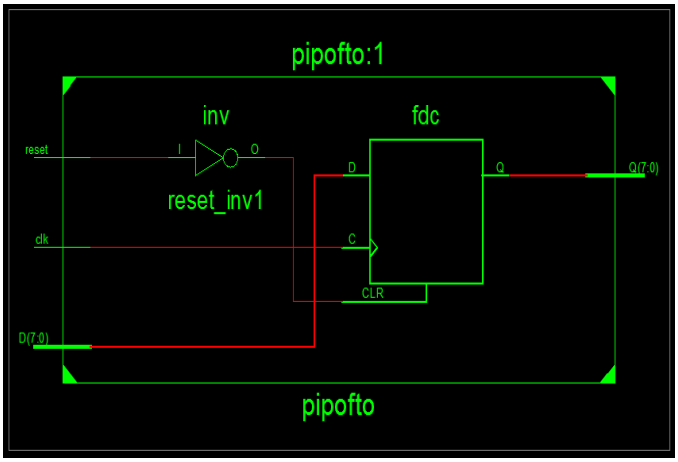


Figure 3. 8 bit PIPO RTL schematic view in Xilinx

Here in above RTL schematic the input is D (7:0) is 8 bit parallel input and Q(7:0) is 8 bit parallel output. The clock signal is given by "clk" and reset is inverted and connected to clear of the flip flops. "fdc" is the group of 8 flip flops, whose output is Q(7:0) i.e. 8 bit parallel output.

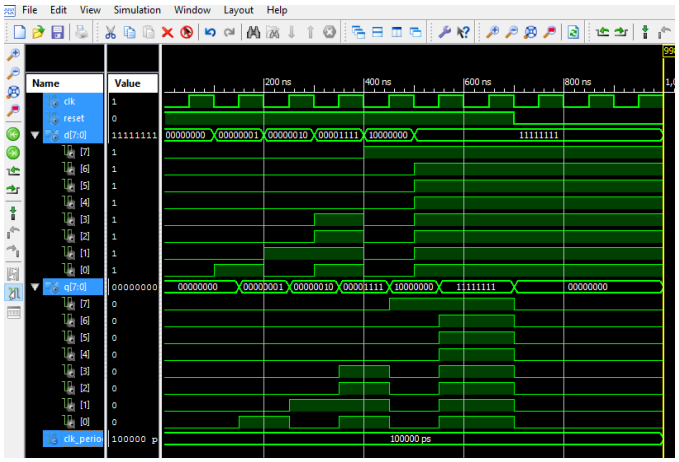


Figure 4. Test-bench simulation of 8 bit PIPO register created in Xilinx

Here shows in above figure, the first signal shows is system clock signal, second signal is reset given to HIGH, third signal is 8 bit input signal and fourth signal is 8 bit output signal. There is one clock cycle delay between input and output signal as shown in above figure.

C. 3 bit SIPO Register

3 bit serial in parallel out shift register is used to store the three output of the comparator. The 1 bit input signal is din and the 3 bit output is given by dout (2:0). The clock is given by clk input signal. The output of the SIPO register is come at every positive edge of clock signal.

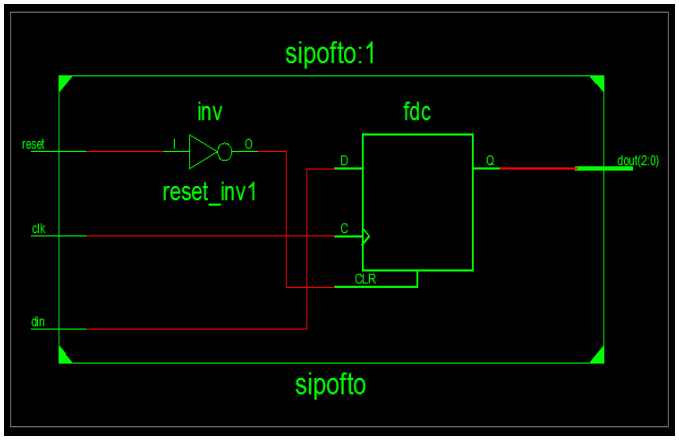


Figure 5. 3 bit SIPO RTL schematic view in Xilinx

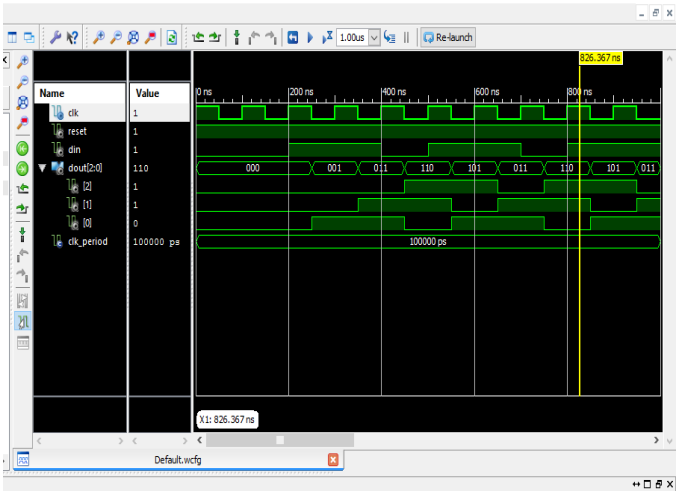


Figure 6. Test-bench simulation of 3 bit SIPO register created in Xilinx

The above figure shows the test-bench simulation of 3 bit SIPO register. The first signal is clock signal , second is reset given to active HIGH, third signal is input signal and the fourth signal is 3 bit parallel output signal.

D. CVSD Level select Algorithm

The CVSD modulator consist an 8 bit comparator for comparing i/p signal with reference signal, 3 bit sipo (serial in parallel out) for detecting slope overload, 8 bit pipo (parallel in parallel out) for providing 1 clock cycle delay , overload detect and level select algorithm is used for selecting the variable step size. The present input compared with previous level selected output in 8 bit comparator. The comparator output is a digital encoded output which is 1 bit compressed output of 8 bit A to D input. If the output of the comparator is HIGH i.e. 1 then the 8 bit selected input is increased by one bit. If the output of the comparator is 0 the 8 bit selected input is decremented by 1 bit. If the output of comparator is "111" or "000" the previously selected input is incremented or decremented by some constant respectively. The below figure is RTL schematic of CVSD level select algorithm.

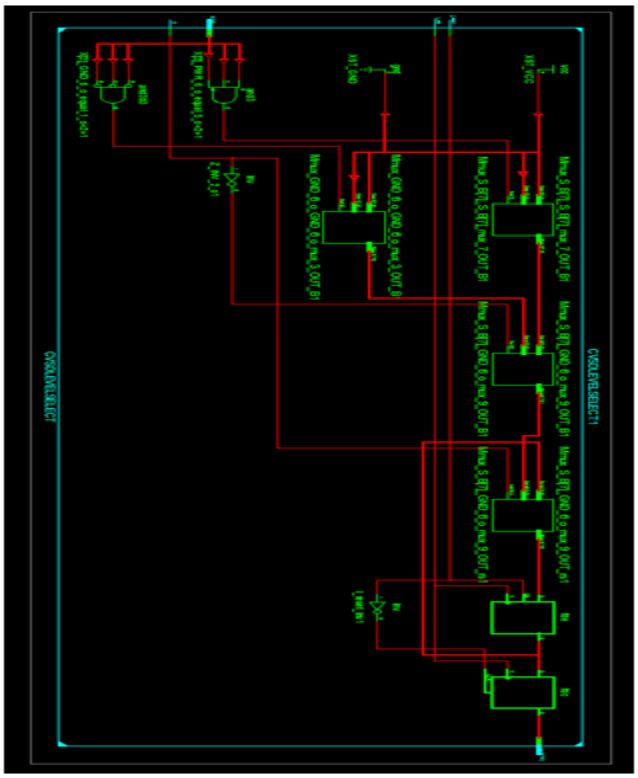


Figure 7. RTL view of CVSD level select module created in Xilinx

E. CVSD Top Module

The CVSD top module is designed by stuctural modeling in VHDL. The below figure is RTL schematic of combinations of all the modules. The CVSD encoder consist an 8 bit comparator for comparing i/p signal with reference signal, 3 bit SIPO (serial in parallel out) for detecting slope overload, 8 bit PIPO (parallel in parallel out) for providing 1 clock cycle delay , overload detect and level select algorithm is used for selecting the variable step size. The present input compared with previous level selected output in 8 bit comparator. The comparator output is a digital encoded output which is 1 bit compressed output of 8 bit A to D input. This encoded output is coming at every trailing edge or falling edge of the CLOCK signal. Here in below figure shows, each block is CLOCK dependent, so the data rate of CVSD is defined by the CLOCK. So by varying the CLOCK frequency we can vary the data rate.

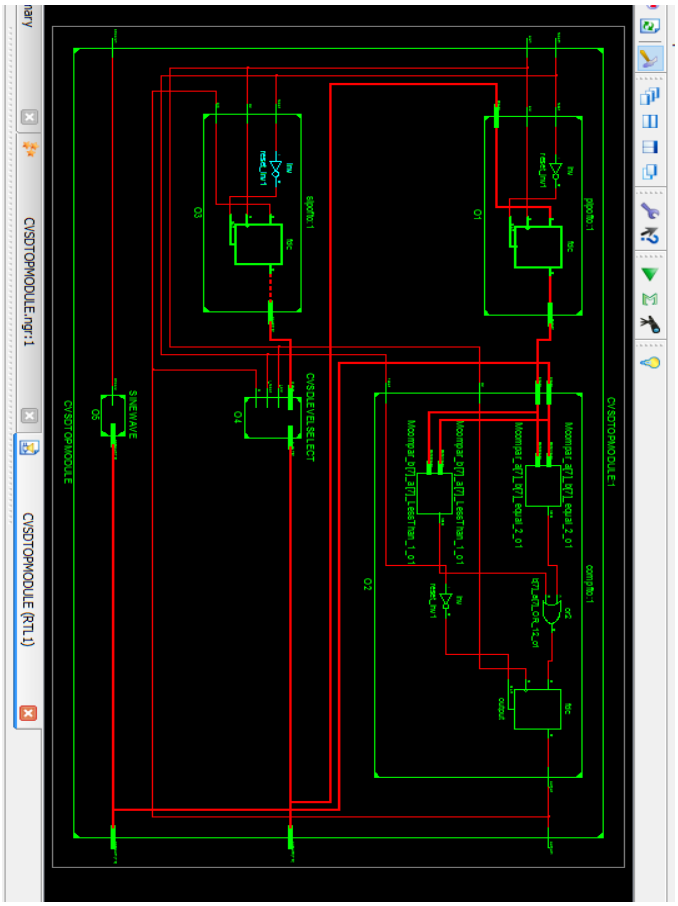


Figure 8. RTL view of CVSD TOP module created in Xilinx

III. SNR CALCULATION

Signal to noise ratio (SNR) is one of the most fundamental metrics used in signal processing. It is defined as the ratio of signal power to noise power expressed in decibels (dB).

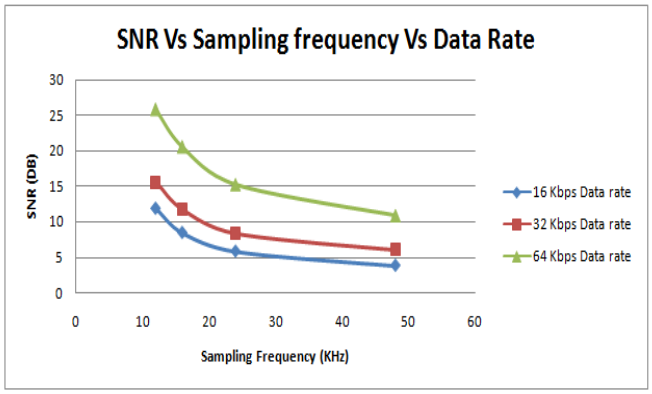
$$SNR = 10\log_{10}\frac{variance\ (Input)}{variance(Output - Input)}$$

(or)

$$SNR = 10\log_{10}\frac{\sum_{n=1}^{N}(x_n)^2}{\sum_{n=1}^{N}(x_n - \hat{x}_n)^2} \quad \text{.....[7,8]}$$

Here,

X(n) = Samples of i/p signal
X^(n) = Samples of Reconstructed O/P signal



The SNR calculated at different data rates at different frequencies. Here if we increase the data rate of the CVSD system the signal to noise ratio is increases and if we increase the sampling frequency of the input signal then comparison of the comparator is decreases so signal quality at output of decoder is decreases so SNR is decreases.

IV.CONCLUSION

The Digital design of CVSD codec algorithm is created using VHDL Codes. VHDL is commonly used to write text models that describe a logic level circuit. Here Various RTL Schematics of the Modules are designed in Xilinx. In digital system design method, register-transfer-level (RTL) schematic is a design perception, which models a synchronous digital circuit in terms of the flow of digital signals. CVSD soft core can be easily implemented on any telemetry processor so that one can easily embedded digitized audio signal on a single frame and send it to ground station.

CVSD can be used in tactical aircraft intercom system. CVSD soft core has huge economical advantage for low power audio signal processing.

CVSD is internationally acceptable algorithms for digital transmission of audio signal. This soft core is portable for defence system.

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