© 2017 IJSRSET | Volume 3 | Issue 8 | Print ISSN: 2395-1990 | Online ISSN : 2394-4099
Themed Section : Engineering and Technology

A Study of Design and Performance Analysis of CMOS Integrated Receiver System for Millimeter Wave Applications

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ABSTRACT

To meet the demands for the multi-band, multi-mode wireless standards in the current market, a highly integrated wireless receive is desired. Technology developments have made CMOS a strong candidate in high-frequency applications because of its low power, low cost and higher-level integration. This paper will present the different works which have been already done and the future aspects.

Keywords : CMOS, LNA, Millimeter wave, Gain, Noise figure, Bandwidth

I. INTRODUCTION

The millimetre-wave region of the electromagnetic spectrum corresponds to radio band frequencies of 30 GHz to 300 GHz and is sometimes called the Extremely High Frequency (EHF) range. The high frequency of millimetres waves as well as their propagation characteristics makes them useful for a variety of applications including transmitting large amounts of computer data, cellular communications, and radar. Every kind of wireless communication, such as the radio cell phone, or satellite, uses specific range of wavelengths or frequencies. Each application provider has a unique "channel" assignment, so that they can all communicate at the same time without interfering with each other [1,2]. Using CMOS technology the following results have been obtained and contributed significant development in technology.

II. PROPOSED CMOS INTEGRATED RECEIVER SYSTEM

In 2004, Doan et al. [7] presented some of the earliest work in the use of CMOS for highly integrated 60-GHzsystems. They demonstrated that adequate performance for 60-GHz operation in CMOS is not attained for all transceiver components if a technology node older than 0.13 µm, such as 0.18 µm, is used. They also demonstrated that optimal finger width for a multi finger 60-GHz transistor is approximately 1 µm. Their results showed transmission lines would need to be extensively used in highly integrated mm-wave transmitters for 60-GHz applications due in part to their ability to clearly define current return paths, and also because on-chip mm-wave transmission lines are primarily characterized by their inductive quality factor instead of a capacitive quality factor. The result of Doan et al.'s [7] transmission line investigation also showed that coplanar waveguide transmission lines should be used instead of micro strip lines due to higher inductive quality factors.

In 2005, Shigematsu et.al [8] developed a 27 to 40-GHz tuned amplifier and a 52.5-GHz voltage-controlled oscillator using 0.18 µ m CMOS. The line-reflect-line calibrations with a microstrip-line structure, consisting of metal-1 and metal-6, was quite effective to extract the accurate -parameters for the intrinsic transistor on Si substrate and realized the precise design. Using this technique, they obtained a 17-dB gain and 14-dBm output power at 27 GHz for the tuned amplifier. they also obtained a 7-dB gain and a 10.4-dBm output power with a good input and output return loss at 40 GHz. Additionally, they obtained an oscillation frequency of 52.5 GHz with phase noise of 86 dBc/Hz at a 1-MHz offset. These results indicate that their proposed technique is suitable for CMOS millimetre-wave design. In 2006, Sun K, et al. [9] A noise optimization formulation for a CMOS low noise amplifier (LNA) with on-chip low- inductors was presented, which incorporates the series resistances of the on-chip low-inductors into the noise optimization procedure

explicitly. A 10-GHz, LNA was designed and implemented in a standard mixed-signal/RF bulk 0.18 µm CMOS technology based on this formulation. The measurement results, with a power gain of 11.25 dB and a noise figure (NF) of 2.9 dB, show the lowest NF among the LNAs using bulk 0.18 µm CMOS at this frequency.

In 2007, Mitomo et al. [30] of Toshiba and Maruhashi et al. [31] of NEC reported 60-GHz receivers and transmitters that incorporated on-chip or in-package antennas. These designs foreshadow future systems on chip in which many or all wired interconnects become wireless. Mitomo et al. [30] on-chip receiver design in 90-nm CMOS used only 2.4 mm to 1.1 mm excluding pads and included a one-stage LNA, down conversion mixer, and PLL synthesizer. The receiver required only 144 mW of power. They did not measure the gain of their on-chip dipole antenna. Maruhashi et al. [31] reported separately packaged receiver and transceiver modules in AlGaAs / InGaAs over Low-temperature Co-fired ceramic substrate each of which occupied roughly1 to 2 cm per side. The receiver incorporated a three-stage LNA down converter and slot antenna, while the transmitter included a two-stage PA, up converter, and slot antenna. Their use of LTCC allowed an antenna gain of 4 dBi. The high antenna gain using an LTCC substrate, when compared to typical gains for on-chip antennas over lossy CMOS substrates without compensating structures such as lenses, illustrates the difficulty of achieving high gains for antennas on CMOS.

In 2009, Dawn et al. [32] of the Georgia Institute of Technology presented two IF up conversion transmitters in 90-nm CMOS. The first used a single-ended transmitter design intended for low-power applications and occupied 1.4 to 1.5 mm, while the second transmitter was a differential design for high-performance applications that occupied 1.3 to 1.5 mm. The single-ended transmitter contained a push–push VCO, LO amplifier, mixer, and three-stage PA. It had a gain of 8.6 dB, P1dB compression point of 1.5 dBm and consumed 76 mW. The high performance differential transmitter included a cross coupled VCO, Gilbert-cell mixer, marchand balun, and three-stage PA. It had a gain of 12.4 dB and a P1dB compression point of 4.1 dBm.

In the same year, Parsa et al. [10] of UCLA also published a 90-nm CMOS near-complete transceiver that occupied 0.19 to 2 and consumed only 36 mW as a receiver and 78 mW as a transmitter. Their design was based on a new Bhalf-RF architecture that allowed a 30-GHz LO to be used to convert a baseband signal to 60 GHz.

In 2009, Arsalan M et al.[11] Presented the smallest reported 5 GHz receiver chip (1.3 mm2) with an on-chip antenna in standard 0.13 µ CMOS process. The miniaturization was achieved by placing the circuits inside a meandered antenna. The on-chip antenna was conjugately matched to the low noise amplifier (LNA) over a wide frequency range. The design methodology for co-design of the on-chip antenna and LNA was described. The LNA was completely differential, consumed only 8 mW of power and provides a gain of 21 dB.

In 2012, Boppel S. et al. [12] presented a paper on field-effect-transistor-based terahertz detectors for the operation at discrete frequencies spanning from 0.2 to 4.3 THz. They implemented using a 150-nm CMOS process technology, employ self-mixing in the n-channels of the transistors and operate well above the transistors' cut off frequency. The theoretical description of device operation by Dyakonov and Shur is extended in order to describe the device impedance, responsivity, and noise-equivalent power for a novel detection concept, which couples the signal to the drain. This approach enables quasi-static (QS) detection and calibration of the detectors. The different transport regimes (i.e., QS, distributed resistive, and plasmonic mixing) and their transitions were theoretically discussed and experimentally accessed. Responsivity values of 350 V/W at 595 GHz, 30 V/W at 2.9 THz, and 5 V/W at 4.1 THz were reported at 0.595 THz, they determined the optical noise equivalent power (NEP) to be 42 pW Hz; at 2.9 THz, the value is 487 pW Hz. All values were reported for optimum gate bias with respect to NEP at 295 K. For 0.595 THz, theory predicts a NEP value at threshold as low as 2 pW Hz for ideal coupling of the radiation.

In May 2015, Kumar S. et al. [13] worked on fully integrated single chip receiver system in the area of millimetre wave (MMW) applications. In this paper, the integration of antenna, filter and CMOS low noise amplifier (LNA) was proposed which provides a new

tri-design receiver system for MMW communication networks. A three-stage CMOS LNA was designed and integrated with co-design of filter and rectangular micro strip antenna which relaxes 50 X impedance matching constraint for designing at 40 GHz. Moreover, the new tri-design technique heavily improves the overall system integration, minimizes the noise and reduces the chip area and thus saving overall cost of the system. A three-stage CMOS LNA design is simulated and layout using 90 nm CMOS design kit in ADS.v.12. The simulation result of CMOS LNA showed an achievement of 3.8 dB noise figure, 15.8 dB gain and -28 dB of return loss using proper impedance matching network. In addition, a theoretical analysis of three-stage CMOS LNA without using input–output matching network was done for the optimization of noise figure. A co-design of filter and patch antenna was also analyzed and integrated with CMOS LNA circuit. Finally, tri-design of receiver system demonstrates a peak gain of 25 dB and noise figure of 2.8 dB using proposed method.

In May 2015, Kumar S. et al. [14] proposed a co-design approach for a new asymmetric rectangular cross shaped slotted patch antenna with low noise amplifier that occupies 17.2–25.8 GHz wide-band for SDR applications. This co-design approach minimizes the chip area and noise and also improves integration system over the bandwidth of 8.6 GHz. Three different architectures have been designed in this work. Firstly, a two stage CMOS CG–CS LNA was designed using a technique of series–parallel resonant network as an input matching network and as inter-stage matching network between CG and CS LNA. In second architecture stage, a rectangular shaped micro strip antenna was designed and a slot of asymmetric cross shape is cut on the patch antenna. In third architecture the slotted antenna was integrated with low noise amplifier in order to form a co-design approach in which series–parallel resonant network was used as a band pass filter between slotted patch antenna and LNA. A two-stage CMOS LNA design is simulated and layout was made using foundry design kit for the TSMC 65 nm CMOS process in ADS.v.12. A simulation result of LNA achieved S11 of -21.4 dB with gain ranging from 7.4 to 21.3 dB over the wide-band of 19.1–28.8 GHz. The slotted antenna achieves S11 of -19 dB at 26 GHz and covers frequency range of 20.1–27.8 GHz with good radiation and receiving patterns. This codesign approach was analysed considering the 50 X impedance matching throughout the design and simulated on the platform of ADS.v.12. The best achievement of proposed codesign approach was reduced noise figure which was most suitable for SDR applications.

In 2016, Pyo G. Et al. [15] presented a CMOS transceiver IC for single-antenna frequency-modulated continuous wave (FMCW) radar. Since transmitter (Tx) leakage is critical in a single antenna radar with CMOS technology, a comprehensive leakage cancelling technique was proposed. It was able to cancel all the leakages caused by antenna reflection, asymmetry of a balanced structure, and lossy substrate without additional power or area. Even-order harmonic leakages from the power amplifier (PA) are also reduced by an even-harmonic filter, which is implemented simply by removing the real ground from the symmetrical point of the PA output transformer. Matching networks are simplified by using a modified coupler structure. A low-noise combining amplifier is used to make the combining circuit compact. As a result, the transceiver achieves the output power of −1.6 dBm, the phase noise of −105.44 dBc/Hz at 1MHz offset, the receiver (Rx) gain of 15.3 dB, and the noise figure of 11.6 dB. Tx leakages are cancelled so that the isolation between Tx and Rx is 47.3 dB. The chip consumes 74.1 mA from a 1.5-V power supply. Despite the high integration level, the chip area including pads is 1.7 mm × 0.9 mm. A K-band FMCW radar module with a single antenna was implemented with this chip.

In 2016, [16] Elkholy M. Et al. presented a tunable integrated electrical balanced duplexer (EBD) as a compact alternative to multiple bulky surface acoustic wave (SAW) and bulk acoustic wave (BAW) duplexers in third-generation (3G)/fourth-generation (4G) cellular transceivers. A balancing network created a replica of the transmitter (TX) signal for cancellation at the input of a single-ended low-noise amplifier (LNA) to isolate the receive path from the TX. The proposed passive EBD is based on a cross-connected transformer topology without the need of any extra baluns at the antenna side. The balancing network enables a single-ended LNA with reliable high TX power operation up to 22 dBm by alleviating the common-mode coupling. The duplexer achieves around 50-dB transmitter–receiver (TX-RX) isolation within a 1.6–2.2-GHz range. The cascaded noise figure (NF) of the duplexer and LNA was 6.5 dB, and TX insertion loss (TXIL) of the duplexer is about 3.2 dB. The duplexer and LNA were implemented in a 0.18- m CMOS process and occupy an

active area of 0.35 mm. This work has presented a step forward to replace today's band-specific SAW/BAW duplexers with a fully integrated low-loss wideband duplexer.

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