© 2017 IJSRSET | Volume 3 | Issue 8 | Print ISSN: 2395-1990 | Online ISSN : 2394-4099
Themed Section : Engineering and Technology

Designo Reversible Logic Circuit Using Quantum Dot Cellular Automata

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ABSTRACT

Conservative logic is a logic which displays the assets that there's identical range of the inputs in addition to inside the output. It may be reversible or irreversible in nature. Reversibility is not anything but the circuit reveals one-to-one mapping between input and output vector, and also represents for each input vector there is an precise output vector and vice versa. Reversibility is specially favoured due to the fact it is able to offer the method for designing low power circuits. Unlike computation mechanisms that contain the switch of electrons, as in CMOS gates, QCA computation does not involve electron switch between adjoining QCA cells. Hence power dissipation could be very less in circuits designed with QCA cells. Therefore it is essential to keep in mind power as an critical parameter during the QCA layout technique. The predominant benefits of this generation are lesser electricity dissipation, advanced velocity and dense systems. In this undertaking layout of reversible combinational circuits like ALUs which is designed with new gates, MUX, Adders, primarily based on QCA era is proposed to provide benefits like reduction in no of quantum value, garbage outputs, complexity of gates, location.

Keywords: Combinational Circuits, Arithmetic Logic Unit (ALU), Reversible logic, QCA, Quantum Cost, Garbage Outputs, Constant Inputs.

I. INTRODUCTION

The digital systems plays high role in today's digital world as a reason power consumption is main concern. So reducing the power consumption is important criterion in design. The irreversible circuits, there is no inevitability of input according to output, and may cause information loss due to which power consumption increases. K T*log2 joules of heat energy is generated, where k is Boltzmann's constant and T is the absolute temperature at which computation is performed [1]. The one of the best solution for this power reduction is reversible logic [2]. Also, Bennett [3] showed that in order to keep a circuit a way from dissipating any power, it had to be composed of reversible gates. The present irreversible computation depends on the number of operations where the information loss takes place e.g. let us consider logic AND gate which have two inputs and single output, the two inputs will be either be 1 or 0 and the output depends upon the two inputs [4]. For the inputs the value is logic 1,which acquires output 1 else 0.Every time when the gate's output is 0 we lose information, because we do not know that the input lines are in which of the three possible states (0 and 1, 1 and 0, or 0 and 0). In detail, several logic gates that has more input lines than the output lines predictably discards information, because we cannot figure out the input from the output. The continuous scaling down of feature size has pushed CMOS technology to approach its convenient and speculative limits [5]. Lot of research efforts at nano scale is in progress to explore alternate viable technologies for future integrated circuits (ICs). While exponential decreasing the feature size in CMOS technology, devices are getting more prone to high leakage current and also getting more sensitive to circuit noise [6]. Landauer computed that in each irreversible operation the heat generated will be in the order of KT, the power indulgence is mainly due to the erasure of the intermediate states that are been used in the computation process. When one bit of data gets erased means the energy dissipation will be in terms of KTln2, where K is

the Boltzmann's constant and T is the absolute temperature [7].

QCA provides an alternative to the silicon technology.QCA based circuits have the improvement of elevated speed, high integrity and power reduction [8]. Also QCA circuits have the advantage of high parallel processing.

QCA is emerging as a potential technology that could be used in future computing circuits/systems replacing existing Silicon technology. It provides a new computing and information transformation paradigm [9]. It is a transistor less technology that uses a square nanostructure called QCA cell comprising of 4 quantum dots [10]. Two free electrons are introduced in a four quantum dot based QCA cell which can tunnel amongst the quantum dots and take seat in any one of them. The two free electrons settle into two stable states within QCA cell that are used to encode two binary states in digital circuits. QCA cells are arranged in arrays for a particular computation and converse with each other by Coulomb interactions. The alignment of electrons at edges of array provides the computational output. The alignment of QCA polarizations in circuit is managed by applying an external clock and functions according to the rules of Boolean algebra [11].
QCA cells execute computation by interacting coulombically with adjacent cells to persuade each other's polarization. A high-level diagram of a four-dot QCA cell appears in Figure 2.1. Four quantum dots are to be found to form a square. Quantum dots are small semi-conductor or metal islands with a diameter that is small adequate to make their charging energy greater than kBT [12]. If this is the case, they will trap individual charge barriers.

Exactly two mobile electrons are loaded in the cell and can move to unusual quantum dots in the QCA cell by means of electron tunneling.

Columbic repulsion will cause the electrons to occupy only the corners of the QCA cell resulting in two specific polarizations [13].

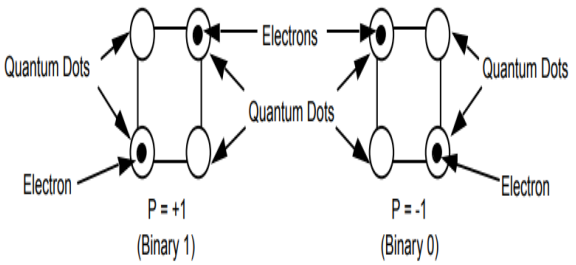

Figure 1. QCA Polarization cells with +1 for logic 1 and -1 for logic 0.

An ALU is incredibly key part of a computer. It is sincerely considered as the heart of a pc. It makes it possible for the laptop to perform many other arithmetic and common sense capabilities. On account that every laptop needs to be ready to do these features, they are at all times integrated in a CPU [14]-[15]. A easy ALU contains two operands, one manipulate signal to select the operation to be carried out and one output sign to provide the outcomes of preferred operation. Reversible ALU is designed for modular arithmetic operations aside from logical operations.

II. PROPOSED REVERSIBLE GATES

The Proposed Gates satisfies the property of Reversibility and Universality. Reversibility represents the precise mapping between the input and the output bit vectors [3].Universality represents reversible in the realization of AND, OR and now not operations. The proposed buildings undergoes reversibility via execution and satisfies the property of Universality via executing AND, OR and no longer operations. This novel gates with special operation aid in design Arithmetic and logical unit. The illustration of the unconventional reversible gate called Reversible Gate 1 (RG1), Reversible Gate2 (RG2) and Reversible Gate 3(RG3); Reversible Gate 4 (RG4) together with their output performance is mentioned in Figure 1, Figure 2, Figure 3, and Figure 4.

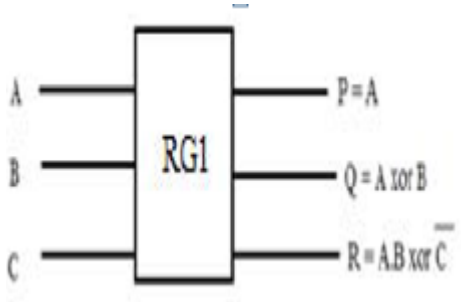

Figure 2. Reversible gate1

The beyond shown Figure is one of the proposed reversible gates. The number of inputs and number of outputs will be equal for reversible gates. Which represents the operations for the inputs A, B, C as P is A, Q is A XORB, and R is AB XOR ~ C.

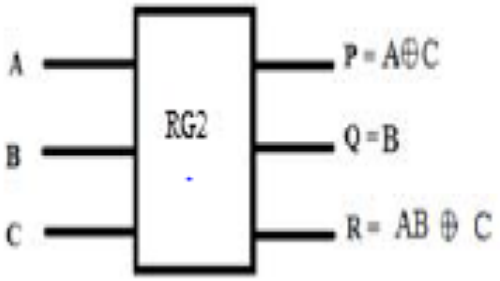

Figure 3. Reversible gate 2

The reversible gate2 (RG2) shows the functionality of P is A XORC, and keeping output same as input for Q, R is A AND B XOR C.

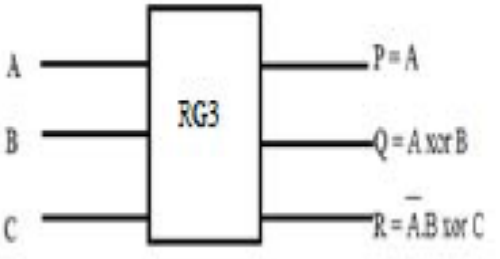

Figure 4. Reversible gate3

The reversible gate 3 performs operations as output P is passed by the input A, Q is A XOR B, and R is ~ A AND B XOR C. The below gate shows the operation for reversible gate 4 P is A+B xor C , Q is B and R is AB xor C.

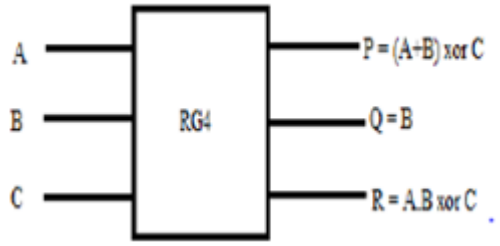

Figure 5. Reversible gate4

These gates will be worn in the ALU design to obtain Significant reduction in the reversible logic parameters.

HNG Gate, It is a 4x4 gate and its logic circuit is as shown in the figure1. It has quantum cost six. It is used for designing adders like ripple carry adder. It reduces the garbage and gate counts by producing the sum and carry in the same gate.

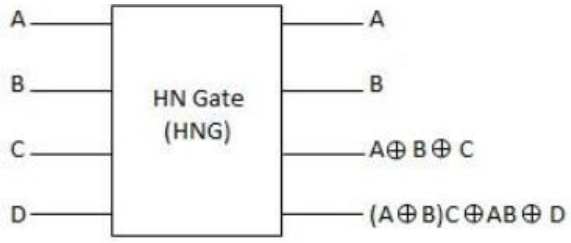

Figure 6. HN gate

III. ARCHITECTURES IN QCAD

A. Multiplexer Design

The Multiplexer design is based on the majority configuration of the QCA cells. The Multiplexer design is as follows:

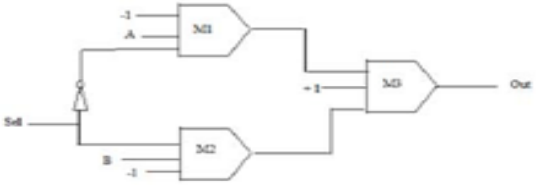

Figure 7. MUX with majority gate

Figure 7 shows the Multiplexer design based on the majority configuration of the QCA cells. Three majority gates and one inverter are needed to construct the multiplexer. The majority gate representation of the function is as follows:

F = M3 (M1 (Sel,A,0), M2 (Sel,B,0),1)

Where M1, M2, M3 denotes the majority cells and 'Sel' denotes the select lines. The input and the constant cells are placed in a proper way so that the outputs of the two majority gates M1 and M2 are propagated to the third majority gate M3 (OR operation) with equal time delay.

B. Design of ripple carry adder

The design of ripple carry adder is based via cascading full adders (FA) blocks in series. Single full adder is accountable for the addition of two binary digits at any stage of the ripple lift adder. The carryout of one stage is fed instantly to the lift-in of the continuing stage. Even though this is a uncomplicated adder and can be

used to add unrestricted bit size numbers, it's nevertheless no longer very efficient when tremendous bit numbers are used. One of the extreme drawbacks of this adder is that the delay raises linearly with the bit length. The conventional 3 bit ripple carry adder is shown in the figure. In reversible ripple carry adder all the full adders are changed with the aid of HNG gate. Reversible eight bit ripple elevate adder s proven in determine. The quantum rate is 48, constant input (CI) s 3, garbage output (GO) is 6 and gate count (GC) is three.

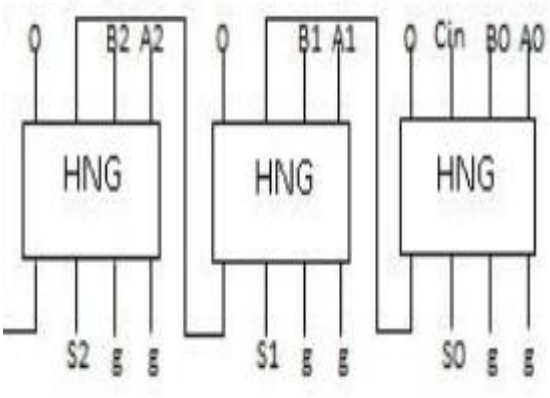

Figure 8. Ripple carry adder

C. Arithmetic and Logical unit design

In the Processor architecture the ALU is considered as the heart of the system. An arithmetic and logical unit should be capable of producing larger number of possible arithmetic and logic functions. Based on the reversible gate structure the ALU design can be made remarkably, the reversible gates should maximize the operations of arithmetic and logical unit. But the cost of the circuit selects lines used for designing the circuit garbage outputs of the circuit design, circuit delays must be reduced, to ensure this at each stage verification should be made whether the reversibility is present in each and every part of the design and the outputs should propagate in a manner to achieve the correct operation of the circuit and also to achieve reversibility of the design.

a. Functions of Proposed Arithmetic Unit

The Arithmetic unit is responsible for handling the Arithmetic operations executed by the program. The proposed arithmetic unit is designed based on the novel reversible gates. The functions of the proposed arithmetic unit are shown in Table 1.

Table 1. Functions of arithmetic unit

Control Inputs			Output	Results
C_0	C_1	C_2		
0	0	0	B	Transfer B
0	0	1	B+1	Increment B
0	1	0	A + B	Addition
0	1	1	A + B + 1	Addition with carry
1	0	0	A + B	1's complement subtraction
1	0	1	A + B + 1	2's complement subtraction
1	1	0	B-1	Decrement B
1	1	1	B	Transfer B

The output function is realized based on the equation 1,

OUT = (AC0+AC1) xor B xor C2 --------- (1)

Where A, B are the inputs given to the reversible gates and C0, C1, C2 are the control inputs. Based on the control inputs the arithmetic functions like transfer operation, increment, decrement, addition, addition with carry, 1's complement subtraction, 2's complement subtraction etc are been performed for the ALU operation.

b. Design of Arithmetic Unit Based On Novel Reversible Gates

The design of Arithmetic Unit composes of five Reversible Novel structures. The design constitutes of three Reversible gate2 (RG2), two Reversible gate3 (RG3) and one Reversible gate4 (RG4). Its corresponding Quantum Cost is 32. The Number of Garbage outputs used here is 6. The number of constant inputs employed here is 1.

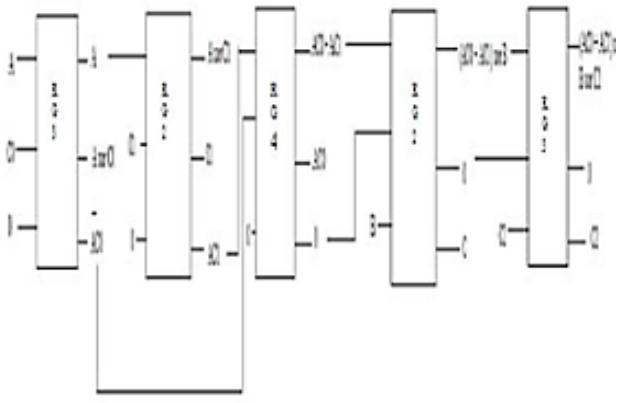

Figure .9 Design of Arithmetic Unit

The Figure 9 shows the design of Arithmetic unit. The operation of Arithmetic unit is as follows initially for theRG3 gate the inputs given will be A, C0 and 0. C0 is the control inputs given to the arithmetic unit design and

0 is the constant inputs in the design. The resultant outputs from the RG2 gate is A, A xor C0, A'C0. The output A is propagated to the next reversible gate RG2, where the second output A xor C0 is considered as the garbage output (that is unused output in the design). Hence the next reversible gate has an input of A, C1, 0 where c1 is the control inputs and 0 is the constant inputs the procured output will be A xor C1, C1, AC1, where A xor C1 and C1is the garbage output and AC1 is propagated to the next Reversible gate. The next reversible gate used is RG4, the inputs given to RG4 is A'C0 which is the output received from the RG3 is propagated to this RG4 gate as an input and the second input will be AC0 which is the output obtained from the RG2 gate is propagated as the input toRG4 and the another input will be 0 the corresponding outputs obtained from the reversible gate4 is AC0+AC1,A'C0 and 0. Here A'C0 is considered as the garbage output function. The outputs AC0+AC1 and 0 is propagated back to the next stage of the process. The next reversible gate2 takes the inputs AC0+AC1, 0 and B and performs the corresponding operation with respect to the gate and procures the outputs. The received output from RG2 is (AC0+AC1) xor B. Here the garbage output obtained is C1. At the final stage the outputs (AC0+AC1) xor B and 0 is propagated to the next stage of the RG2 with an additional input of C2, where C2is the control inputs. The obtained output from the RG2 is(AC0+AC1) xor B xor C2, 0, C2.The outputs C2 and 0 is taken as the garbage outputs. For example, when the control input C0, C1, C2 is equal to111, the output from RG3 is A', the output from RG2 is A, by giving this two input to the RG4 gate the respective output will be A'+A this function is given as the input to the RG2 gate, the obtained output is B. Then this output is propagated to RG2 as the input after getting processed, the output obtained from RG2 is B. Therefore for the control input combination of 111 the transfer operation (B) is carried out.

c. Functions of Proposed Logic Unit

The Logical unit is the another important constituent in the Central Processing Unit as it is responsible for handling the logical operations executed by the programmer. The proposed design of logical unit design is based on the novel reversible gates. The functions of the proposed logical unit are shown in Table 2.The functionalities of Logical unit can be designed by the output equation as follows:

OUT = A'B'C0+AB'C1+A'BC2+ABC3 ---- (2)

Table 2. Functions of Logical Unit

Control Inputs				Output	Results
C0	C1	C2	C3		
0	0	0	0	0	-
0	0	0	1	A.B	AND
0	0	1	0	B	COPY
0	1	0	1	A	COPY
0	1	1	0	A xor B	XOR
0	1	1	1	A+B	OR
1	0	0	0	(A+B)'	NOR
1	0	0	1	(A xor B)'	Equal
1	0	1	0	A'	NOT
1	1	0	0	B'	NOT
1	1	1	0	(A.B)'	NAND
1	1	1	1	1	Constant

The value of C0, C1,C2,C3 is taken as the control inputs based on the control input values that is by changing the inputs combinations of 0's and 1's the

Respective logical functions can be obtained. The obtained logical functions from the above control inputs are AND, COPY, XOR, OR, NOR, Equal, NOT, NAND and Constant.

d. Design of Logic Unit Based On Novel Reversible Gates

The proposed design of logical unit is based on the proposed novel reversible structures. The logical unit

Comprises of nine novel reversible gates. Its corresponding Quantum Cost is 32. The Number of Garbage outputs used here is 6. The number of constant inputs employed here is 1.

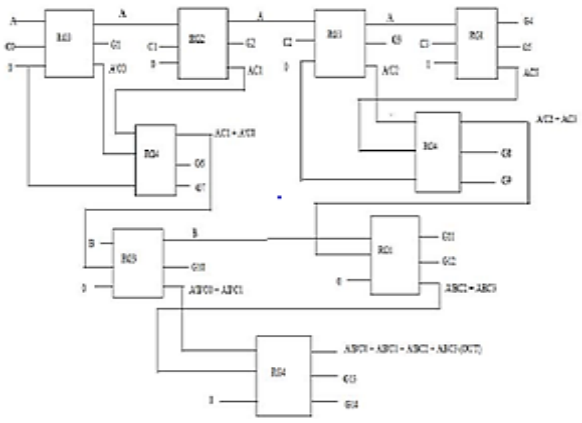

Figure.10 Design of Logic Unit

The Figure 10 depicts the design of Logical Unit. The operation of Logical unit is as follows: Initially the input applied to the reversible gate3 is A, C0 and 0, where C0 is the control inputs After proceeding over the

RG3 gate operation the corresponding obtained output will be A,A'C0 and one Garbage output (unused function in the circuit). The obtained output A from the RG3 gate is given to the next reversible gate RG2. The RG2 which takes the input A, C1, 0. After preceding over RG2operation the obtained output function will be A, AC1 and one Garbage output. The RG4 takes two inputs that isA'C0 from RG3 and AC1 from RG4 the obtained output will be A'C0+AC1 and which includes two garbage outputs. The obtained output from RG2 A is given as the input to the RG3 gate with an additional input of C2 and 0, where C2 is the control input and 0 is the constant input to the reversible gate. The obtained output from RG3 is A, A'C2 with an additional of one garbage output. Next the output from RG3 is given to RG1 and it takes the input of C3 and 1, Where C3 is the control input and 1 is the constant input. The obtained output from RG1includes two garbage outputs with an additional output ofAC3. The outputs from RG3 and RG1 gate A'C2 and AC3 Respectively is given to the RG4 gate with an additional input 0 obtained from RG3 gate. The obtained output from RG4 is A'C2+AC3 with an additional output of two garbage's. Further one of the output from RG4 (AC1+A'C0) is given to the RG3 gate with an additional input of B and 0, where 0 is the constant input provided to the gate. The output of RG3 gate is B, A'B'C0 + AB'C1with one garbage output. At the next stage the output obtained from RG3 is given to RG1 and the output obtained from

A'C2+AC3 is given as the input to RG1 with the additional input of 0. The obtained output fromRG1 is A'BC2+ABC3 with the two garbage outputs. At the next stage the outputs from RG3 and RG1A'B'C2+AB'C1 and A'BC2+ABC3 respectively given asthe input to RG4 gate with an additional constant input of0.The additional output from the RG4 includes additional two garbage's. Hence the total reversible gate required to design the logical unit will be 9. The total garbage outputs obtained is 14. The number of constant inputs employed in the logical unit design is 2 as the constant inputs are getting propagated to the various reversible gates in the circuitry. C0, C1, C2, C3 are the control inputs in the design corresponding to the control inputs the logical functions can be preceded. The control inputs should be increased to perform more logical operations. For example, for the control input combination 0001, from the gates RG3, RG2, RG1 only the garbage values will be generated. From the gate RG4 the output will beAC3, this output is further given to RG1 which gets multiplied by B and the corresponding output from RG1 is ABC3, this function is given as the input to the RG4gate with the other inputs which is generated as garbage's. Hence the final output obtained from RG4 gate is AB that is the multiplication operation is carried out for the corresponding control input combination of 0001.The design of Arithmetic unit and Logical unit should be integrated together in order to form a complete design. The integration can be done by using the multiplexer. Where the multiplexer receives the inputs from the arithmetic and logical unit and depending upon the select lines the required operations will be performed.

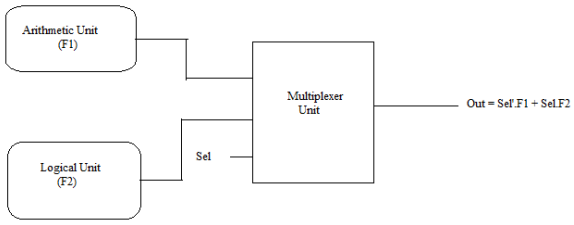

Figure 11. Integration of Arithmetic and Logical Unit

Figure 11 shows the Integration of Arithmetic and Logical Unit. The multiplexer design takes the input F1 from the arithmetic unit and F2 from the logical unit and sel is the select lines. The output of the multiplexer will be satisfying the equation 4.

OUT = SEL'.F1 + SEL.F2 ------ (4)

Table 3 . Integration of ALU in MUX table

SEL	OPERATION	OPTIONS
0	Arithmetic operation	Add, Sub, Transfer, Complement etc…
1	Logical operation	AND, XOR, OR, COPY etc…

When the select line is equal to 1 the Logical operation will be performed. When select line is equal to 0 the Arithmetic operation will be performed. On selecting F1 the arithmetic operations like transfer operation, increment, decrement, addition, addition with carry, 1's complement subtraction, 2's complement subtraction etc are been performed. On selecting F2 the logical operations like AND, COPY, XOR, OR, NOR, Equal, NOT, NAND, Constant is performed. As compared to the existing multiplexer design the multiplexer design based on the majority gate configuration is comparatively better in terms of the number of majority gates used as the multiplexer design is based upon the majority cell configuration. The one bit ALU is

extended to any number of bits by integrating the multiplexer design. The fixed point ALU can be achieved by this integration of the arithmetic unit and logical unit by using multiplexer.

IV. RESULTS AND DISCUSSION

The MUX, Ripple carry adder and Arithmetic unit, Logical unit, Multiplexer based on majority gate configuration, Integration of Arithmetic and Logical unit has been designed. They are simulated using the QCA Designer tool. The comparison between the existing and the proposed ALU has been performed in this section.

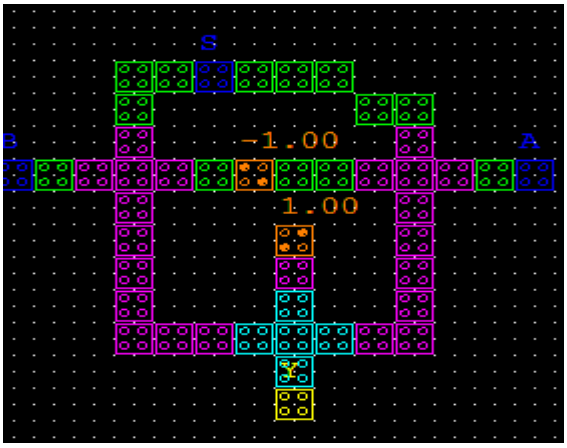

Figure 12. QCA layout for the Multiplexer.

Figure 12 depicts the design of Multiplexer with three majority gates. Having constant values -1 for 0 and +1 for 1 to get logic 1 and -0 constant values.

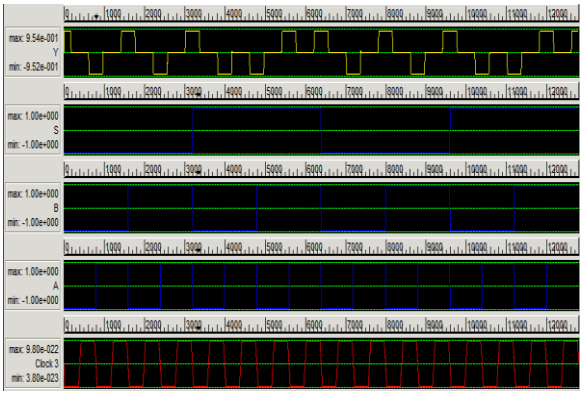

Figure13. Simulation result for Multiplexer.

This above figure shows the output result for the multiplexer.

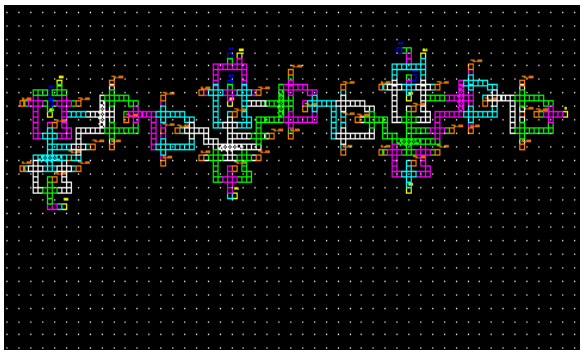

Figure 14. QCA layout for the Ripple carry adder.

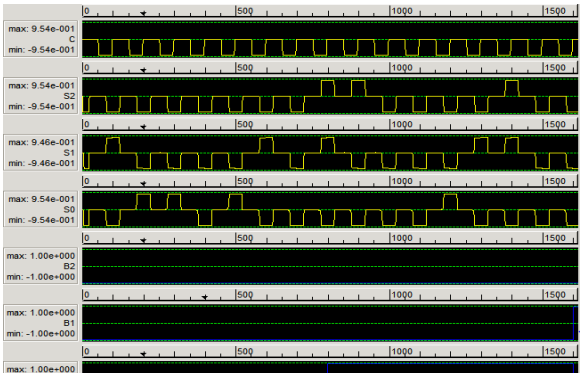

Figure 15. Simulation result for the RCA.

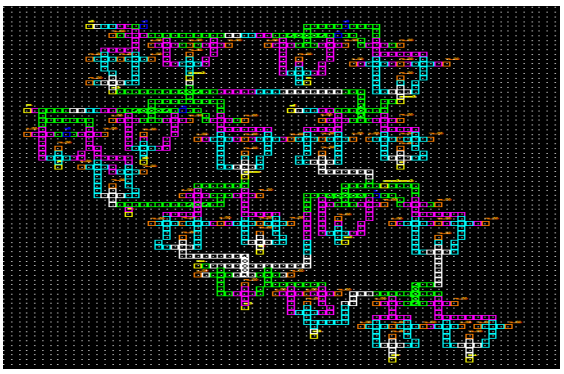

Figure 16. QCA layout for the Logic unit

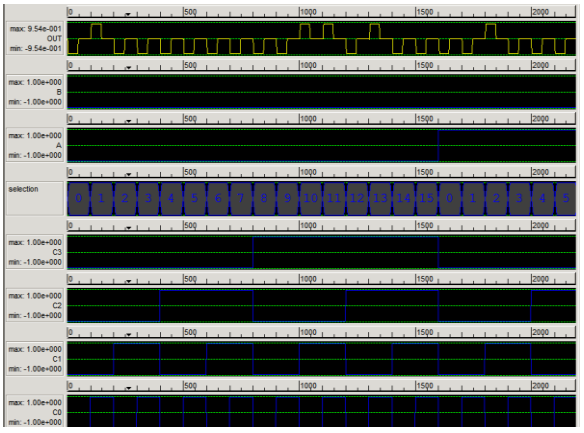

Figure 17. Simulation result for the Logic unit

All the figure here shows the simulation and design in QCA lay out. Figure 16 shows the QCA lay out for the

Logic unit equation which performs different operations listed in table for logical operations. Figure 17 shows the output wave forms ie simulation results in QCA. Similarly The QCA layout and output wave forms for Arithmetic unit and Arithmetic and logic unit are shown in figure 18, figure 19, figure 20, and figure 21

Figure 18. QCA layout for the Arithmetic unit.

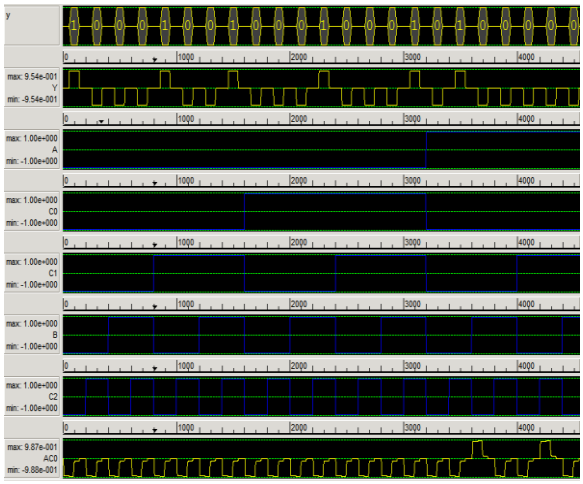

Figure 19. Simulation output for the Arithmetic unit

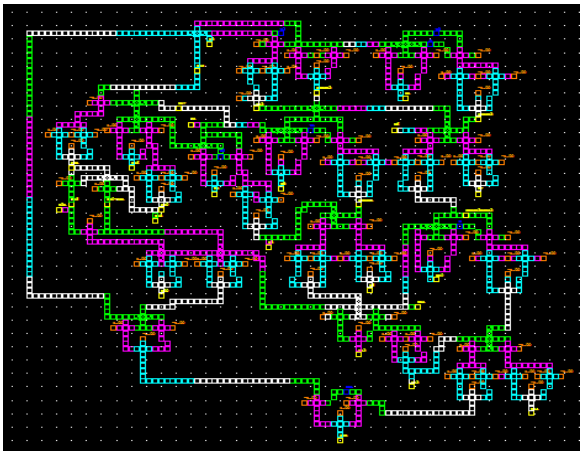

Figure 20. QCA layout for the ALU.

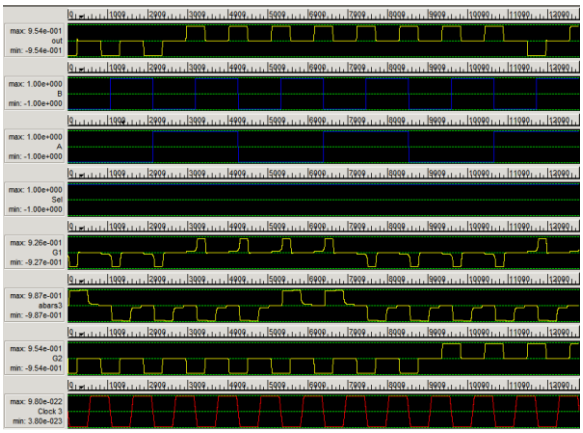

Figure 21. Simulation result for the ALU

The following table 4 shows the comparison for existing and proposed designs in terms of quantum cost, garbage outputs, gate count and constant inputs.

Table 4. Comparison table for Arithmetic unit

parameters	**Existing design**	**Proposed design**
Quantum cost	23	32
Garbage outputs	10	6
Gate count	5	5
Constant input	5	1

The below table shows the variation of parameters in terms of QC, GO, CI with proposed and existing system for logic gate

Table 5. Comparison table for Logic unit

Parameters	**Existing design**	**Proposed design**
Quantum cost	52	62
Garbage outputs	14	14
Gate count	12	9
Constant input	12	2

Table 6. Comparison table for ALU

Parameters	**Existing design**	**Proposed design**
Quantum cost	75	94
Garbage outputs	24	20
Gate count	17	14
Constant input	19	3

Table 7. Comparison table for RCA

Parameters	Existing design	Proposed design
Quantum cost	24	18
Garbage outputs	6	6
Gate count	6	3
Constant inputs	3	3

The above tables shows the comparisons of Arithmetic logic unit and Ripple carry adder between existing and proposed.

V. CONCLUSION AND FUTURE WORK

In this paper three novel Reversible Gates are proposed for ALU. The proposed gates are having minimal quantity of cells as in comparison with the prevailing gates such as Fred kin gate. The proposed gates show growth in terms of optimization parameters in reversible logic as in comparison with the existing reversible gates. The design is validated within the QCA platform. The proposed QCA based MUX, Ripple carry adder and arithmetic and good judgment unit suggests prodigious growth in the design parameters of reversible concept and the simulation constraints like to discipline, simulation time and quantity of cells employed in the design. Hence the proposed process has minimal subject with QCA and low energy dissipation with Reversible logic. The proposed ALU can be used within the Processor structure and in Future the whole structure may also be designed utilizing the reversible good judgment concepts and gates.

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