Analysis of Testing Techniques for Low Power Applications

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ABSTRACT

Power consumption during test has become an important role in test manufacturing because it can lead to the destructive testing and some time the problem of wrong response due to overheating, so reducing power is a main objective during circuit design. This paper proposes comparison of results of the existing techniques. New techniques can be proposed in the future to reduce more power without any compromise.

Keywords : Test Pattern, X-Filling, Arithmetic Coding, Genetic Algorithms, Built, Self-Test.

I. INTRODUCTION

Device dimensions are decreasing over the few last decades and new techniques are leading to smaller and smaller possible size. As size decreases, circuits complexity and power consumptionincreases but, the main issue is power consumption during testing small size circuits.

Power consumption during testing circuits can be four times more of that in normal mode operation. The increment in the power during testing can be due to higher switching activity, circuit overheating, test data volume, and current density. Due to high power consumption during testing good chip gets damaged and can lead to the manufacturing yield loss and decrease in reliability. [1]

Need Of Esting

Testing is a process in which a circuit is exercised and the response is checked that it behaves correctly or not. Testing is done to check the function as well as logical behavior of the circuit which can be manipulated by design error, fabrication error, fabrication defects and physical failures.[2] Testing is done on input and internal lines and the result is tested by system itself or by an external device.

II. LOW POWER TECHNIQUES

2.1 Low-Power Test Pattern Generation

Test pattern generation is main part of testing circuits by which switching activity can be decreased. Power can be reduce during testing by low power test compaction, low power X-filling, and test vector ordering.[1] With the help of this technique two problems, like circuit overheat and performance degradation can be overcome.

2.2 Low power test compaction

The requirement of compaction is to reduce number of test vectors. Test cube can be exploited using test compaction, test cubes are the test vector containing unspecified bits or X- bits. Test data compaction can be done as dynamic compaction and static compaction. Dynamic compaction specifies the X-bits in a test cube in order to detect more faults than the initially targeted fault, while static compaction uses the X-bits in compatible test cubes to merge them into one test cube. [3]
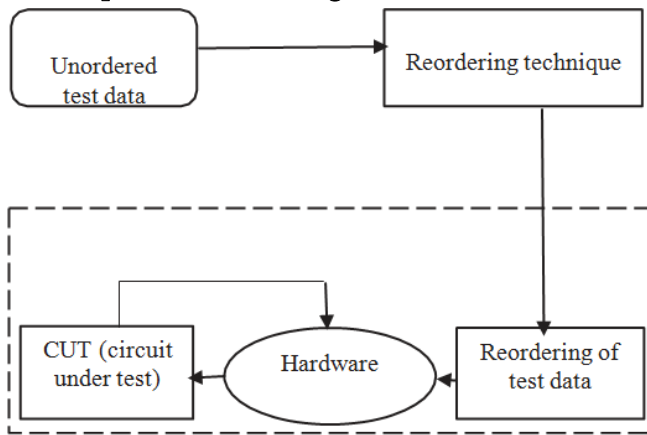
2.3 Low power test ordering

Figure 1. Test data reordering technique

There are many different techniques for test vector ordering which are as follow,

2.3.1 Artificial Intelligence Approach to Test Vector Reordering

With the help of this technique we can overcome the problems like reliability and short term malfunction. In this technique, we have reduced dynamic power consumption during test application without losing stuck-at fault coverage. [5]

2.3.2 Scan chain reordering

Using scan chain reordering the overall average power and peak power are reduced. In this method fault coverage, test application time, and hardware area overhead is negligible. [6]

2.4 Low-Power X-Filling

As some of the test vectors are left with unspecified value; for example 10X01X. In X filling technique each X bit is replaced by 0 or 1. The main point is to reduce the number of transition in scan cell which leads to the reduction in overall switching.

The X filling technique is divided into three different approaches: minimum transition filling technique (MT- filling), 0 filling (set all X bit to 0), 1 filling (set all X bit to
1) [8]

As a simple example, consider the test cube [0XX1X0X1XX]. By applying all three filling techniques on above test tube the resulting vectors and the number of transitions will be

- ✓ MT-Filling: 0001100111 (3 transitions)
- ✓ 0-Filling: 0001000100 (4 transitions)
- ✓ 1-Filling: 0111101111 (3 transitions)

2.5 Test Data Compression

Test data compression technique is used to handle the problem of increased test data volume.

2.5.1 Compression of VLSI Test Data by Arithmetic Coding

In this method of compression Huffman code, Golomb code and Run-Length coding are used. Golomb coding achieves good compression provided input symbols representing runs with shorter group prefix have higher probabilities.

In Arithmetic coding word length is close to the entropy and high compression ratio can be obtain. As the data is reduce the switching decreases. [9]

2.5.2 Static Test Data Volume Reduction Using Complementation

Using complementation of the some of the bits it is possible to reduce the size of stored test sets. With this technique the input data volume is reduced but the number of the patterns applied to the circuit is increases.

Applying Arithmetic coding technique on benchmarks the compression ratio is found as below [10]

Table 1. compression ratio

Benchmarks	Compression ratio		
	Golomb	Huffman	Arithmetic
S5378	48%	50%	65%
S9234	57%	54%	66%
S13207	82%	69%	86%
S15850	65%	60%	75%

S35932	13%	55%	70%
S38417	45%	51.5%	70%
S38584	54%	53.5%	69%
Average	52%	56%	72%

2.6 Genetic Algorithm for VLSI Test vector Selection

The algorithms take the priority of the different conditions into consideration. This allows the validation team to fulfill different testing coverage objectives. For example, testing objective can be set to choose the minimum number of sets that covers at least 90% of the high risk operations and 80% of the low risk operations. [11]

The genetic algorithm is the first to find the best set of test vectors that satisfies the target coverage under different scenarios, while taking into consideration operations priority and computing cycles required by each test vector.

2.7 Low-Power BIST Techniques

BIST (Build in self-test) in which a circuit is equipped with an on-circuit stimuli generator and a response evaluator. A BIST-equipped circuit tests itself, thereby reducing the ATE (Automatic test equipment) storage requirement. Furthermore, BIST provides at-speed test application and enables the use of low-cost ATE as requirements on timing accuracy, vector memory, and pin count are strongly reduced. Also, BIST offers superior test quality because a large number of patterns can be applied to the circuit using on-chip TPG (Test pattern generator), which increases the detection probability of unmolded defects. Other advantages of BIST are board-level/system level test and in-field test of critical applications.

III. RESULTS AND DISCUSSION

Above techniques are implemented on different circuits and devices and the result of this techniques are summarized in the table 2.

The result also shows power reduction done using different technique, this comparison is essential in order show the reduction in power during testing. We note that the average power consumption is greater but the difference between peak power is less.

Table 2. comparison of techniques

Sr. Number	Techniques	Approx. Power reduction (%)
1	Low-Power Test Pattern Generation	15% [1]
2	Low power test compaction	11% [3]
3	ow power test ordering	22% [4,6]
4	ow-Power X-Filling	5% [8]
5	Test Data Compression	9% [9]
6	Genetic Algorithm for VLSI Test vector Selection	10% [10]

IV. CONCLUSION

This paper describes different techniques by which there is a significant decrement in the power during testing circuits. Low power test ordering technique is found to be best among all techniques as it reduces the power and fault coverage is maximum, by reducing the power we can overcome problems of destructive testing and improvement in manufacturing loss and reliability.

V. REFERENCES

[1]. Abramovici, M.; Breuer, M.; Friedman, A, "Digital Systems Testing and Testable Design", Wiley-IEEE Press, 1990

[2]. Patrick Girard, Nicola Nicolici, Xiaoqing Wen, "Power Aware Testing and Test Strategies for Low Power Devices", Springer Science Business Media, 2010

[3]. Patrick Girard, "Low Power Testing of VLSI Circuits: Problems and Solutions", Quality Electronic Design, IEEE 2000 First International Symposium on March 2000

[4]. Chul-ki Baek, Insoo Kim, Jung-Tae Kim, Yong-Hyun Kim, Hyoung Bok Min, and Jae-Hoon Lee, "A Dynamic Scan Chain Reordering for Low-Power VLSI Testing", Information Technology Convergence and Services (ITCS), 2nd International Conference on August 2010

[5]. Samah Mohamed Saeed, Ozgur Sinanoglu,and Sobeeh Almukhaizim, "Predictive Techniques for Projecting Test Data Volume Compression", IEEE transactions on very large scale integration systems, vol. 21, no. 9, September 2013

[6]. Sudip Roy, Indranil Sen Gupta and Ajit Pal, "Artificial Intelligence Approach to Test Vector Reordering for Dynamic Power Reduction during VLSI Testing", TENCON, IEEE Region 10 Conference, November 2008

[7]. H. Hashempour and F. Lombardi, "Compression of VLSI Test Data by Arithmetic Coding", Defect and Fault Tolerance in VLSI Systems, 2004. DFT 2004. Proceedings. 19th IEEE International Symposium on 10-13 Oct. 2004

[8]. P.Basker & A.Arulmurugan, "Survey of Low Power Testing of VLSI Circuits", International Conference on Computer Communication and Informatics (ICCCI-2012), Jan. 10 – 12, 2012

[9]. Peter Wohl, John A. Waicukauski, Frederic Neuveux, Emil Gizdarski, "Fully X-tolerant, Very High Scan Compression", Design Automation Conference (DAC), 2010 47th ACM/IEEE

[10]. Walid Ibrahim, Amr Elchouemi, and Hoda Amer, "A Two-Phase Genetic Algorithm for VLSI Test vector Selection", IEEE Congress on Evolutionary Computation, July 2006

[11]. Po-Han Wu, Tsung-Tang Chen, Wei-Lin Li and Jiann- Chyi Rau, "An Efficient Test-Data Compaction for Low Power VLSI Testing", Electro/Information Technology, IEEE International Conference on May2008.