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Implementation of Self-Checking Carry-Select Adder Based on Two-Rail Encoding in FPGA

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ABSTRACT

Self-checking carry-select adder design based on two-rail encoding is an efficient method, due to its arithmetic operations and short delay. This paper presents the design of the Compressor based Self-checking carry-select adder design .The circuit can detect all single stuck-at faults during on-line operation mode. Its performance is increased by using compressor by replacing all full adders.

Keywords: Compressor, Carry Select Adder, Area, Delay, Area-Delay Product.

I. INTRODUCTION

Technology is improving in on-line error detection in very large scale integration (VLSI) [3]. Arithmetic circuits are important blocks in many circuits such as integrated circuits (IC) digital signal processors [2].So, it is a challenge to design the high performance and highly reliable adders have become the important issue and hot spot.

The different types of adders[2] are, e.g., ripple carry adder, carry look ahead adder, carry skip adder, conditional sum adder, carry-select adder (CSeA) and so on. Each and Every adder has different in delay time, chip area, design complexity, and power. Among all the adders, CSeA is used widely due delay time, low power dissipation, easy implementation .The area and speed of different adders is shown in the figure.1

Type of adder	*Area (10^3 μm^2)*	*Delay (ns)*	*Overhead (%)*
Ripple-carry	2.65	28.3	34
Manchester	2.44	14.7	35
Carry-skip	3.46	11.3	27
Carry-select	5.97	9.2	30
Conditional-sum	6.07	10.6	31

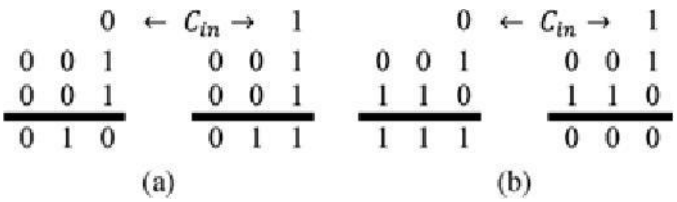
Figure 1 : The area and speed of different adders

In addition, CSeA, which is high performance, area overhead. The probability of faults, especially single-stuck-at-faults, is grown in VLSI systems. In order to guarantee highly reliability, the online detection of faults in carry select adder is important

II. METHODS AND MATERIAL

2. Relation between Sum Bits

Property: The relation between sum bits calculated with identical inputs is only dependent on the carry-input, and for complemented values of carry-input, we will obtain complemented sum bits (keeping other airs of input bits identical).



For the carry input cin=0,cin=1

1. For the identical inputs, if carry input zero or one then it will be normal addition operation.
2. For the inverted inputs with carry input zero then it will be all ones.
3. For the inverted inputs with carry input one then it will be all zeros.

3. Existing System

3.1 Design of A Self-Checking 2-Bit Carry-Select Adder

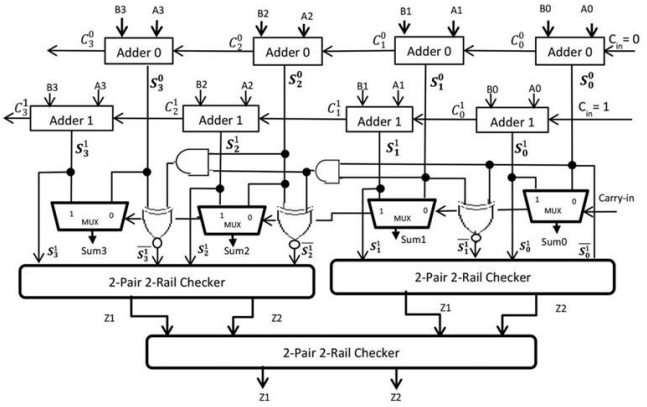


Figure.3: Existing System [1]

The stages of the self-checking carry select adder design Based on two rail encoding is a chain of full adders to form ripple carry adder and it is a two rail ripple carry adders and these full adders are connected to And gate and Multiplexers. The two-pair-two-rail checker has four inputs and two outputs.

3.2 Two-pair-two-rail checker

The two-pair-two-rail checker, multiplexers [2], EX-NOR can detect the presence of any single stuck-at fault in the circuit during on-line. At the primary outputs self-checking Multiplexers will detect faults internal in the circuit these faults are propagating to the output stage. At the output stage the totally self-checking checker determines the presence of the fault in the circuit.

The checker has two types i.e., 01 and 10 are considered valid code words. The inputs to the checker. A non-valid checker output, i.e., 00 or 11 detects the presence of a fault in the circuit or in the checker

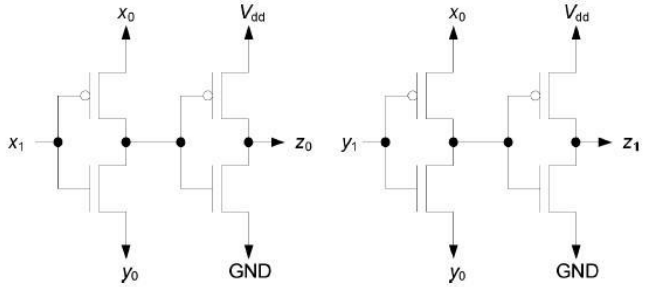


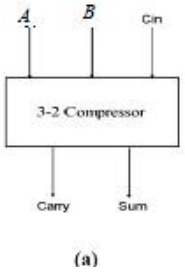
Figure.4: Two-pair two-rail checker

4. Proposed System

The proposed circuit replaces Full adders with 3:2 compressors [4] and its architecture consists of XOR gates and multiplexers. This will increase performance of the circuit by reducing the delay of the system.

4.1 Compressors

Compressors are used to minimize delay [4] and area which leads to increase the performance of the overall system. So in the place of full adder 3:2compressor can be used. A 3-2 compressor has three inputs A, B, cin and generates two outputs, the sum and the carry bits. The block diagram of 3-2 compressor is shown in figure



A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(b)

Figure 5: 3-2 Compressor

A 3-2 compressor cell [4] can be implemented in many different logic structures. However, in general, it is contains three main modules. The first sub circuit is required to generate XOR or XNOR function [4], or both of them. The Second sub circuit is used to generate sum and the last sub circuit is to produce carry output. The 3-2 compressor can also be drawn as a full adder

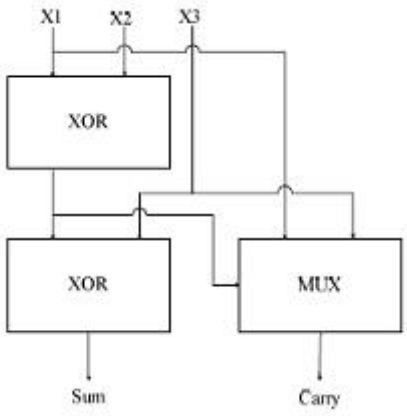
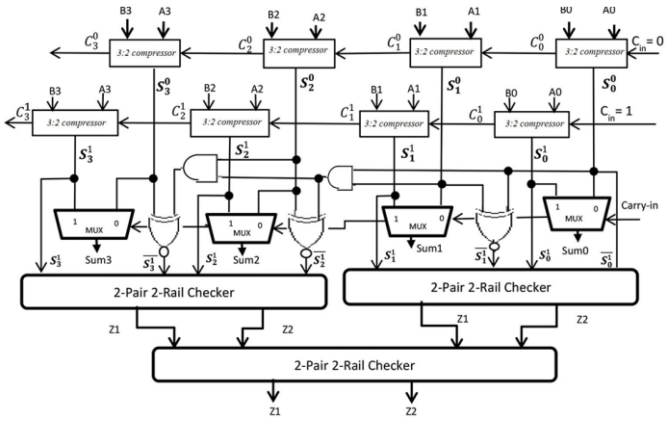


Figure 6: the internal architecture of 3-2 Compressor using XOR and Multiplexer

The Internal structure of 3-2 compressor shown in figure, it has two XOR gates. The sum output is generated by the second XOR and carry output is generated by the multiplexer (MUX). The equations governing the conventional 3-2 compressor [4] outputs are shown below:

5. IMPLEMENTATION

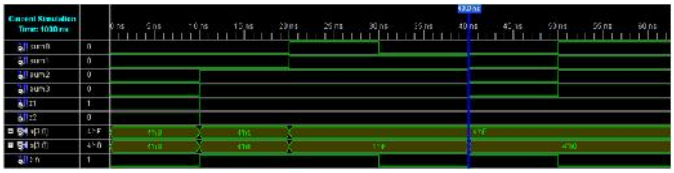
The proposed circuit consists of 3:2 compressors, multiplexers, EX-NOR and the Mechanism is shown in the fig



III. RESULTS AND DISCUSSION

The Proposed system is simulated and verified using Verilog HDL in Xilinx ISE 10.1.This is the simulation results for the 4 bit self-Checking circuit and it is calculated for cin=0, cin=1

For the cin=1



For the cin=0

This Table represents the comparison of full adder and compressor in terms of delay and power.

Bits	4-bit	8-bit	16-bit	32-bit	64-bit

With Full adders

Delay	10.687	13.965	21.507	36.266	63.499
Power	30.78	32.34	34.26	36.75	38.53

With Compressor

Delay	9.292	13.965	14.554	16.025	17.146
Power	30.75	32.29	34.12	36.32	37.12

IV. CONCLUSION

This paper analyzes the self-checking carry-select adder design based on two-rail encoding, which can be used in the testing applications purposes. In the proposed method compressor is used to overcome the limitations. Simulation results and synthesis results confirm that the proposed system has better power- delay product than existing system.

V. REFERENCES

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