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Three Stage Cascaded Multilevel Inverter using Pulse Width Modulation Technique

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ABSTRACT

In the last few years, the necessity of increasing the power quality enhancement in industry has sustained the continuous development of multilevel- inverters due to high efficiency with low switching frequency control method. The inverter is a semiconductor device which is used to convert the fixed DC voltage into symmetrical AC voltage without changing the magnitude. To improve the power quality (AC) from the inverter output by performing the power conversion in small voltage steps resulted in lower harmonics. The output voltage on the AC side can take several discrete levels of equal magnitude. The harmonic content of this output voltage waveform is greatly reduced, if compared with a two level voltage wave form (inverter). This method is called as multilevel inverter. Multi-level power inverters employ power semiconductor switches in the inverter to select one or more of multi dc voltage source to create staircase voltage waveform at the inverter output. In the multilevel inverter the output voltage is in the form of stepped waveform, so that the harmonics will be reduced and thereby increase the voltage gain and power quality of the output AC from the MLI.
Keywords: Multilevel Inverter-CMLI,DMLI-PWM-H BRIDGE-INVERTER

I. INTRODUCTION

Several topologies for multilevel inverts have been proposed over the years the most popular being the diode clamped, flying capacitor and cascaded H-bridge structures. One aspect which sets the cascaded H-bridge apart from other multilevel inverts is the capability of utilizing different DC voltages on the individual H-bridge cell which results in splitting the power conversion amongst higher-voltage lower-frequency and lower-voltage higher frequency inverts. An alternate method of cascading inverts involves series connection of two three phase inverters through the neutral point of the load.

An advantage of this approach is that isolated sources are not required for each phase. It should be noted that cascaded inverter system can be considered from a number of different viewpoints. Considering the cascaded inverter to be one unit, it can be seen that a higher number of voltage levels are available for a given number of semiconductor devices. Capacitors batteries and or renewable energy voltage sources can be used as a DC voltage sources.

-commerce has become one of the vital parts of the modern life. Online payment is the supportive application for the payment of money for the products we buy. For the past years online security breach created a major problem and lots of money had been stolen. The proposed document deals by securing the payment through iris recognition [1]. This method also adds the method of using visual cryptography for securing the user credentials. This visual cryptography method was formerly invented by Moni Naor and Adi Shamir in 1994[6].

II. METHODS AND MATERIAL

A. Stages of Multilevel Inverter

The three stages of CMLI are high-voltage stage, medium voltage stage and low voltage stage. The high, medium and low voltage stages are made of three-level inverters constructed using cascaded H-bridge. This method is used to avoid the undesirable high switching frequency for all the voltage stages despite the fact that the inverter's dc sources are selected to maximize the inverter levels by eliminating redundant voltage state.

B. Multilevel Inverter Topologies

i Introduction

The multilevel voltage source inverter is recently applied in much industrial application such as AC power supplies, static VAR compensators, drive systems, etc, one of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency of decreasing the inverter power output. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitors voltage sources. As the number of levels reach infinity the output THD approaches zero. The number of the achievable voltages levels, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout and packaging constraints.

ii Types of Multilevel Inverter

There are three types of multilevel inverter namely Diode-Clamped Multilevel Inverter, Flying-Capacitor Multilevel Inverter and Cascaded-Inverters with Separated Dc Sources. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generates voltages with stepped waveforms with less distortion, less high switching frequency, higher efficiency, lower voltage devices and better electro-magnetic compatibility. The commutation of the switches permits the addition of semiconductors must withstand only reduced voltages.

- **Diode-Clamped Multilevel Inverter (DCMLI)**

The Diode-Clamped Multilevel Inverter uses capacitors in serried to divide up the Dc bus voltage into a set of voltage levels. To produce m level of the phase voltage, an m level diode-clamp inverter need m – 1 capacitors on the DC bus. A single phase five-level diode-clamped inverter is shown in Fig.3.1.

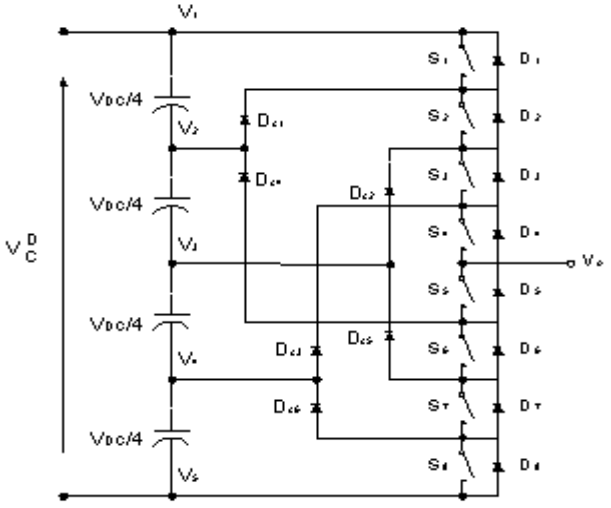

Figure 1: Diode-Clamped Multilevel Inverter (DCMLI)

Table 1 shows the phase voltage level and their corresponding switch states. When the switch is on the output voltage becomes one otherwise the value becomes zero. Table 1 shows the switching pattern of Diode clamped Multi- Level Inverter and the output phase voltage for the corresponding switching states when the switch S1 and S8 is ON, the output phase voltage is produced by the voltage of $V_{1\ and}\ V_5$.

Table 1: Switching Pattern of DCMLI

POWER INDEX VALUE	OUTPUT PHASE VOLTAGE (V_O)				
	V1	V2	V3	V4	V5
S1	1	0	0	0	0
S2	1	1	0	0	0
S3	1	1	1	0	0
S4	1	1	1	1	0
S5	0	1	1	1	1
S6	0	0	1	1	1
S7	0	0	0	1	1
S8	0	0	0	0	1

- **Flying Capacitor Multilevel Inverter**

Capable Of Solving Capacitor Voltage Unbalance Problem And Excessive Diode Count Requirement In Dcmi .Employs Separate Capacitors Pre Charged To [(Nl-1)/(Nl-1)X Vdc], [(Nl-2)/(Nl-1)X Vdc] …{[Nl-(Nl-1)]/[Nl-1]X Vdc}. Size Of Voltage Increment Between Two Capacitors Defines Size Of Voltage Steps In Icmi Output Voltage Waveform.A Flying Capacitor Multilevel Inverter In Fig 2 Uses A Ladder Structure Of Dc Side Capacitor Where The Voltage On Each Capacitor Differs From That Of The Next Capacitor

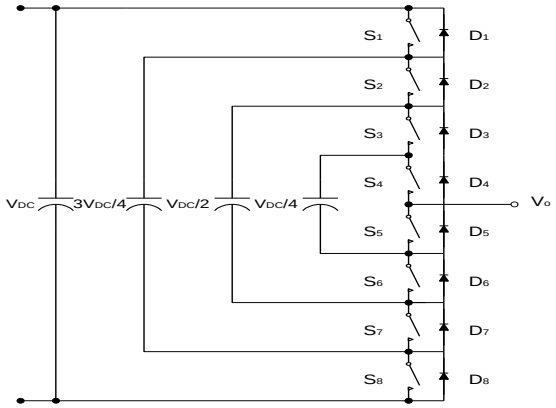

Figure 2: Flying Capacitor Multilevel Inverter (Fcmli)

To Generate M-Level Staircase Output Voltage, M1 Capacitors In The D Bus Are Needed. Each Phase-Leg Has An Identical Structure. The Size Of The Voltage Increment Between Two Capacitors Determines The Size Of The Voltage Levels In The Output Waveform.

Table 2: Switching Pattern of FCMLI

OUTPUT V_{Ao}	SWITCH STATE							
	Sa1	Sa2	S_{am-1}	S_{am}	$S_{a'1}$	$S_{a'2}$	$S_{a'm-1}$	$S_{a'm}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_3=V_{dc}/2$	1	1	0	0	1	1	0	0
$V_2=V_{dc}/4$	1	0	0	0	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

Table 2 Shows The Phase Voltage Level And Their Corresponding Switch States. From Table 3.2, State 1 Represents That The Switch Is On And State 0 Represents The Switch Is Off.

- **Cascaded Multilevel Inverter**

The general function of this multilevel inverter is the same as that of the other two previous inverters. This multilevel inverter using cascaded inverter with SDCSs synthesis a desired voltage from several independent sources DC voltages which may be obtained from batteries, fuel cells, all solar cells. of different level inverters are connected in series.

A. Circuit Diagram

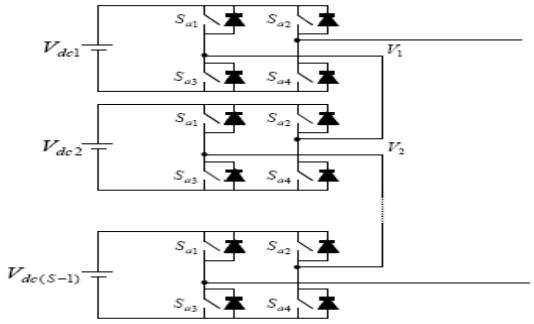

Figure 3. Cascaded Multilevel Inverter (CMLI)

B. Operating Modes

Fig.4 shows the synthesized phase voltage waveform of a five-level cascaded inverter with four SDCSs. The phase output voltage is synthesized by the sum of four inverter outputs, Uan = Ua1 + Ua2 + Ua3 + Ua4. Each inverter level can generate three different voltage outputs, + Vdc' 0, and – Vdc' by connecting the de source to the ac output side by different combinations of the four switches, S1, S2, S3 and S4. Using the top level as the example, turning on S1 and S4 yields Ua4 = Vdc. Turning on S2 and S3 yields Ua4 = Vdc. Turing off all witches yields U4 = 0. Similarly, the ac output voltage at each level can be obtained in the same manner.

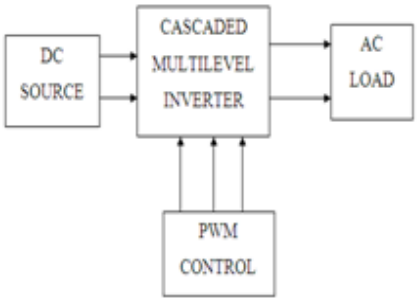

Figure 4: Block Diagram

III. RESULTS AND DISCUSSION

TYPES OF MODULATION TECHNIQUES

4.1: INRODUCTION

The inverter output can be changed and controlled according to the desired level by the triggering pulse given to the gate terminal in the inverter. This controlling method is obtained by a method called as modulation technique. There are several types of PWM modulation techniques for controlling the inverter output by changing the pulses given to the gate from the PWM modulation technique. The pulses from the PWM output are obtained by comparing the carrier based signal and sampling signal. So this pulse is used as a triggering pulse for the gate terminal of the power devices which is used to ON and OFF the power devices.

The various pulse width modulation techniques for controlling the multilevel inverter topologies are step modulation, sinusoidal PWM, space vector modulation, selective harmonic PWM, modified sinusoidal PWM and multiple pulses PWM. Among this space vector PWM is now used in research and development areas but its algorithm is very complex having many number trigonometric functions, so this has less preference to use in the practical implementation.

4.2: PRINCIPLE OF SPWM

In the proposed system the pulse width modulation taken for the controlling of inverter output is the sinusoidal pulse width modulation and it has variation of ON and OFF delay time for switching the power devices without any short circuit. This short circuit occurrence during the switching of power device is carried by the dead time regeneration. So the output of inverter circuit is controlled by the gate triggering pulses given by the pulse width modulation technique.

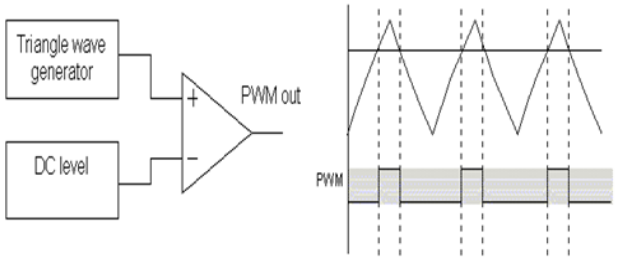

Figure 5: Principle of SPWM

4.3: SINUSOIDAL PWM

Modulation index (m_i):

$$M_i = \frac{\text{Amplitude of the mod waveform}}{\text{Amplitude of the carrier waveform}}$$

Here the sine waveform is taken as the sampling waveform or modulating waveform and the triangular waveform is taken as the carrier waveform. Now by comparing these two waveforms of sine wave and triangular wave the gate pulses are generated by using comparator. Now the gate pulse generated are having various ON and OFF time which is given to the IGBT or MOSFET power devices to controlling the output voltage.

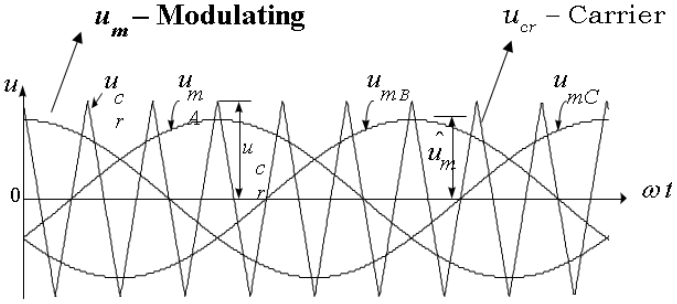

Figure 6: Modulating and Carrier Waves

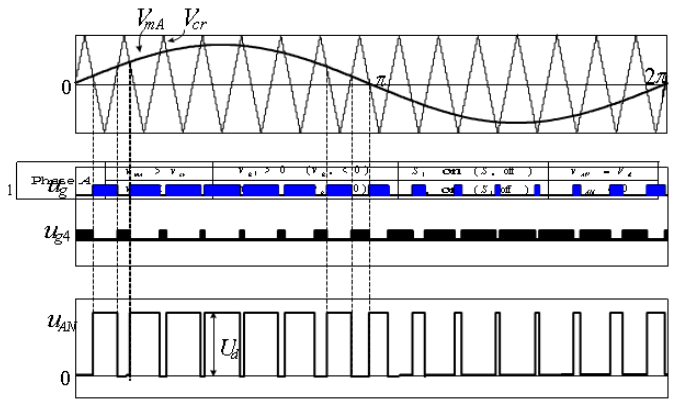

Figure 7: Principle of Sinusoidal Pulse

Here the principle of sinusoidal pwm is predicted. here by varying the modulation index we can change the output voltage by means of varying the ON and OFF pulses.

MATLAB MODEL FOR 27 LEVELS CMLI

Fig 7.3 shows MATLAB model of model three stage cascaded multilevel inverter with modulation control. This model contains DC source voltages, gate pulse circuit, power switches like IGBT's.

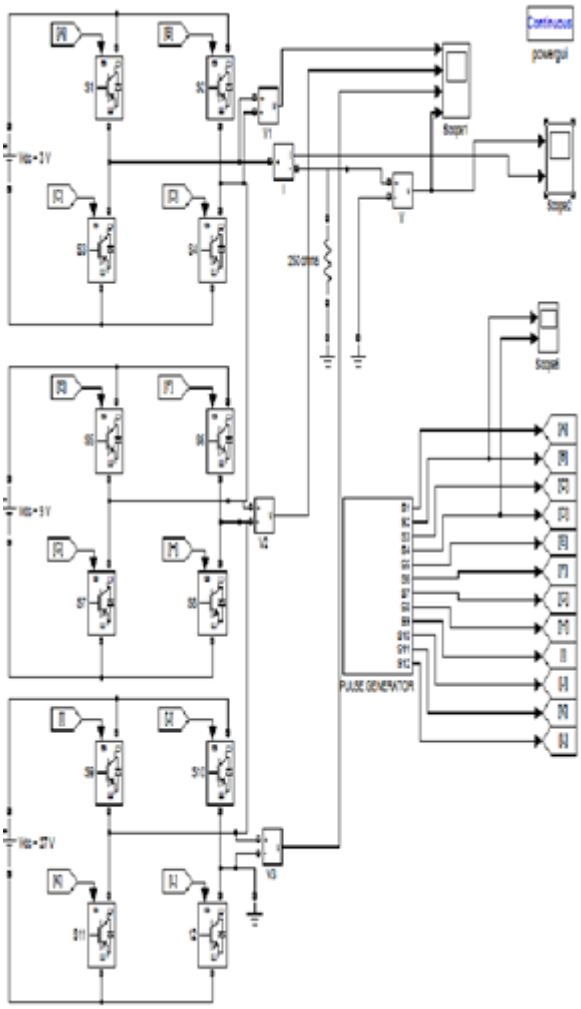

Figure: 7.2: Simulink Models of 27 Levels CMLI

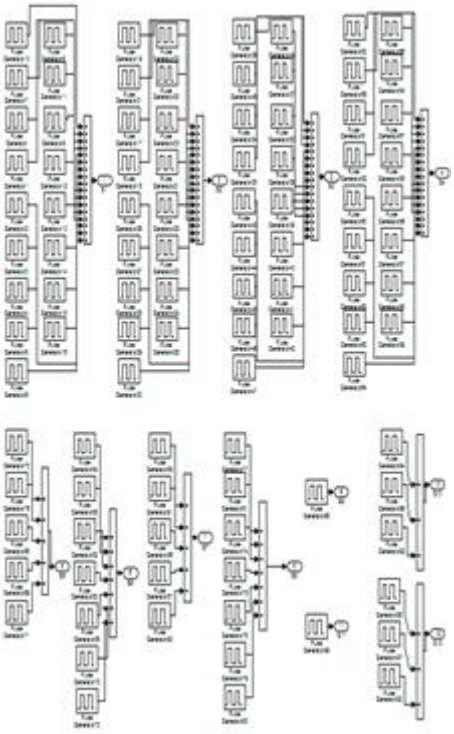

Figure 7.2: Sub System of SPWM Generating Simulating Block

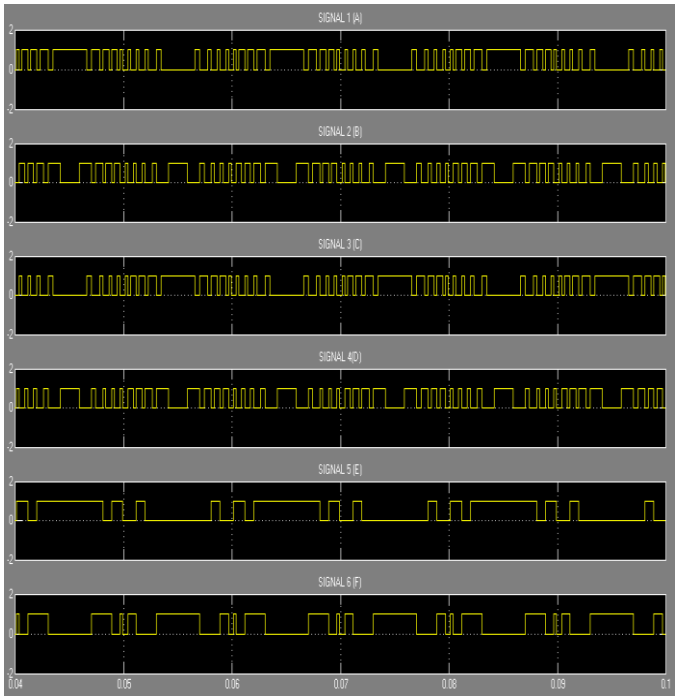

Figure 7.3: SPWM- P1, P2, P3, P4,P5, P6 PULSES

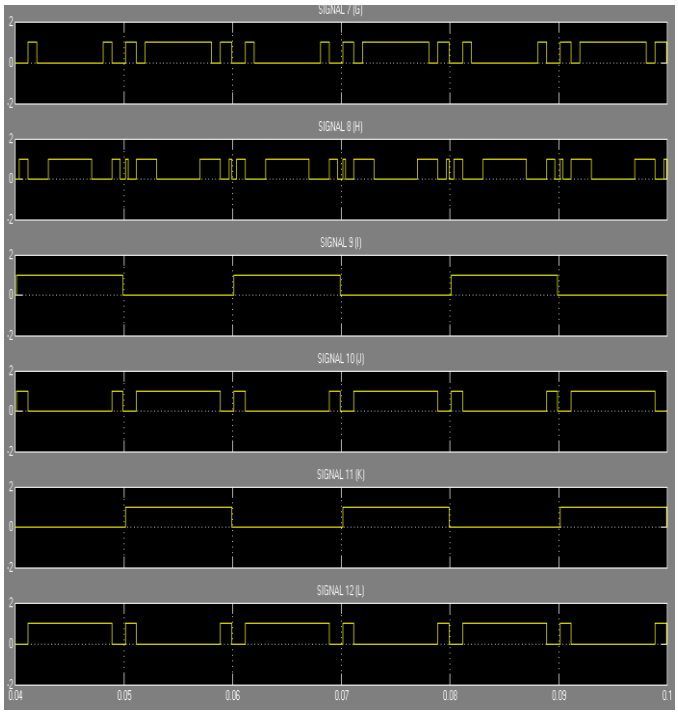

Figure 7.4: SPWM- P7, P8, P9, P10,P11, P12 pulses

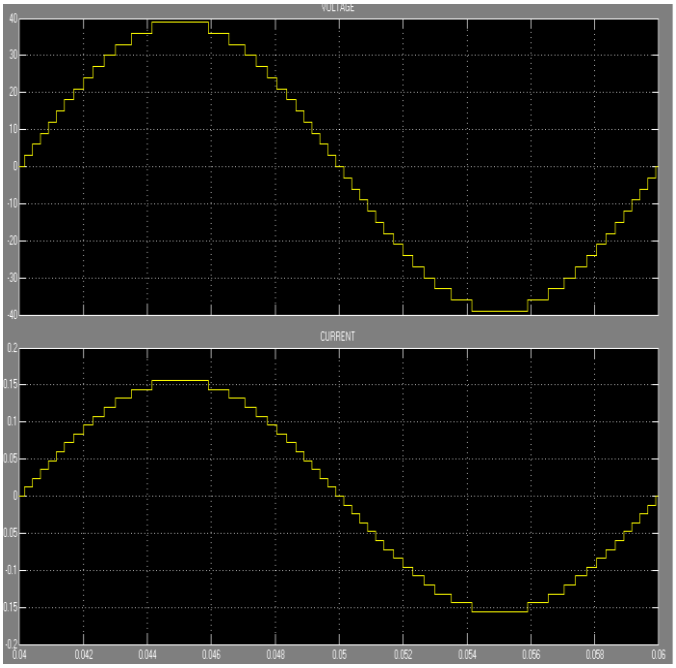

Figure 7.5: output of 21 levels CMLI

IV. Conclusion

The disturbances in power electronics equipment are often periodic and rich in higher harmonics. They have been frequencies and are often above the bandwidth of regulators used to control fundamental components. Therefore the 'regular' control can only partially reduce their effects on the distortion of control variables. The three stage cascade multilevel inverter with number of DC sources is illustrated and the gate triggering pulse is given by the SPWM technique. Here the inverter power device circuit used is IGBT device and it has the better switching frequency and gate control compared to all other semiconductor inverter devices such as power MOSFET, SCR, TRIAC etc., This pulse width modulation (PWM) control techniques enables us to obtain better harmonic reduction characteristics of the output AC stepped voltage with 21 levels under the utilization ratio of different modulation, and achieve optical control of output waveform by different modulation ratio. Finally, we obtained the output AC voltage waveform and their frequency spectrums. Besides that, it realized better multilevel output and achieved desired results.

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