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Design of Dual Quality 4:2 Reverse Compressor Based Configurable Multiplier

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ABSTRACT

Reversible logic gates became very important and computing paradigm having its applications in low power CMOS technologies and Quantum computing we proposed reversible gates methodology also introduces for quantum cost reducing of circuit. Multiplier plays a vital role in many applications such as digital image processing, digital signal processing etc so it is important to design the multiplier with low power consumption and reduced delay. In order to reduce this factor we design the multiplier using four 4:2 compressor and these compressors has a switching mode and this is used to switch between the exact and approximate modes. In this paper, we introduce a novel architecture to perform high speed multiplication using ancient Vedic math techniques. A new high speed approach utilizing Dual quality 4:2 reverse compressor. The efficiencies of these compressors in a 16-bit multiplier are evaluated and by comparing their parameters with those of the state-of-the-art approximate multipliers. The results of comparison indicate, average lower delay and power consumption in the approximate mode. This paper is synthesized and simulated in XILINX software using verilog as hardware description language.

Keywords: Reversible Gates, Compressors, Vedic Multiplier.

I. INTRODUCTION

Multipliers are frequently used in DSP, Image processing architectures and microprocessors. Fast Fourier Transform (FFT), Discrete Wavelet Transform (DWT) and auto-correlation are the few important areas where multipliers are mostly used. As switching and critical computations of a multiplier are high, compared to other datapath units of a processing architecture, design of low power, high speed multipliers are carried out to reduce latency and power dissipation of a processing system.

The speed of a processor greatly depends on its multiplier‟s performance. This in turn increases the demand for high speed multipliers, at the same time keeping in mind low area and moderate power consumption. Over the past few decades, several new architectures of multipliers have been designed and explored. Multipliers based on the Booth‟s and modified Booth‟s algorithm is quite popular in modern VLSI design but come along with their own set of disadvantages. In these algorithms, the multiplication process, involves several intermediate operations before arriving at the final answer.

The intermediate stages include several comparisons, additions and subtractions which reduce the speed exponentially with the total number of bits present in the multiplier and the multiplicand. Since speed is our major concern, utilizing such type of architectures is not a feasible approach since it involves several time consuming operations. In order to address the disadvantages with respect to speed of the above mentioned methods, and explored a new approach to multiplier design based on ancient Vedic Mathematics. Vedic Mathematics is an ancient and eminent approach which acts as a foundation to solve several mathematical challenges encountered in the current day scenario. Vedic Mathematics existed in ancient India and was rediscovered by a popular mathematician, Sri Bharati Krishna Tirthaji. He bifurcated Vedic mathematics into 16 simple sutras (formulae). These Sutras deal with Arithmetic, Algebra, Geometry, Trigonometry, Analytical Geometry etc. In this paper, we explore a novel method to further enhance the speed of a Vedic mathematics multiplier by replacing the existing full adders and half adders of the Vedic mathematics based multipliers with compressors by using Compressors, in its several variants, are logic circuits which are capable of adding more than 3 bits at a time as opposed to a full adder and capable of performing this with a lesser gate count and higher speed in comparison with an equivalent full adder circuit.

II. THE CONVENTIONAL 4-2 COMPRESSOR STRUCTURE

The number of half and full adders count to the total delay in conventional multiplier. The use of compressor structures which perform more than three bit addition.

4-2 compressor has five inputs and three outputs, as shown in Fig. 1. The four inputs X0, X1, X2, and X3, and the output have the same weight. Cin is the output carry of preceding module and Cout, the carry output of current stage is fed to the next compressor. The output Carry is weighted one binary bit order higher. The compressor is governed by the following basic equation:

$$X_0 + X_1 + X_2 + X_3 + C_{in} = Sum + 2.(Carry + C_{out})$$

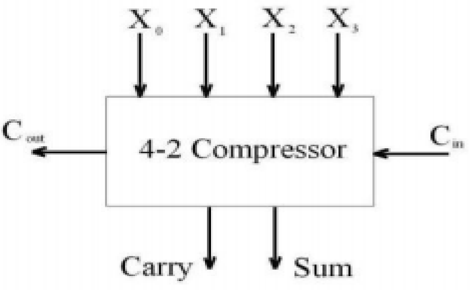

Figure 1. Block diagram of a 4-2 compressor

Besides, to accelerate the carry save summation of the partial products, it is imperative that the output Cout be independent of the input Cin.

The conventional architecture of a 4-2 compressor consists of two serially connected full adders, as shown in Fig. 2 Straight forward implementation of this circuit leads to a long critical path delay. Also because of uneven delay profiles of outputs from different inputs.

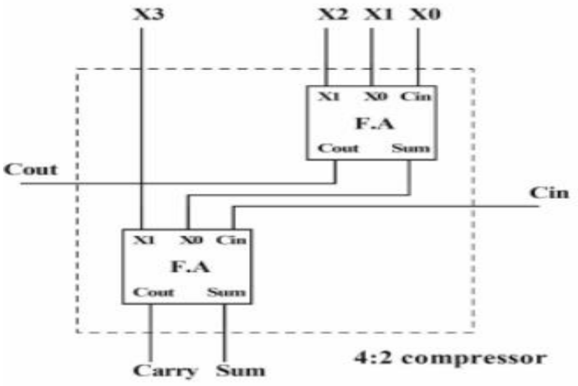

Figure 2. Convential 4-2 compressor scheme

III. DUAL QUALITY 4:2 COMPRESSORS

In this paper, we present four dual-quality reconfigurable approximate 4:2 compressors, which provide the ability of switching between the exact and approximate operating modes during the runtime. The compressors may be utilized in the architectures of dynamic quality configurable parallel multipliers. The basic structures of the proposed compressors consist of two parts of approximate and supplementary. In the approximate mode, only the approximate part is active whereas in the exact operating mode, the supplementary part along with some components of the approximate part is invoked.

The proposed DQ4:2Cs operate in two accuracy modes of approximate and exact. The general block diagram of the compressors.

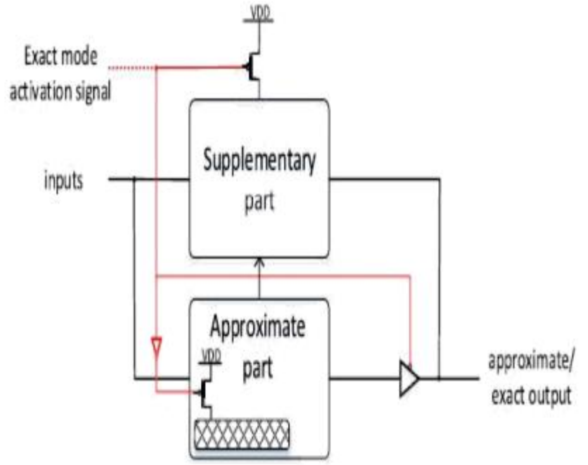

Figure 3. .Block diagram of proposed approximate 4:2 compressors. The hachured box in the approximate part indicates the components, which are not shared between this and supplementary parts

The diagram consists of two main parts of approximate and supplementary. During the approximate mode, only the approximate part is exploited while the supplementary part is power gated. During the exact operating mode, the supplementary and some parts of the approximate parts are utilized. In the proposed structure, to reduce the power consumption and area, most of the components of the approximate part are also used during the exact operating mode. We use the power gating technique to turn OFF the unused components of the approximate part.

a. Structure 1 (DQ4:2C1):

For the approximate part of the first proposed DQ4:2C structure, as shown in Figure(a), the approximate output carry (i.e., $carry'$) is directly connected to the input $x4$ ($carry' = x4$), and also, in a similar approach, the approximate output sum (i.e., sum') is directly connected to input $x1$ ($sum' = x1$). In the approximate part of this structure, the output $Cout$ is ignored. While the approximate part of this structure is considerably fast and low power, its error rate is large.

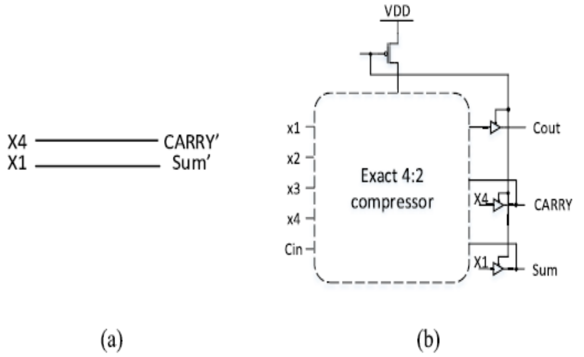

Figure 4. (a) Approximate part and (b) overall structure of DQ4:2C1.

The supplementary part of this structure is an exact 4:2 compressor. The overall structure of the proposed structure is shown in Figure (b). In the exact operating mode, the delay of this structure is about the same as that of the exact 4:2 compressor.

b. Structure 2 (DQ4:2C2):

In the first structure, while ignoring $Cout$ simplified the internal structure of the reduction stage of the multiplication, its error was large. In the second structure, compared with the DQ4:2C1, the output $Cout$ is generated by connecting it directly to the input $x3$ in the approximate part. Fig. shows the internal structure of the approximate part and the overall structure of DQ4:2C2. While the error rate of this structure is the same as that of DQ4:2C1, its relative error is lower.

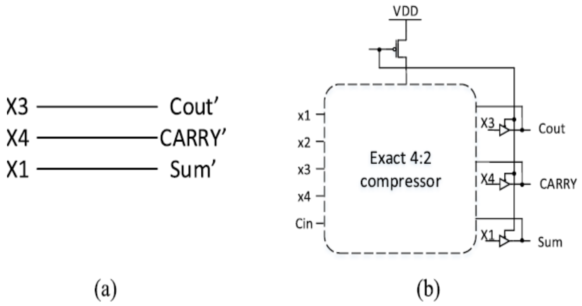

Figure 5. (a) Approximate part and (b) overall structure of DQ4:2C2

c. Structure 3 (DQ4:2C3):

The previous structures, in the approximate operating mode, had maximum power and delay reductions compared with those of the exact compressor. In some applications, however, a higher accuracy may be needed. In the third structure, the accuracy of the approximate operating mode is improved by increasing the complexity of the approximate part whose internal structure is shown in Figure (a). In this structure, the accuracy of output *sum'* is increased. Similar to DQ4:2C1, the approximate part of this Structure does not support output *C*out. The error rate of this structure, however, is reduced compared to previous structures.

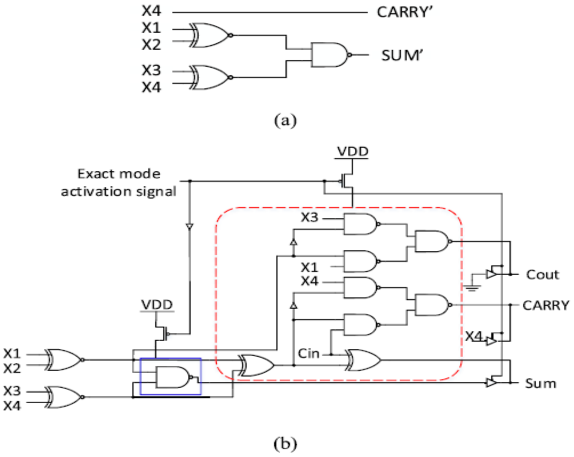

Figure 6. (a) Approximate part of DQ4:2C3 and (b) overall structure of DQ4:2C3.

The overall structure of DQ4:2C3 is shown in Figure (b) where the supplementary part is enclosed in a red dashed line rectangle. Note that in this structure, the utilized NAND gate of the approximate part (denoted by a blue dotted line rectangle) is not used during the exact operating mode. Hence, during this operating mode, we suggest disconnecting supply voltage of this gate by using the power gating

d. Structure 4 (DQ4:2C4):

In this structure, we improve the accuracy of the output *carry'* compared with that of DQ4:2C3 at the cost of larger delay and power consumption where the error rate is reduced more. The internal structure of the approximate part and the overall structure of DQ4:2C4 are shown in Figure. 7. The supplementary part is indicated by red dashed line rectangular while the gates of the approximate part, powered OFF during the exact operating mode, are indicated by the blue dotted line.

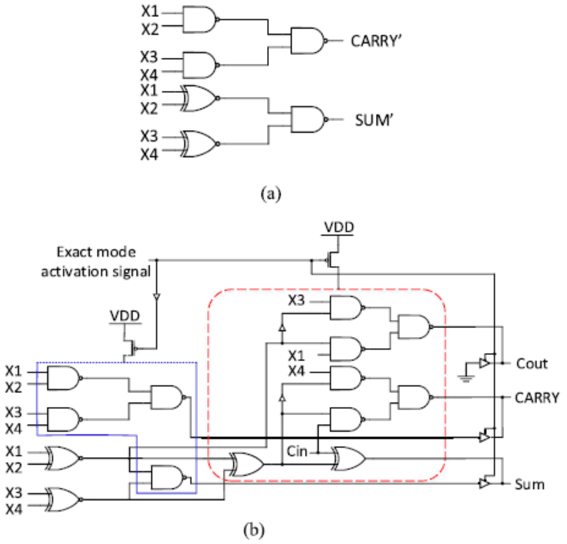

Figure 7. (a) Approximate part of DQ4:2C4 and (b) overall structure of DQ4:2C4.

IV. PROPOSED SYSTEM

Reversible Logic:

Reversible logic plays an important role in recent years due to its ability to reduce the power dissipation which is the main requirement in Low power VLSI design . It is based on the Quantum computing using a physical mechanism that is thermodynamically as well as logically reversible. According to Landauer's research the amount of energy dissipated for every irreversible bit operation is at least kTln2 joules, where k=1.3806505*10-23m2kg-2K-1(joule/Kelvin-1).A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there exist one to- one correspondence between its input and outputs . In this paper a basic 4x4 input TSG gate is taken and used as Full Adder and the same is used to build 4:2 compressors. Basic gates used in this paper are Peres gates, TSG gates.

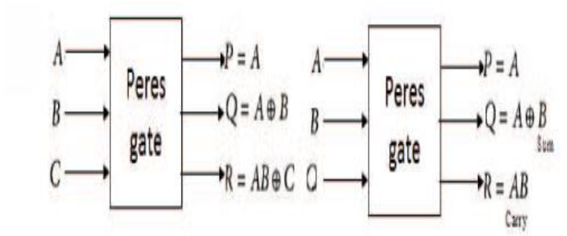

Figure 8. (a) Peres gate ,Fig.(b) Peres gate as adder

The Peres Gate Fig b shows a 3*3 Peres gate. The input vector is I (A, B, C) and the output vector is O (P, Q, and R). The output is defined by P = A, Q = A ⊕B and R = (A.B) ⊕C). Quantum cost of a Peres gate is four .

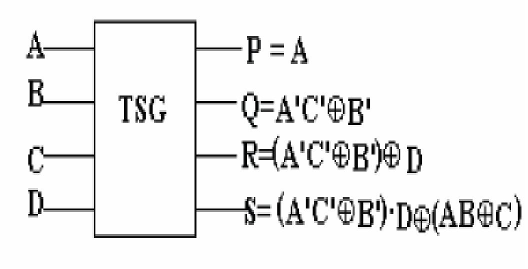

Figure 9. TSG gate

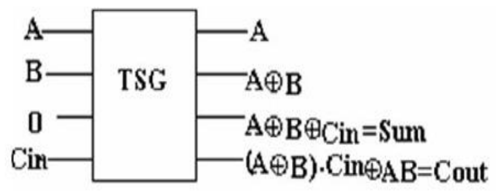

Figure 10. TSG gate as full adder

Figure a describes an 4 input TSG reversible logic gate with 4 outputs as shown above and by making input C as ‘0’ it acts as Full Adder.

Compressors are used to implement arithmetic and digital signal processing architectures for high performance applications. These are used especially in adder structures to reduce the complexity and time delay. These are also used in Multiplier architectures to add all partial products and for final addition. In multiplier architectures the main source of power, delay and area consumption are from how these partial products are accumulated. These compressors are used to reduce time delay and increase its speed for specific architecture. Generally compressors reduce N-input bits to a single sum bit of equal weight to that of the inputs and carry out bit. In usage we had 3:2, 4:2, 5:2, etc. we used only 4:2 compressors with four inputs (x1, x2, x3, x4) and two outputs sum and carry. The 4:2 compressors receive an input Cin from the preceding module of one binary bit order lower in significance, and produce an output Cout to the next compressor module of higher significance as shown in figure 6. Besides, to accelerate the carry save summation of the partial products, it is imperative that the output, Coutbe independent of the input Cin.

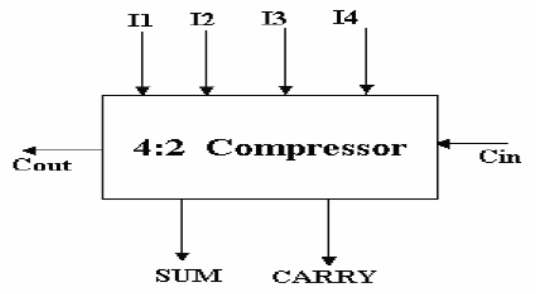

Figure 11. TSG gate as full adder

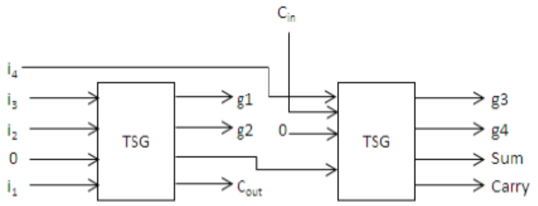

Figure 12. TSG gate as full adder

Basically Multiplier consists of 3 stages

1. Partial Product Generation, 2.Partial Product Addition 3. Final Product Addition. Multiplier essentially consists of 2 operands a multiplicand “Y” and Multiplier “X” and produces a product. In stage 1 each bit is multiplied to produce Partial products. Stage 2 is an important stage where all partial products gets added using various adder structures in a tree like fashion. Stage 3 is used to generate the Final Product. Our proposed multiplier uses Peres gates to generate partial Products, 4:2 TSG based compressors to add

partial products and the same is compared with conventional Multipliers.

Partial Product Generation:

To generate Partial Products we used peres gates because quantum cost per gate is less when compared to other reversible gates. Quantum Cost for Fredkin gate is 5 but for Peres gate it is 4. So we choosen Peres gate to reduce QC. We require 64 gates to generate 64 partial products.

Partial Product Addition:

This paper combines two different technologies like Compressor logics and Reversible Logics for adding Partial Products on Vedic Multiplier and it was observed that number of stages and number of gates used reduces when compared to other existing structures.

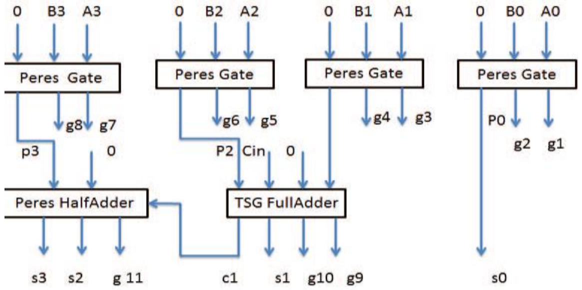

Figure 13. 2x2 bit Reversible Vedic Multiplier

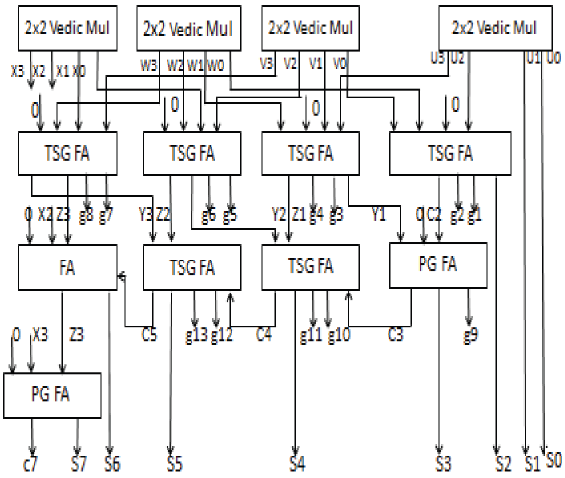

Figure 14.4x4 bit Reversible Vedic Multiplier using 2x2 bit Vedic Multipliers

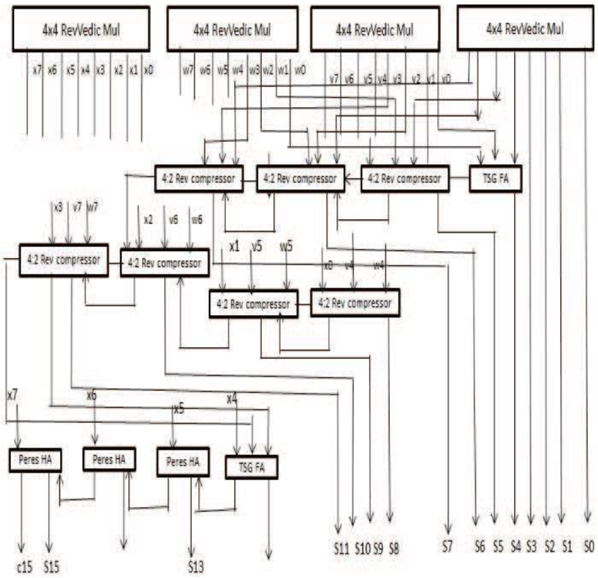

Figure 15. 8x8 bit multiplier using 4x4 bit Multipliers

Final Product Summation

In the proposed method final adders are not required the output of the compressors itself gives Final Product. Hence we can say that complexity of the circuit reduces when compare to conventional multipliers. The same parameter is calculated in terms of Logical Calculations and it was observed that number of calculations are less in vedic multiplier

V. RESULTS

Here in this section applying reversible concept to the adder, which is giving using reversible gates like peers gate, TG gate 4:2 compressors are designed and using all this a novel Vedic multiplier.

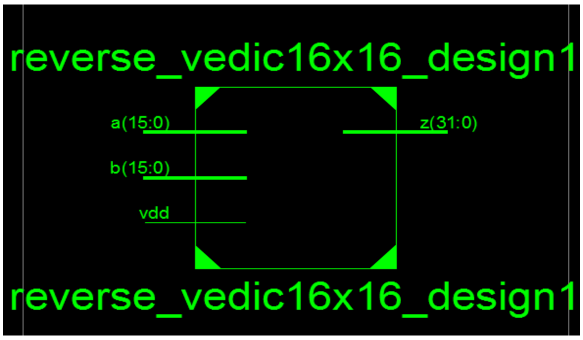

Figure 16. block diagram

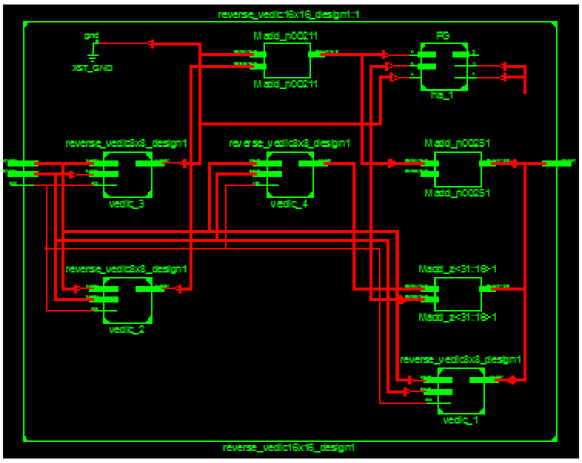

Figure 17. RTL Schematic

Figure 18. simulation results

Table 1. Comparision of multiplier designs

Designs	Dadda multiplier		Reverse vedic multiplier	
	Number of LUT's	Delay	Number of LUT's	Delay
Multiplier 1	124	6.274 ns	109	6.823 ns
Multiplier 2	127	6.080 ns	111	6.833 ns
Multiplier 3	145	5.736 ns	115	6.840 ns
Multiplier 4	158	6.925 ns	124	8.024 ns

VI. CONCLUSION

In this paper we presented four DQ4:2Cs, Compressor based Vedic multiplier has been designed using reversible logic. Which had the flexibility of switching between the exact and approximate operating modes. In the approximate mode, these compressors provided higher speeds and lower power consumption at the cost of lower accuracy .each of these compressors had its own level of accuracy in the approximate mode as well as different delays and power in the approximate and exact modes. These compressors were employed in the structure of 8 bit multiplier to provide a configurable multiplier whose accuracy (as well as its power and speed) could be changed dynamically during the runtime.

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