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Implementation of Low Power CMOS Structure Using Pass Transistor Adiabatic Logic

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ABSTRACT

Power consumption is the important and basic parameters of any kind of digital integrated circuit (IC). There is always a tradeoff between power and performance to meet the systems requirement. System cost is directly affected by power. Adiabatic circuits are those circuits which work on the principle of adiabatic charging and discharging and which recycle the energy from output nodes instead of discharging it to ground. Conventional CMOS circuits achieve a logic '1' or logic '0' by charging the load capacitor to supply voltage Vdd and discharging it to ground respectively. All simulation result and analysis are perform on 90 nm PTM technology using Tanner tool.

Keywords : Power and Performance, Adiabatic Circuit, Charging And Discharging, CMOS Circuits, Tanner Tool

I. INTRODUCTION

Pass Transistor Adiabatic Logic (PAL Logic) refers to the low power scheme that has been used in the present project. It is an adiabatic Complimentary Metal Oxide Semiconductor (CMOS) logic based on the principal of recycling of energy between an AC power clock and the Logic. Common to all the adiabatic (low power) logics is the periodic exchange of energy between the power clock and the logic. The path for the energy transfer depends upon the logic. Logic evaluation follows one of the several possible schemes including the *retractile cascade, regenerative or memory scheme*.

Memory schemes with partial energy recovery are preferred because of much simpler and area efficient implementation. Also, in the memory scheme, each logic stage performs a memory function so that logic outputs may remain valid for use in the next stage even though the logic inputs do not remain constant [1]. Assuming standard CMOS logic implementation, this leads to a loss of $C|V_t|^2$, where V_t is the device threshold voltage (which is of the order of ~1V for 3V supply), accompanies each logic transition when the memory is being erased. Still, its way less than the CV_{dd}^2 loss occurring in the conventional CMOS logic.

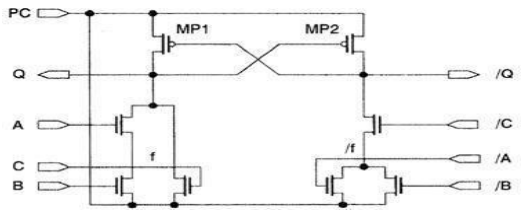

Figure 1a : Schematic of an A.B+C block implemented using the PAL design logic

II. METHODS AND MATERIAL

1. PAL gates

Pass Transistor Adiabatic Logic is a dual rail adiabatic logic with a relatively low gate complexity and it operates with a two phase power clock. It has memory function performed by a pair of cross

coupled PMOS gates and the logic function performed by a pair of true and complimentary pass transistors' NMOS functional blocks (f, f'). Referring to the figure1a,

the implementation of the function A.B+C has been shown using the PAL logic. The power is supplied through a power clock [2]. The inputs make a conduction path, when the sinusoidal power clock is rising, from the input to one of the output nodes (f or f'). The other node will be tristated and kept to zero volts by its load capacitance. This, in turn, causes one of the PMOS transistor to conduct and charge the node that should go to logic one, up to the peak of he power clock. The output state is valid at around the peak of the power clock. The power clock will then ramp down from the top towards the zero value, recovering the energy stored in the output node capacitance.

2. PAL gates cascaded

Cascade of logic gates is provided with alternately connecting it to the power clock (PC) and its 180 shifted signal power clock (PC'). All odd logic states are supplied by the sinusoidal voltage PC and all the even ones by PC'. There are two phases, the evaluate phase and the discharge phase. When the PC is rising it's the evaluate phase of the gate, when it's discharging, it's the discharge phase [3]. So, connecting the cascaded gates with two power clocks differing in phase by 180 we ensure that the discharge phase of all the odd phases coincides with the evaluate phase of the even phases and vice versa. The cascade of four inverters has been shown in the figure 1(b) and the corresponding waveform in figure1(c)

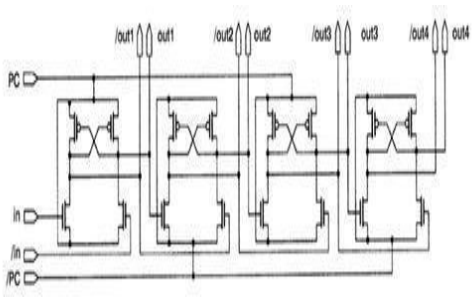

Figure1b : Schematic of four PAL NOT gates connected in cascade using two phase power clock

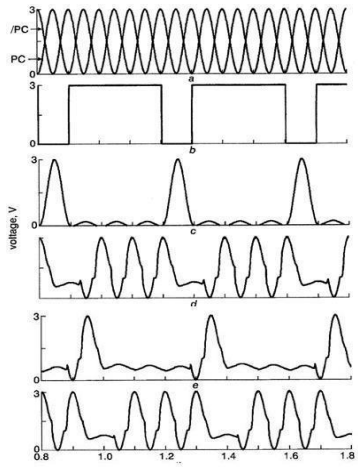

Figure1c: Waveforms for the schematic in fig.1(b)

All the design structures using CMOS Pass Transistors Adiabatic Logic (PAL) were designed and simulated using 90nm CMOS technology and 3V supply at an operating temperature of 27C. Tanner tool has been used for all design and simulations. The basic cell like an Inverter has been designed using appropriate sizing [5].

The Power Clock in all the presented gate simulations has been given using a sinusoidal pulse generated using the concepts developed in chapter 3. Later, after the whole configuration of the circuit, the main Power Clock has been replaced by the designed Power Clock which has been configured using all the bulk circuit parameter of the final circuit in order to generate the sinusoidal power clock. In all the simulation results shown below, we have the power clock input then the input(s) followed by the output.

3. CMOS Inverter using PAL logic

The one input inverter was designed using the conventional CMOS and the PAL technology on the Tanner tool using the 90nm CMOS technology and 3V supply.

Figure 2a: Schematic of Inverter/Buffer based on PAL technology

III. RESULTS AND DISCUSSION

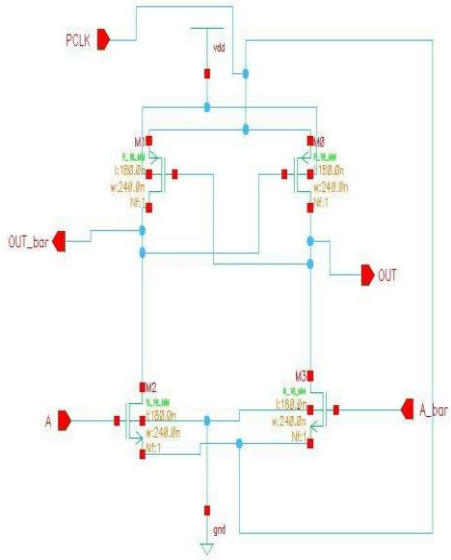

Figure 2b: Simulation result of Inverter based on conventional CMOS technology.

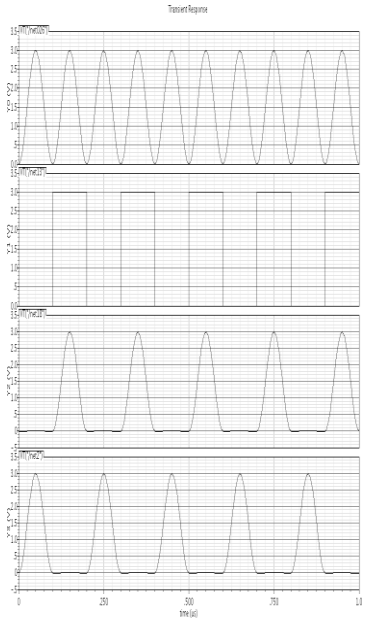

Figure 2c: Simulation result of Inverter based on PAL technology.

Table1. Comparative Table of Power Dissipation of CMOS/PAL Inverter on various frequencies

Sl. No.	Frequency of the Power Clock (MHz)	Power Dissipation using standard CMOS inverter (watt)	Power Dissipation using PAL inverter (watt)
1.	10	0.00000225	0.000000044
2.	20	0.00000461	0.000000211
3.	50	0.0000117	0.00000126
4.	100	0.0000223	0.00000519

IV. CONCLUSION

Simulated Results are achieved from proposed adiabatic CMOS inverter for low power consumption at the low frequency. The comparison of proposed adiabatic logic circuit with conventional logic circuit has proved that power consumption of adiabatic logic circuit is very less as compared to CMOS based technology. All simulated results are shown at 90nm technology using Tanner tool.

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