

Power Dissipation Analysis of Memristor for Low Power Integrated Circuit Applications

Miss Fatima, Reshma Begum

Assistant Professor, K C T Engineering College, Gulbarga, Karnataka, India

ABSTRACT

This seminar reports a memory resistance (memristor) behavior for low power integrated circuit applications. The power dissipation of memristor is analyzed by using Simulation Program with Integrated Circuit Emphasis (SPICE). For power dissipation checking, the memristor is driven by some power supplies: sinusoidal, trapezoidal, triangular, and rectangle waveforms. From the SPICE simulation results, we found that the power dissipation which is driven by the triangular supply waveform is smaller as compared with the other power supplies.

Keywords : Routing, non-repudiation, Byzantine failure, MANET, Security, Authentication, Integrity, Non-repudiation, Confidentiality, Key and Trust Management(KTM).

I. INTRODUCTION

In 1971, Chua argued the existence of forth passive component which is called memristor [1]; however, we had great difficulty finding the physical implementation of memristor. In 2008, the lab members of Hewlett-Packard have implemented the memristor by using Metal-insulator-metal structures based on titanium dioxide [2]. Then, many applications of memristor have been presented (e.g., synapse circuit [3], content addressable memory [4], and dynamic memory [5]). These papers have been reported the circuit configuration and the simulation/implementation results, but have never been the power dissipation analysis. In the integrated circuit design power dissipation analysis is a very important factor, so that we need to know about power dissipation of memristor which is caused by the difference in waveform of power supply. In this seminar, we report an analytical method of low-power consumption for memristor. At first, we investigate a behavioral power-dissipation factor of

memristor by SPICE simulation. This factor will be analyzed by using some power supply waveforms (sinusoidal, trapezoidal, triangular, and rectangle). Secondly, using the obtained results we will design a new low power synapse circuit which has been presented in [3]. Finally, simulation results and conclusion will be summarized.

II. METHODS AND MATERIAL

ORIGIN OF MEMRISTOR

Anyone with a basic knowledge in electrical engineering knows that there are four fundamental circuit variables: Current i , Voltage v , Charge q , and Flux φ . Then it is clear that with these four parameters, there can be six possible combinations for relating them to each other. So far we have complete understanding and control over five of these combinations in which three of them are passive two terminal fundamental circuit elements, namely the resistor R , the capacitor C and the inductor L . Unlike

the active components which can generate energy, these three components are passive elements which are only capable of storing or dissipating energy but not generating it. The behavior of each of the three elements can be described by a linear relationship between two circuit variables. The relationship between 'voltage and current', 'voltage and charge', and 'current and flux' are defined by a resistor, capacitor and an inductor, respectively. Figure shows these three relationships. Moreover, the two other combinations are defined by Faraday's law. Faraday's law shows that the current is the time derivative of the charge and the voltage is the time derivative of the magnetic flux.

Figure shows the relationship between these parameters.

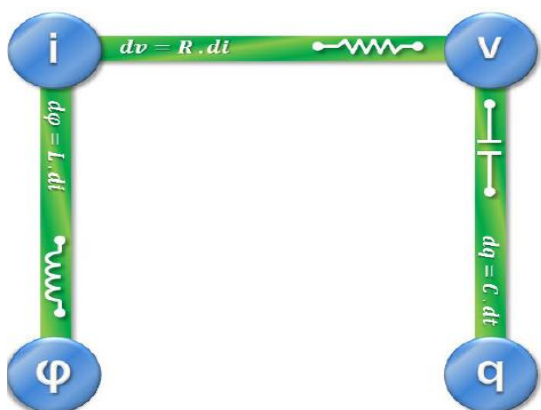


Figure 1. Relations between circuit variables that define resistor, capacitor and inductor.

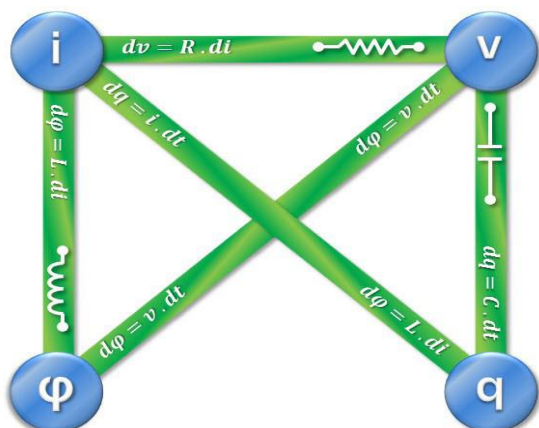


Figure 2. The relation between the four circuit variables known before Chua's paper. Note the missing link between ϕ and q .

The Missing Link

In 1971, Leon Chua, an EE professor from UC Berkeley compared this definition to Aristotle theory of matter. Based on Aristotle's theory, and as it is shown in Figure, all the matters are consisted of four fundamental elements, namely Earth, Water, Air and Fire. There are also four basic properties namely dryness, moistness, hotness and coldness (from Chua's talk in [36]).

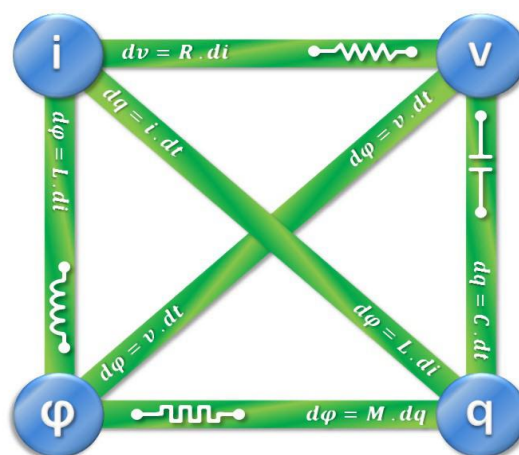
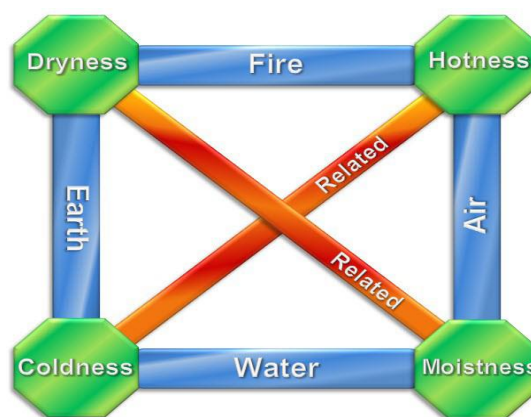


Figure 3. The relationship between the four circuit variables, defining four circuit elements including the memristor

Any of the fundamental elements represent two of the four basic properties. After some inspection Chua found out that there is a similarity between the relationship among above elements and the relationship among electrical circuit parameters. He noticed that there was no element relating the magnetic flux and electric charge. Therefore, he

predicted that based on symmetry, there should be a fourth fundamental circuit element. He called this hypothetical element, “memristor”. The fourth element describes the relationship between the charge and the magnetic flux. But why nobody considered this missing link before is quite an interesting question itself. After that it took about 40 years for the memristor to be actually implemented in a physical form. Figure 3.1(c) Shows the complete relation between all four circuit elements and variables.

3.2 Memristor properties

Flux-charge relation

The $q-\phi$ curve, has a monotonically increasing characteristic. The slope of this curve is the memristance $M(q)$. Hence, the memristance is always positive $M(q) \geq 0$. Based on the passivity condition, a memristor is a passive element if and only if the memristance has a non-negative value. The instantaneous power dissipated by the memristor is given by:

$$P(i) = M(q)i(t)^2,$$

and since $M(q) \geq 0$, the dissipated power is always positive as well.

Therefore, memristor is a passive device. This means that it cannot create or store energy, but only consumes power. Similar to a resistor, a memristor is purely dissipative

FUNDAMENTALS OF MEMRISTOR

The memristor is defined by non-linear algebraic relationship due to the magnetic flux $\phi = \hat{\phi}(q)$ and charge q [1]. Taking the derivative of both sides of $\phi = \hat{\phi}(q)$, we

$$\frac{d\phi}{dt} = \frac{d\hat{\phi}(q)}{dq} \cdot \frac{dq}{dt}$$

From the aforementioned equation, we have:

$$v(t) = \frac{d\hat{\phi}(q)}{dq} i(t) \equiv M(q)i(t)$$

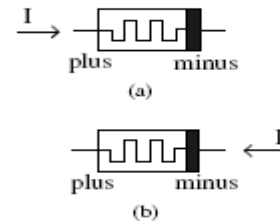


Figure 4. Polarity behavior of memristor. (a) Positive condition: Memristor

becomes a low-resistance. (b) Negative conditions: Memristor has a high

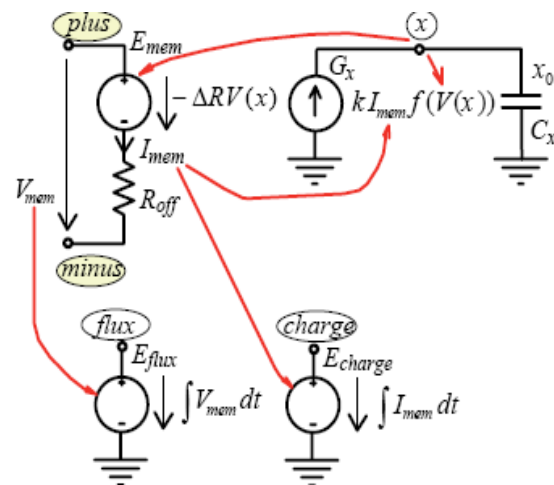


Figure 5. structure of SPICE model

where $v(t) = d\phi/dt$ is voltage of memristor, $i(t) = dq/dt$ is current, and $M(q) = v(t)/i(t)$ is a charge-controlled resistance. From the aforementioned equation, we find that the memristor is a non-linear resistance element which depends on the integral of the current value. Figures 4 show behaviour and structure of SPICE model of memristor, respectively. In Fig 4, when current flows from + to -, memristance (resistance value of memristor) is reduced and then the memristor is turned ON. On the contrary, when current from - to +, memristance is increased and then is turned OFF. Hence, the memristor is like

operated as nonlinear switch. The structure of SPICE model is shown in Fig 4

The relation between the memristor voltage and current is modeled as

$$R_{\text{mem}}(x) = R_{\text{off}} - x\Delta R, \Delta R = R_{\text{off}} - R_{\text{on}}$$

From this equation and the circuit model as shown in Fig. we summarize that the circuit model of memristor resembles RC charge/discharge model of CMOS logics in many respects. Therefore, we will focus on the adiabatic circuit technology to reduce the power consumption of memristor. In the next section, we will briefly explain the adiabatic logic circuit technology with respect to the RC circuit model.

ADIABATIC CIRCUIT TECHNOLOGY

The adiabatic circuit technology is one of the most popular technique of suppressing the energy, it is achieved that voltage across and the current through the on-resistance of metal oxide semiconductor (MOS) becomes always small by using the power supply which has gradual decreasing/increasing voltage (i.e., sinusoidal, trapezoidal, rectangle and so on). Figure 4 shows static/adiabatic CMO equivalent circuit models and their transition voltage/current, respectively. In Fig 5(a), the power dissipation of static CMOS circuit is as following:

$$E_{\text{diss}} = (1/2)CV_{\text{dd}}$$

On the other hand, the power of adiabatic CMOS circuit shown in Fig. 5 has

$$E_{\text{diss}} = (RC/T)CV_{\text{p}}$$

Where T is the time it takes the gate to charge or discharge. In non-reversible circuits, the charging time T is proportional to RC. Reversible logic uses the fact that a single clock cycle is much longer than RC

and thus attempts to spread the charging of the gate over the whole cycle and thus reduces the energy dissipated. In order to extend the charging time of the gate we make sure never to turn on a transistor that has a potential difference between source and drain, and furthermore, once the transistor is turned on, energy flows through it in a gradual and controlled manner. From the aforementioned equation, it is possible to reduce the power consumption when T is decreased where T is a time over which switching occurs. Compared with Fig. 2 and 3, we will get an idea that the power dissipation of memristor can be reduced using gradually decreasing/increasing power source.

The second rule that adiabatic circuits must follow is never to turn off a transistor when there is current flowing through it. The reason for this follows from the fact that transistors are not perfect switches going from on to off instantly. Instead, it gradually changes from on to off when the gate voltage changes. Furthermore, the change is proportional to the speed at which the gate voltage changes.

TARGET APPLICATION FOR LOW POWER MEMRISTOR

To confirm our idea, adiabatic circuit technology will be applied to synaptic circuit [3]. Fig. as described in [3] is a synapse circuit using memristor. This synapse circuit is composed of a doublet pulse generation circuit, a memristor weighting circuit, and a differential amplifier. In the next subsection, we will explain the more detailed weighting circuit and doublet pulse generation circuit for a better understanding of synapse circuit.

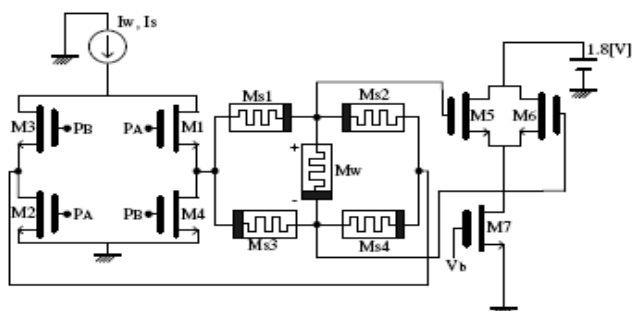


Figure 6. synapse circuit using memristor in[3].

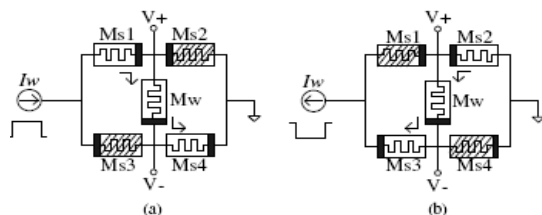


Figure 7. Configurations of the memristor-based sign switching circuit.

- (a) Positive weighting configuration (Ms1=Ms4=Min, Ms2=Ms3=Max).
- (b) Negative weighting configuration (Ms1=Ms4=Max, Ms2=Ms3=Min.)

III. METHODS AND MATERIAL

SIMULATION RESULTS

The typical result provided in this paper was obtained using SPICE simulation with a 0.18 μm , 1.8 V standard CMOS technology. To validate the results, we simulated and compared using sinusoidal, trapezoidal, triangular and rectangle pulses. These pulses is used for determining the value of memristance. A SPICE model of memristor is used as shown in [6]. Figure 8 shows the input waveforms of the synapse circuit when square power source is used, where the sign/weight value setting waveform is IW, synaptic input is a Is. In this simulation we apply some adiabatic power sources to IW.

Fig 7 shows the time transitions required to set the weight resistance value: 1000 Ω . Also, Fig 7.1 shows the comparison results of the energy consumption. From these results, the use of the triangular wave causes the most reduced

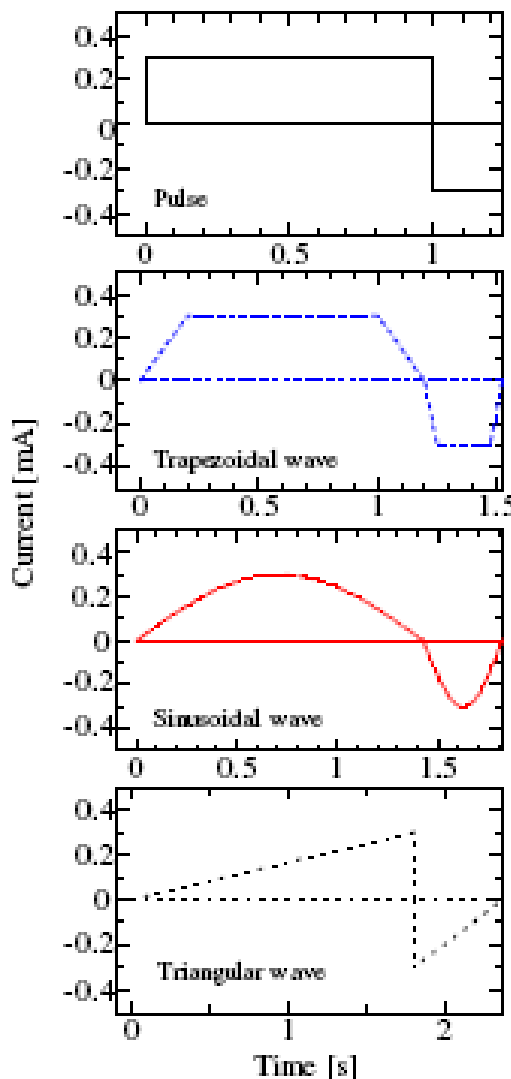


Figure 8. Weight current (IW) conditions (up) and their simulation results of the changing memristance (down).

The results show that the waveforms having slope angle can be set the target value of memristance.

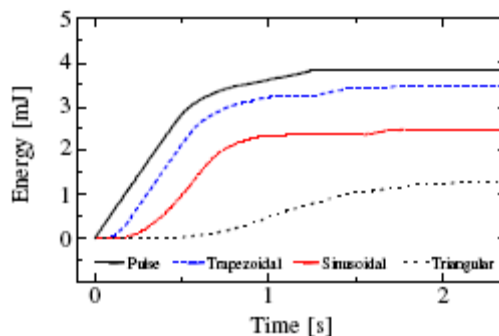


Figure 9. The energy consumption comparison of different waveforms.

APPLICATIONS

Two important characteristic of memristor that is more interesting for researchers are its nanometer scale and the fact that it can have memory properties and latching capabilities. The nanometer dimensions enables up to build high density memories with less power consumption. Moreover, fabricating devices in nanometer scale is cheaper and easier comparing to CMOS fabrication process. And with the memristor memory properties, nanocomputing methods will be possible.

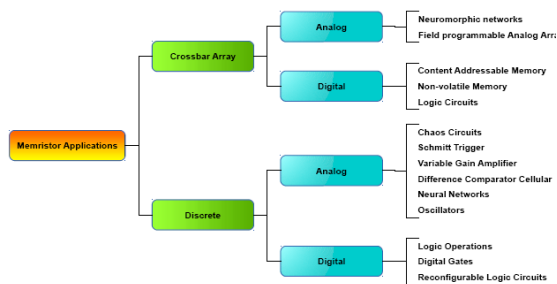


Figure 10. The taxonomy of memristor applications

IV. CONCLUSION

The power dissipation of memristor is analyzed by using Simulation Program with Integrated Circuit Emphasis (SPICE). For power dissipation checking, the memristor is driven by some power supplies: sinusoidal, trapezoidal, triangular, and rectangle wave forms. We have applied the adiabatic circuit technology to synapse circuit, and evaluated the power dissipation. From the SPICE simulation results, we found that the power dissipation which is driven by the triangular supply waveform is smaller as compared with the other power supplies.

V. FUTURE WORK

The initial phase in memristor and memristive systems researches have been completed. Several physical structures have been manufactured and tested and models are designed. Regarding the future impact that the memristor can have during the next 10 years, it is said that it can replace the flash

memories which have a 10 billion dollar per year market. It is also a promising candidate for replacement of DRAM and the magnetic hard disks, where both have 50 billion dollar markets. Moreover, we can build new systems and circuits with unique features. Even if some of the circuits are redesigned in a way by including memristor, it is possible to gain the similar functionality, but with fewer components. This makes the circuits less expensive and with a lower power consumption.

VI. REFERENCES

1. L. O. Chua, "Memristor-the missing circuit element," *IEEE Trans. Circuit Theory*, vol. CT-18, no. 5, pp. 507-519, Sept. 1971.
2. D B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, pp. 80-83, May 2008.
3. H Kim, M. Pd. Sah, C. Yang, T. Roska, Fel, and L. O. Chua, "Neural synaptic weighting with a pulse-based memristor circuit," *IEEE Trans. Circuit and Syst. I*, vol. 59, no. 1, pp. 148-158, Jan. 2012.
4. K Eshraghia, K. -R. Cho, O. Kavehei, S. -K. Kang, D. Abbott, and S.-M. S. Kang, "Memristor MOS content addressable memory (MCAM): Hybrid architecture for future high performance search engines," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 8, pp. 1407-1417, Aug. 2011.
5. Y Takahashi, Y. Urata, T. Sekine, N. A. Nayan, and M. Yokoyama, "Memristor 1T-SRAM with adiabatic driving," in *Proc. IEEE IEDMS 2011*, , Nov. 17-18, 2010, Taipei, Taiwan, 4 pp.
6. Z Bielek, D. Bielek, and V. Biolova, "SPICE model of memristor with nonlinear dopant drift, *Radioengineering*," vol. 18, no. 2, pp. 210-213, 2009.
7. A G. Andreou, K. A. Boahen, P. O. Poulighen, A. Pavasovic, R. E. Jenkins, and K. Strohhahn, "Current-Mode Subthreshold MOS Circuits for Analog VLSI Neural Systems," *IEEE Trans. Neural Netw.* vol. 2, no. 2, Mar. 1991.