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Reversible Logic Based Feynman Gate Using Quantum Dot Cellular Automata Technology

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ABSTRACT

Quantum-dot Cellular Automata (QCA) is a new technology for development of logic circuits based on nanotechnology, and it is an one of the alternative for designing high performance computing over existing CMOS technology. The basic logic in QCA does not use voltage level for logic representation rather it represent binary state by polarization of electrons on the Quantum Cell which is basic building block of QCA. Feynman gate can be categorized as a unique feature to identify a person. Irreversible technology experiences some difficulties like higher dissipated heat. Thus reversible logic is essential where dissipation of heat will be almost negligible. A Reversible circuit using Feynman gate has been proposed in this paper and implemented with QCA. Both the theoretical values and the simulation results are matched which justifies the authenticity of the proposed circuits design. Implementation and testing of the circuit are achieved using QCAD designer tool.

Keywords : Reversible Gates, Feynman Gate, Majority Gate, QCA, Quantum Cost.

I. INTRODUCTION

A revolution has been started off in the field of nano digital circuits as well as nano Communication using QCA. This is one of the upcoming technologies which have left behind CMOS technology in terms of density of the circuits, their functional capacity as well as power consumption. Power consumption is actually very low since QCA does not require any electricity from external source. Based on the arrangement of electrons within the quantum dot cells gives rise to electrostatic charge, this combined with columbic effect gives rise to two stable states when two or more QCA cells are placed side by side. The Bistable nature of the circuit is used for doing any type of computations in digital field. Security is an essential feature which is required to protect our valuable information. As nanotechnology is advancing day-by-day, the nano-communication between nano devices are also increasing. There comes the requirement of security. Reversible formats of JK, SR, T, and D flip-flops are introduced. The defects of a Feynman gate are also analyzed. A secure Nano communication circuit is designed using QCA for the generation of cipher text. In an efficient design for reversible QCA gates has been amended. QCA based nano sensor processor is presented. The nano sensor processor has several functionalities. Similarly, the application of QCA in image processing domain has also been explored. QCA is used to design a multichannel filter for image processing. In image thresholding has been accomplished using QCA. In order to consume low power and to achieve a nano-scale circuit, QCA is being used to perform image negative operation. In Median filtering is carried out binary images using QCA.LSB based Steganography

using QCA is introduced where the LSB bits of a gray scale image is being replaced by the secret message. In contrast to a reversible architecture for LSB based Steganography is proposed.

II. THEORTICAL BACKGROUND

Reversible logic:

Reversible circuits are those circuits that do not lose information and reversible computation in a system can be performed only when the system consists of reversible gate. Reversible computing investigates the relation between energy dissipation and computing at logic level, which leads to the thermodynamic limit of computation. Research on reversible logic is not only of theoretical importance, but also of realistic necessity. Reversible computation is accomplished at logic level by establishing a one to-one onto mapping between the input states and output states of the circuit.

Feynman gate:

Feynman gate is a reversible logic circuit. It consists of two inputs and two outputs as shown in Figure. Input and output has one-to-one mapping. The input vector is I (X, Y) and the output vector is O (O1, O2) and the relation between input and output is given by O1=X, O2 = X ⊕ Y. Since it is a 2 x 2 gate, it has a quantum cost of 1. It is used to copy the input without producing garbage bits.

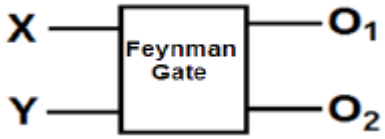


Figure 1. Feynman gate.

Table 1. Feynman Gate's Truth Table

Input		*Output*	
X	*Y*	O_1	O_2
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

III. QCA BASIC BUILDING BLOCK

QCA cell:

Cells are the elementary entities of QCA based circuit and they are usually constituted of four quantum dots positioned at the corners of a square pattern. Each cell is charged with two supplementary electrons which channel from one low potential state to another across a high potential direction and a back plane voltage switches the cell occupancy. The electrons will be located in transversely to each other owing to reciprocal repulsive electrostatic power, possessing the utmost distance between them. A remote cell may be in one of two corresponding energy positions. These positions are called cell polarizations P = +1.00 and P = –1.00 as shown in Figure 1 (a) p = 0 denotes an unpolarized cell which covers no information.

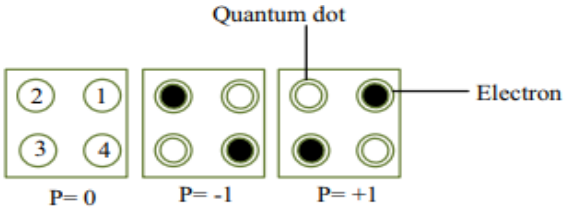


Figure 1(a). quantum cell

QCA wire:

QCA wire encompasses of series of cells where the cells are united one after another. QCA wire is employed to transfer signal from one position to another in a circuit. Logical charges are moved from cell to cell because of the coulomb contacts. There are two modes of alignments in a QCA wire namely binary wire and inverter chain. QCA wires can be either originated up of 45° cells or 90° cells as shown in Figure 1(b) and (c). In case of inverter, if two cells point at 45° with regard to each other their contact will be reverse and for that, these cells are mostly employed for coplanar wire crossings.

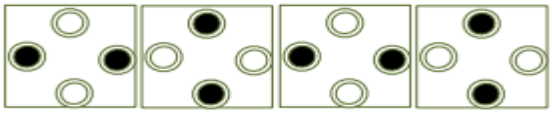


Figure 1(b). 45^0inverted QCA cells

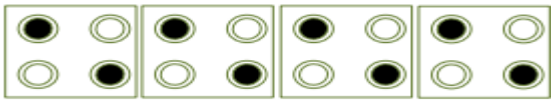


Figure 1(c) . 90^0 inverted QCA cells

Binary wire transfers signal with similar polarity from one place to another, while inverter chain reverses the input cell polarity when odd figures of cells are employed in it.

MAJORITY GATES:

Majority gate is assembled of five QCA cells; a central cell, one output, and three inputs. Polarity of the middle cell, as identified as device cell is imposed, by the coulomb repulsion to be equivalent to the output cell. The device cell at the center of the gate has its least energy when it accepts the polarization of the majority of the three input cells since this is the formation where the repulsion among the electrons in the three inputs cells and the electrons in the device cell is the lowest. So, an arrangement of inverter and majority voter is appropriate to construct an extensive logic set for scheming any circuit.

Majority voter can operate as AND or OR logic gate depending on the static polarity of the third input of the majority voter presented in Figure 1(d) and (e). Logical 2-input AND and 2-input OR functions can be executed using majority voter by putting one input cell to binary "0" and "1", subsequently. The logical equation of the 2-input majority gate can be stated as follows

$$MV(A, B, C) = AB + BC + AC$$

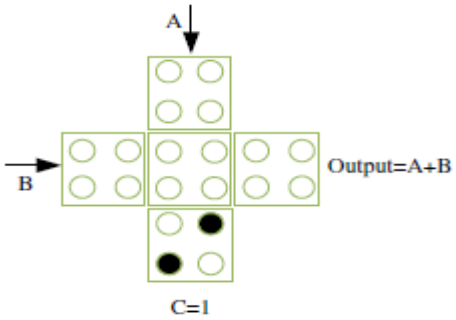


Figure 1(d). OR gate design

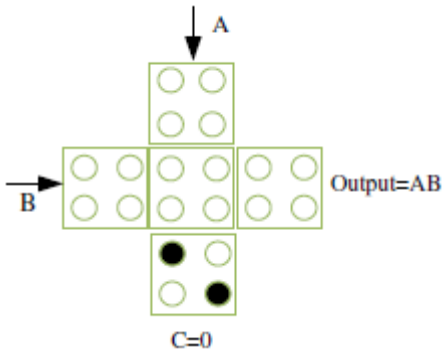


Figure 1(e). AND gate design

QCA clocking mechanism:

To form more complicated QCA devices, the location of QCA cell is not only essential also needs to coordinate the information, so that evade having a signal extending a logic gate and proliferating before the other inputs move the gate. The clock is an electrical region that switches the channeling barriers within a cell, therefore retaining control when a cell may or may not be polarized. QCA clocking is produced of four periods as shown in Figure 2. In each region, a certain potential can adjust the barriers between the dots and the organization of clock zones allows a group of QCA cells to construct a particular calculation and then its positions are stationary and its outputs can be applied as inputs to the following clock zone.

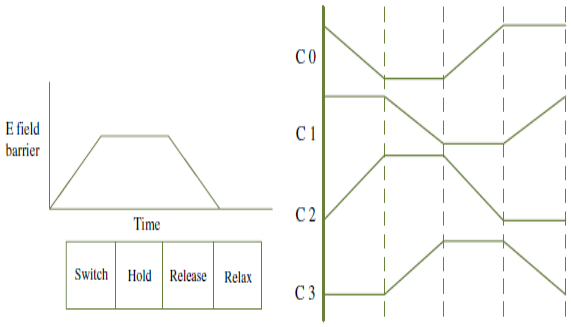


Figure 2. QCA four stage clocking and signal for clocking zones

Switch period: the barrier between dots of QCA cell is elevated and the dots are motivated by the electron of its adjoining as well as electron begins channeling between dots. Thus, the cell turns into polarized.

Hold period: cell barrier stays high and electron cannot channel between dots and the cell keep its existing position.

Release period: barrier between dots are decreased, the electron can channel within dots and cell comes to be unpolarized.

Relax period: barrier remains at lowered and cell stays in unpolarized position.

IV. PROPOSED WORK

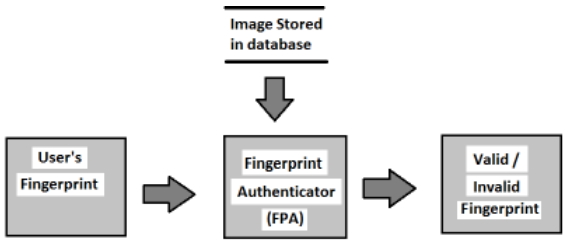
Feynman gate Authenticator:

Feynman gate authenticator (FGA) is a digital logic circuit which validates a user is authenticated or not. It matches one fingerprint with another. If the finger prints resemble then the user can be considered as valid otherwise not. Fig1 (a). Represents the block diagram of the FGA system. An image's information will be stored within the database. A new value is inputted through FGA which is compared with the value already present in the database. If both the Values are matched then the user will be authenticated. The bits of both the images are checked sequentially. When match is found between the bits of both images then '1' is produced at the output F and '0' is generated at output F when mismatch is found. If sequences of all '1' are generated then both the fingerprints are identical. If the generated sequence consists of one or more '0' then the fingerprints are not identical. X, Y represents the inputs to the authenticator circuit. F represents the FGA's output. The generated output at F will be either '1' or '0'. Table 1 displays the truth table of FGA. The corresponding K-map resulting from the Table I is demonstrated in Fig. The Boolean expression generated from the K-map is given by

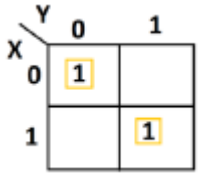
$$F = \overline{X}\,\overline{Y} + XY \qquad (1)$$

Table 2. Truth Table Of Fga

Input	*Output*	
X	*Y*	*F*
0	0	1
0	1	0
1	0	0
1	1	1



(a)



(b)

Figure 2(a). Procedure of verification, (b) K-map for output (F) of FGA circuit

Reversible Feynman gate Authenticator

To design the authenticator circuit, a single OR-gate, two AND-gates, and two NOT-gates are needed, as described in (1). Thus, the unique features of Feynman gate can be used to realize the reversible architecture for the proposed fingerprint authenticator as shown in Fig. 5. If one NOT-gate is placed after the input X of Feynman gate, then X Y + XY will be produced at the output, i.e., FGA X Y XY out = + . The output expression at out FGA is same as expression of F for conventional authenticator as shown in (1). Fig 5 characterizes the block diagram. The other output at line O1 will be considered as garbage data termed as Gar, i.e., O1 =Gar which is equivalent to X , i.e., Gar = X .The reversible FGA receives a Feynman gate from a user in the form of binary values and then verifies it with the information already exist in the database. If match is found between both the information, and the input value will be valid value, otherwise it will

be treated as invalid value. The truth table of the FGA is described in Table 3.

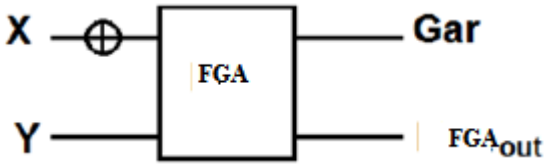


Figure 3. Proposed Reversible Feynman gate Authenticator's block diagram

Table 3. Reversible Fga's Truth Table

Input		*Output*	
X	*Y*	*Gar*	F_{out}
0	0	1	1
0	1	1	0
1	0	0	0
1	1	0	1

QCA based logic equation for reversible can be derived as

$$Gar = \overline{X}$$

$$\mathbf{FGA}_{out} = M\left(M\left(\overline{X},\overline{Y},0\right),M\left(X,Y,0\right),1\right)$$

The QCA generated outline of FGA required only three majority gates and three inverters.

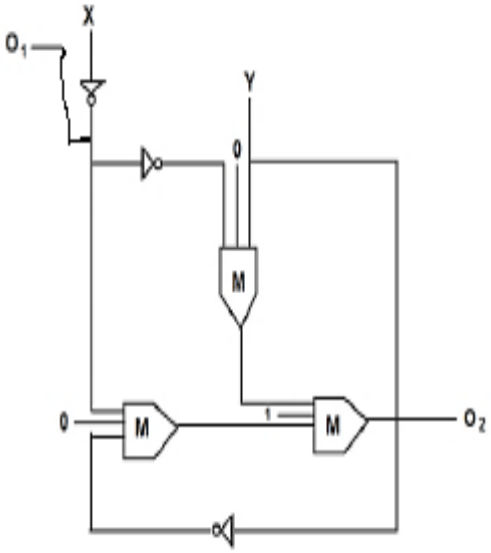


Figure 4. Reversible Feynman gate Authenticator schematic using QCA

V. RESULTS

Layout design:

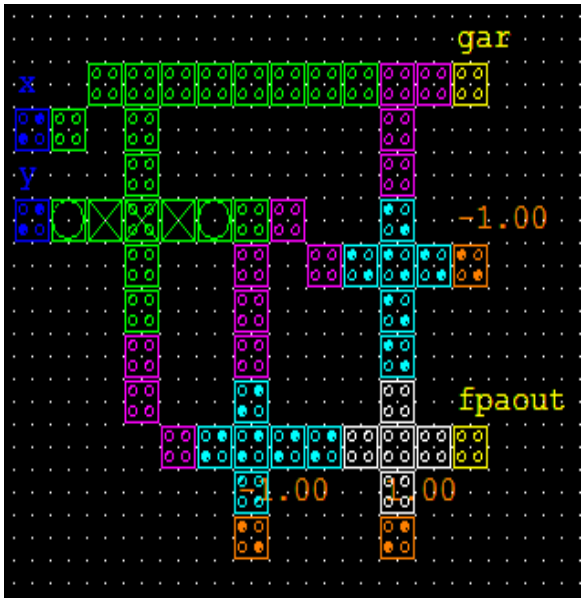


Figure 5. reversible Feynman gate authenticator layout design using QCA

Feynman gate consists of 3 majority gates and 2 inverters whereas FGA consists of 3 majority gates and 3 inverters. Both the designs have identical area of usage and latency. Each of the circuit consists of 58 cells and consumes 0.07 μm2 of total area and its latency recorded 1ns.

Simulation results

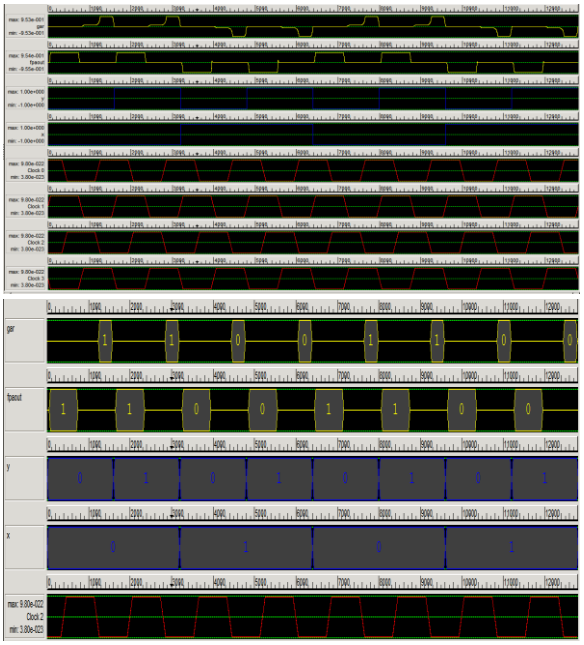


Figure 6. Reversible FGA simulation results

VI. CONCLUSION

The main aim of nanotechnology is to reduce the dissipation of heat as well as to decrease the size of a circuit so that it can be easily embedded within an instrument. QCA technology in combination with reversible logic can be the solution to eradicate these problems. The authentication has become a necessary part of every domain otherwise our valuable data will be stolen and misused. A novel reversible QCA based Feynman gate Authenticator is designed. The suggested reversible Feynman gate increases the security of information through authentication of a valid user. QCA is used to achieve the low power nano-circuit for this FPA. The authenticator circuit has lower quantum cost, i.e., 1. The truth table confirms with the simulation result thereby explains the appropriateness of the circuit. More complex architecture to enhance the security of information can be designed with the proposed FGA circuit.

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