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Four Quadrant Analog Multiplier Based on Squarer Cells

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ABSTRACT

In this paper, a current-mode analog multiplier circuit is proposed that utilizes MOS translinear principle. The parameters of TSMC 0.18μm technology are used to design the proposed multiplier that employs CMOS transistors operating in weak inversion region. Simulations are performed by HSPICE for the circuit to prove its great merits of; low power consumption (100μW), low supply voltage (1.6V), body effect immunity, wide input range (±100nA), bandwidth of 1 MHz, and THD of 4%.

Keywords: Analog Multiplier, Squarer Cell.

I. INTRODUCTION

Recently, the low-power low-voltage analog current-mode circuits have gained an increasing attention. This attention is especially focused on the computing systems that prefer circuits with minimum consumed power, wide dynamic range and good linearity. In the meanwhile, four-quadrant multiplication is one of the great important needed operations in both analog computation and analog signal processing.

Analog multiplier design was first reported in the work of Gilbert [1] which was implemented using BJT. Since then noticeable number of works have been reported specially in CMOS technology [2-4]. The increasing demand for low voltage/low-power integrated circuits has encouraged the development of CMOS current-mode architectures. As in their voltage-mode counterparts, the operation principle of most available current-mode structures lays on drain current either deep in strong inversion [5-7] or in weak inversion region [8-9]. In both cases linearity becomes poorer as the amplitude of input signals increases. Based on the exponential characteristics of MOSFETs in weak inversion region) or BJTs, four-quadrant current multiplier circuits have been designed from such different principles as stacked and folded MTL loops that the circuits need additional supply voltages and manufacture solutions for biasing and being immune from body effect, respectively [4, 10-12].

In this paper, a current-mode analog multiplier is presented which contains two squarer cells with MOS transistors operating in weak inversion region, causing low power consumption and provides exponential applications. The general structure design is based on the translinear loop used in [13] for squarer cells to implement squaring operation applying CMOS transistors working in weak inversion region. Also, [14] and [15] shows RMS-to-DC converter and analog multiplier respectively that they use squarer cell using folded structure through which they obtain other mathematical operations. In [15], authors use the characteristics of weak inversion region of CMOS transistors to reduce power consumption. However, low power designs suffer from low bandwidth which does not matter for biomedical applications not requiring that much bandwidth. Nonetheless, using weak inversion region of MOS transistors, bandwidth and input range would be decreased. The advantage of this circuit is that it does not need additional supply voltage for biasing usually less than main supply

voltage, thereby; it would have less power consumption compared to similar circuits. In addition, translinear loops cause that this circuit would be immune from body effect. The simulation results indicate that the circuit achieves low power, low voltage, and wide input range. This work is organized as; in section II, principle operation of proposed multiplier is presented. In section III, the circuit analysis will be done. Section IV shows the simulation results of the multiplier's circuit. Section V includes conclusions of the proposed multiplier.

II. Principle Operation of the Multiplier

According to fig. 1, circuits of the first category only can act as a one quadrant Multiplier but the second are often able to implement a four-quadrant multiplier. Block diagrams of figure 1 have been implemented by two methods of trans-linear scheme and non-trans-linear scheme. Nontrans-linear multipliers use various schemes for implementing multiplication function. Dependence on circuit parameters and supply voltage are main disadvantages of non-trans-linear multipliers; also, approximation is used for realization of some of them. Trans-linear multipliers don't have these problems and have pure current relation in their output [16].

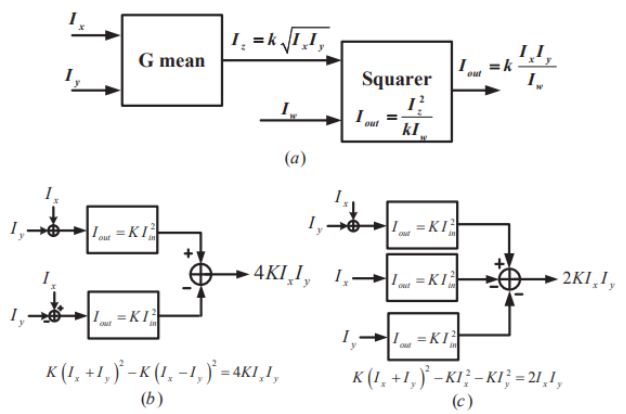

Figure. 1. Block diagram of the proposed multiplier [16]

III. CIRCUIT ANALYSIS

A. Squarer Circuit

The squarer circuit includes ABS block shown in fig. 2. The structure of the squarer cell used in this paper is based on the ABS and squarer. This structured has been chosen due to the fact that it uses translinear loop with the transistors working in weak inversion area making the circuit suitable for biomedical applications consuming lower power. In addition, this structure helps with having more input signal range. However, the disadvantage of this structure is that due to the fact that it uses ABS circuit for making the squarer cell four-quadrant—ABS circuit is made of current mirrors—the total THD goes up. But, for the applications requiring lesser THD, more precise current mirror can be used to reduce the THD. The circuit structure consists of the transistors M3-M6 operating as a current mirror, the transistor M2 connected in cascade to the mirror input and the transistor M1 is used for biasing. In the case of the positive input and the transistor M1 is used for biasing. In the case of the positive input signal current is passed through node X and Vgs2>0 the transistors M2 is ON, therefore, the output signal current of the absolute-value circuit IABS is equal to the input signal Iin, (IBIAS=Iin). In the case of the negative input current is passed through node X and Vgs2<0 the transistor M2 is OFF, transistor M3 can be copied the current through the transistor M6 (Id3= Id6). Therefore, the output signal current equals to the absolute of its input signal current, Iabs=|Iin|.

$$V_{gs12}+V_{gs13}=V_{gs14}+V_{gs15} \quad (1)$$

The drain current of MOS transistor that operates in weak inversion is given by:

$$I_D = I_0\left(\frac{w}{l}\right)e^{\frac{V_{gs}}{nV_T}}\left(1-e^{\frac{-V_{DS}}{nV_T}}\right) \quad (2)$$

Where VT is the thermal potential, I0 is a device dependent coefficient, n represents the subthreshold

slop, W is the width of the gate and L is the length of the gate. If Vds>4VT, then (2) can be re-written as:

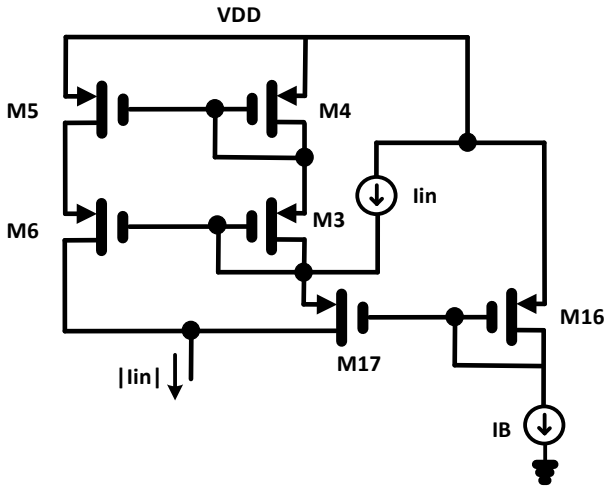

Figure. 2. Absolute-value circuit of the RMS-to-DC converter.

$$I_D = I_0(\frac{w}{l})e^{\frac{V_{gs}}{nV_T}} \quad (3)$$

From equation (1) and (3), it can be deduced:

$$\frac{I_{12}}{\left(\frac{W}{L}\right)_{12}.I_0}.\frac{I_{13}}{\left(\frac{W}{L}\right)_{13}.I_0} = \frac{I_{14}}{\left(\frac{W}{L}\right)_{14}.I_0}.\frac{I_{15}}{\left(\frac{W}{L}\right)_{15}.I_0} \quad (4)$$

If (w/l)12. (w/l)13=(w/l)14. (w/l)15, then equation (4) can be shown as:

$$I_{12}.I_{13} = I_{14}.I_{15} \quad (5)$$

From the circuit analysis in Fig. 2, I15 = Isq, I14=IB and I12=I13=|Iin|, thus equation (6) can be written as:

$$|I_{in}|^2 = I_B.I_{sq} \rightarrow I_{sq} = |I_{in}|^2 / I_B \quad (6)$$

Where Isq is the output current of the squarer circuit.

IV. The Proposed Multiplier Circuit

The proposed Circuit is designed based on the Fig. 1(b) which uses two squarer circuits. According to this structure, we used two squarer cells shown in fig. 3, the output of which is nothing but $4KI_{in1}I_{in2}$. In this equation, K is the multiplication coefficient which is determined by bias current ($K = I_B$).

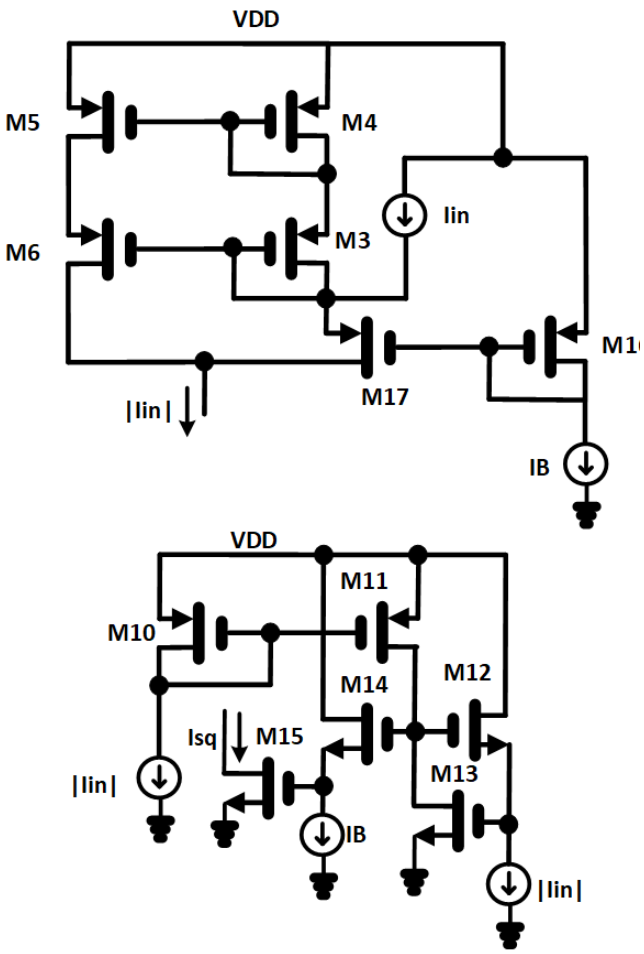

Figure. 3. The squarer with the absolute-value circuit

V. SIMULATION RESULTS

The performance of the circuit has been studied through simulation results using, MOS transistor provided by the 180nm CMOS TSMC process HSPICE software. The supply voltage and power dissipation are 1.6V and 100μW, respectively. To bias the devices in the weak inversion region, the bias current is set to 400nA. Both I_{in1} and I_{in2} are between $\pm$ 100nA.

Fig. 4 shows the application of the proposed multiplier as an amplitude modulator. The modulation is performed when I_{in1} and I_{in2} are the input sinusoidal signals which have the amplitude of 100nA and the frequency of 100 KHz and 10 KHz, respectively.

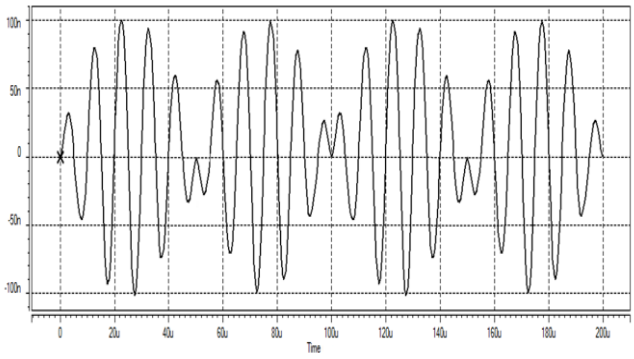

Figure. 4. Multiplication performance of the multiplier.

Fig. 5 and 6 show frequency responses of the output current I_{out} versus the input currents I_{in1} and I_{in2} in the proposed multiplier, respectively. Where a dc current of 100nA is applied to I_{in2} while I_{in1} is sinusoidal signal with the variable frequency in Fig. 5 and vice versa in Fig. 6. The -3db bandwidth is approximately 1 MHz for both. The summary of simulation results is shown in Table. I.

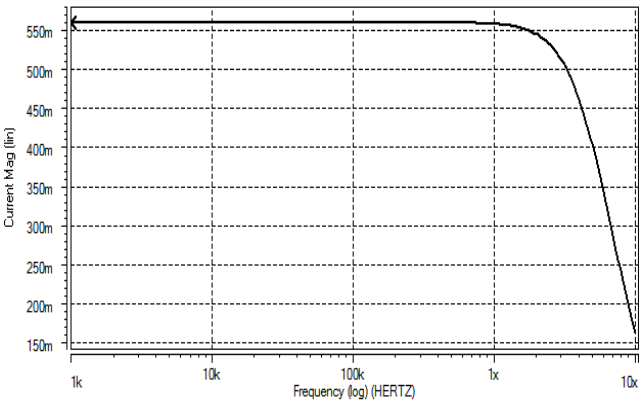

Figure. 5. Frequency response of I_{out} / I_{in1}

VI. CONCLUSION

In this paper, a current mode multiplier based on MOS translinear loops operating in weak inversion is presented. We used weak inversion region of CMOS transistors to help the circuit consumes less power. We used the topology of using three squarer cells for building our analog multiplier. The proposed multiplier has many applications for a wide range of analog signal processing. We analysed the circuit by several mathematic equations to show how our structure reach to a multiplier circuit. The circuit has been designed in 180nm technology process with supply voltage of 1.6V. The simulations were done through HSPICE software. Simulation results have been given to confirm the validity of the theoretical analysis.

The simulation results show that this circuit consumes around 100µW with the bias current of 400nA and supply voltage of 1.6V. Also, this circuit can be used for the applications requiring the input signal amplitude less than 100nA. Therefore, this circuit can be used for biomedical applications. In the future works, the authors will show how multiplication operation can be done through two squarer cell instead of three squarer cell. This idea will help the circuit to be simpler bringing about low power consumption which is needed for biomedical applications.

TABLE I. THE SPECIFICATIONS OF THE PROPOSED MULTIPLIER

Technology (nm)	Power Con/Supply Voltage	Bias Current	Input Range	Non-Linearity (%)	THD (%)
180	100µW/1.6V	400nA	±100	5	4

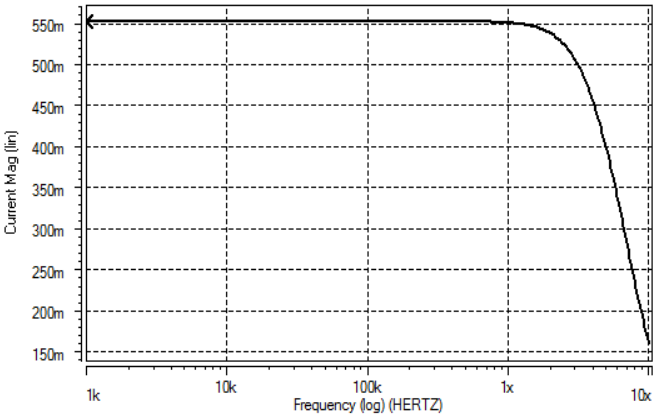

Figure. 6. Frequency response of I_{out} / I_{in2}

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