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A Survey on Different Multiplier Architectures

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ABSTRACT

This paper presents a comparative analysis of different multiplier architectures. The different multipliers architectures are array multiplier, a column bypass multiplier, row bypass multiplier and an array multiplier using Reversible Logic schemes. The multipliers are implemented on Spartan 2 FPGA. The architectures are compared in terms of critical path delay, power dissipation and area (resource usage in FPGA). The different multipliers are compared in terms of dynamic power consumption due to the scaling effects on leakage current. Each of these multipliers has its own trade-offs between power and delay. At last a novel multiplier is proposed, in which the number of layers is reduced to three, this will reduce the hardware resource usage and power consumption of design.
Keywords - Low Power, Multiplier, Switching Delay, bypassing techniques, reversible logic.

I. INTRODUCTION

Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets – high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation.

It is well known that Multipliers consume maximum power in DSP computations [1]. Hence, it is very important for modern DSP systems to design low-power multipliers to reduce the power dissipation. In low-power multiplier design, many researcher experiments & find out results on the reduction of the switching activities [2] have been published. Besides that, a simple and straightforward approach [3] for low-power multiplier is to design a low-power Full Adder to reduce the power dissipation in an array multiplier. The other designs are proposed to reduce the power dissipation in a multiplication operation by interchanging dynamic operands [4] or using partially guarded computation [5]. Furthermore, to minimize power dissipation architectural modification can be used via row bypassing [6] or column bypassing [7] techniques. Based on the concept of theory row and column bypassing techniques for the reduction of the power dissipation, a low-power 2 - dimensional bypassing based multiplier [8] and a low-power row-and- column bypassing-based multiplier [9] are further proposed. However, the introduction of the extra bypassing circuit decreases the ability of minimize the power dissipation, and it also induces extra delay in the circuit. The paper is organized as follows in section II related work is given, in section III, IV and V array, column bypass and row bypass are discussed respectively. In section VI comparison of different multiplier architecture s are discussed. In section VII conclusion and in section VIII a novel multiplier is briefly explained.

II. METHODS AND MATERIAL

A. Related Work

The multiplication of two 4 bit numbers is shown in the figure 1.

			Y=	Y3	Y2	Y1	Y0
			X=	X0	X0	X0	X0
				Y3X0	Y2X0	Y1X0	Y0X0
			Y3X1	Y2X1	Y1X1	Y0X1	
		Y3X2	Y2X2	Y1X2	Y0X2		
	Y3X3	Y2X3	Y1X3	Y0X3			
P7	P6	P5	P4	P3	P2	P1	P0

Figure 1 : 4 X 4 Array Multiplication

An example of above multiplication process is shown in figure 2:

			Y=	1	0	0	1
			X=	1	1	1	0
				0	0	0	0
			1	0	0	1	
		1	0	0	1		
	1	0	0	1			
0	1	1	1	1	1	1	0

Figure 2 : 4 X 4 example of array multiplication

Generally AND & OR gates are used to generate the Partial Products, PP, If the multiplicand is N-bits and the Multiplier is M-bits then there is N* M partial product. The way that the partial products are generated or summed up is the difference between the different architectures of various multipliers.

For CMOS circuits design, the power dissipation can be divided in two categories as static power dissipation and dynamic power dissipation. In general, static consumption is from the leakage current and dynamic consumption is from the switching transient current. For static power dissipation, the consumption is proportional to the number of the used transistors. For dynamic power dissipation, the consumption is provided from the charging and discharging of load capacitance. The average dynamic dissipation of a CMOS gate is

$$P\ avg = \tfrac{1}{2}\ CfV_{dd}N$$

Where C is the load capacitance, f is the clock frequency, VDD is the power supply voltage and N is the number of switching activity in a clock cycle .Hence, it is very important for modern DSP circuit application to develop low-power multipliers to minimum the power dissipation.

In this paper we present various techniques are shown to minimize dynamic power dissipation in digital multipliers, concentrating on the switching activity. There have been proposed a lot of techniques to reduce the switching activity of a logic circuit design. To reduce the power dissipation of an array multiplier, the simplest approach is to design a full adder (FA) that consumes less power. The other method is to reduce the switching activities by architectural modification via row or column bypassing techniques [4]. The bypassing technique disables the operation in some rows or columns to minimize the power dissipation. For the parallel multiplier, the array implementation is the Braun's design. The components used in the Braun's design are full adder as well as AND gate.

B. Array Multiplication

In array multiplier, each partial product is generated by taking into account the multiplicand and one bit of multiplier each time. The Impending addition is carried out by high-speed carry-save algorithm and the final product is obtained by employing fast adder – the number of partial products depends upon the number of multiplier bits. A 4x4 array multiplier is shown in Fig. 3. The structure of the full adder can be realized on FPGA. Each products can be generated in parallel with the AND gates. Each partial product can be added with the sum of partial product which has previously produced by using the row of adders. The carry out will be shifted one bit to the left and then it will be added to the sum which is generated by the first adder and the newly generated partial product. The shifting would carry out with the help of Carry Save Adder (CSA) and the Ripple carry adder or any fast adder can be used for the final stage. [10].

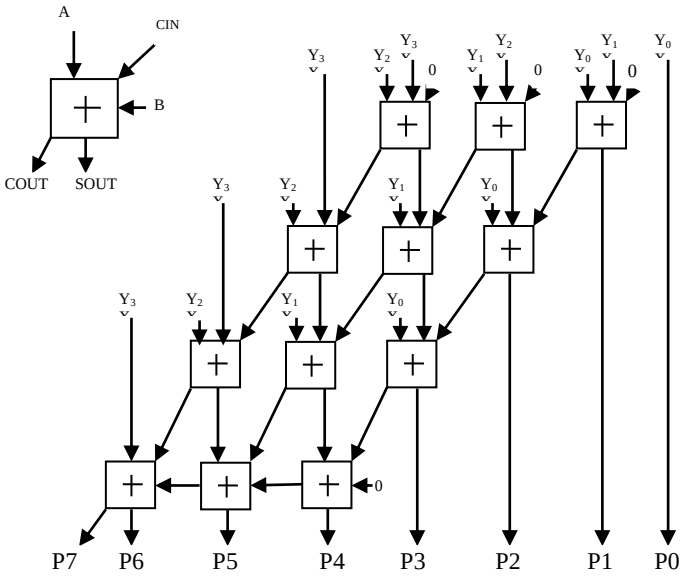

Figure 3: Array Multiplier

C. Column Bypass Multiplication

Multiplier designs in which columns of adders are simply are bypassed is called column bypass multiplier. In this process, the mathematical operations in a column can be disabled if the corresponding bit in the multiplicand is 0. A low-power column-bypassing multiplier, the addition multiplication operations in the (i+1)-th column can be bypassed if the bit, ai, in the multiplicand is 0, i. e., all partial products ai bj, $0 \leq j \leq$ n-1, are zero. In the multiplier design, the modified Full Adder is simpler. Each modified Full Adder in the Carry Save Adder array is only attached by two tri- state buffers and one 2-to-1 multiplexer. As the bit, ai, in the multiplicand multiplier, the addition mathematical calculation in the (i+1)-th column can be bypassed if the bit, ai, in the multiplicand is zero, i. e., So all partial products ai bj, $0 \leq j \leq$ n-1, are zero. In the multiplier design, the modified Full Adder is simpler. Each modified Full Adder in the Carry Save Adder array is only attached by two tri- state buffers and one 2-to-1 multiplexer. As the bit, ai, in the multiplicand is zero, their inputs in the (i+1)-th column will be disabled and the carry output in the column must be set to be 0 to produce the correct output. Hence, the modification protecting process can be achieve b adding an AND gate at the outputs of the last row [10].

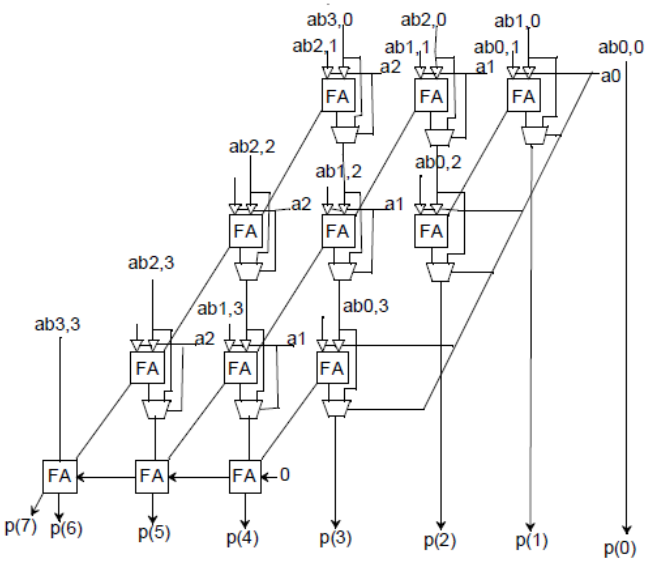

Figure 4: Column Bypass Multiplier

D. Row Bypass Multiplication

This is a modified version of Braun's multiplier which is a parallel multiplier and contains adders in array form. In this method transition activity optimization is achieved through bypassing row of adders which are redundant. It's known that in multipliers, partial products are created by ANDing the multiplicand bits with the multiplier bits one by one.

It is always possible that a bit in the multiplier is a zero, in this case, as the zero bit enters as one of the input of the AND gate to produce a partial product, zero being the dominating factor, forces the output to be zero, this means that the complete row of partial product becomes zero. Now adding elements of this row, in adder circuit present in the array of full adders is merely wastage of energy, as adding a zero bit yields the same output as it was before adding it. So, in this multiplier circuit it is proposed to dynamically bypass such additions by disabling the complete row of adders, thus decreasing the number of signal transitions in the carry-adder array without affecting the result.

For example, let X2 bit present in the multiplier be 0. In this case, the Carry save adder in the second row can be bypassed as marked in red, and the SUM outputs from the first row can be fed directly to the third row CSA using 2:1 MUX, and the carry-bits are passed downwards instead of to the right. To take care of the carry-bit of right-most adder cell, extra circuits are added in the circuitry of modified Braun's multiplier as marked in blue in the circuit diagram of Row-bypassing precision multiplier.

In the internal structure of adder cell used in Row-bypassing multiplier, the select line of the 2:1 multiplexers and the select line of Tri-state buffers is taken to be the same bit of multiplier element in which row the adder circuit lies.

Whenever it's detected that the select line is zero, the output of the previous adder is passed through the multiplexer to the input of the next adder, and in the same time the partial product is interrupted to enter the adder circuit with the help of Tri-state buffer present in the input. Thereby results in bypassing the complete row of adders.[10]

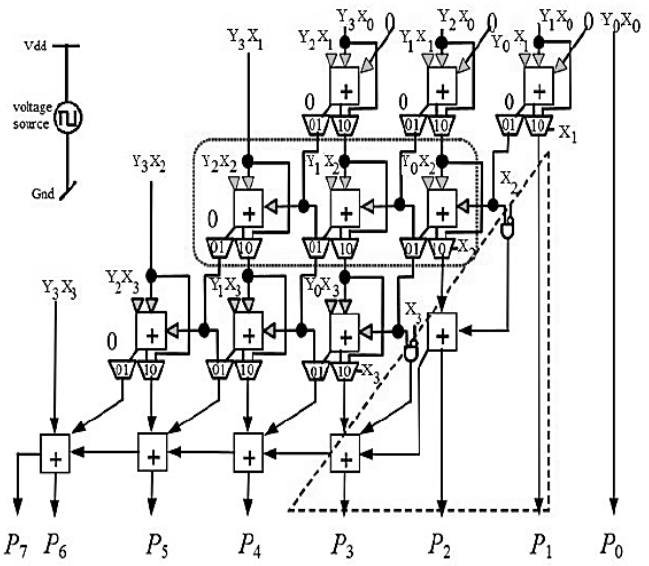

Figure 5: Row Bypass multiplier

E. Row Bypass Multiplication

Reversible logic has emerged as one of the most important approaches for the power optimization with its application in low power VLSI design. They are also the fundamental requirement for the emerging field of the Quantum computing having with applications in the domains like Nano-technology.

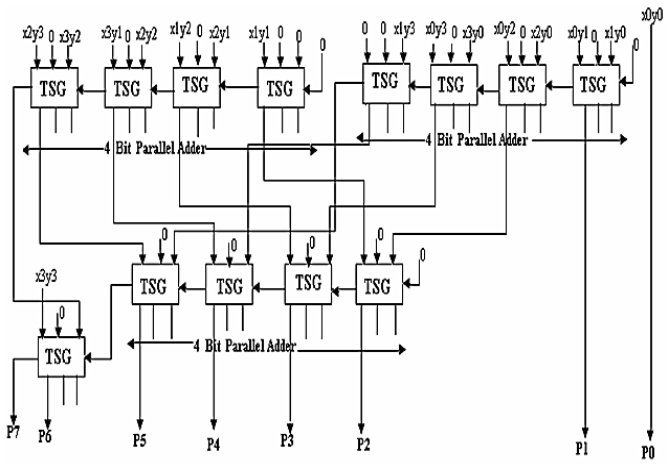

Figure 6: Reversible Multiplier

III. RESULTS AND DISCUSSION

Comparison of different multiplier architectures

A brief comparison of above mentioned five multiplication techniques is discussed in the following sections in terms of delay, power and area.

a) In Terms of Power

i. Column-bypassing multiplier consumes more power compared to 2-D bypassing multiplier but less power when compared to Row-bypassing multiplier.

ii. Row-bypassing multiplier consumes more power when compared to Column-bypassing multiplier, but less power when compared to standard Braun's multiplier.

iii. Braun's multiplier having no bypassing technique consumes maximum power.

b) In Terms of Area

i. Area consumed by Row-bypassing precision multiplier is much less than that of 2-D bypassing multiplier, but greater than that of Column-bypassing multiplier.

ii. Area consumption of Column-bypassing multiplier is lesser than that of both 2-D bypassing and Row-bypassing precision multipliers, but is greater than the area consumed by Braun's multiplier.

iii. Braun's multiplier requires minimum area, when compared to other low power multipliers.

c) In Terms of Delay

i. Delay observed in Column-bypassing multiplier is lesser than that of 2-D bypassing precision multipliers, but is greater than that observed in Row-bypassing multiplier.

ii. Delay in Row-bypassing precision multiplier is much less than that of 2-D and Column bypassing multiplier, but greater than that of basic Braun's multiplier.

iii. Braun's multiplier exhibits minimum delay when compared to other low power multipliers.

Table 1 shows the tabular comparison of different parameters of multipliers.

Table 1: Design summary of different multiplier architectures [11]

Parameters	***Array***	***Row Bypass***	***Column Bypass***	***Reversible***
Device	*Spartan2*	*Spartan2*	*Spartan2*	*Spartan2*
Power Consump.	*44mW*	*39mW*	*35mW*	*43mW*
Time Delay	*21ns*	*51ns*	*14ns*	*30ns*
Number of LUTs	*590*	*921*	*941*	*600*

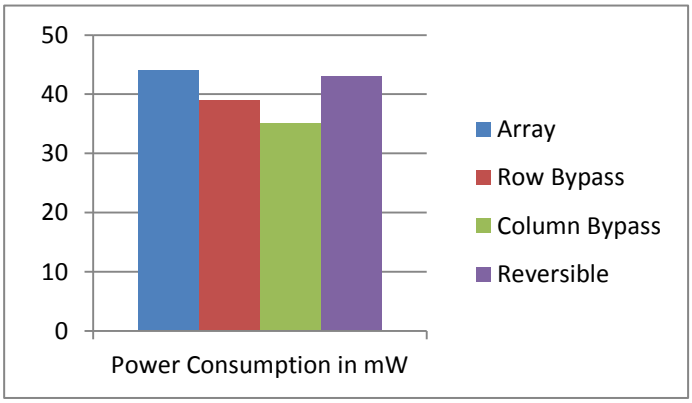

Figure 7: Bar Graph – Power Consumption

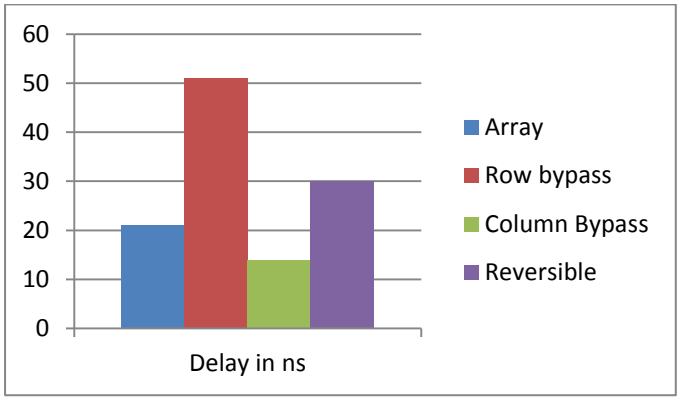

Figure 8: Bar Graph – Delay

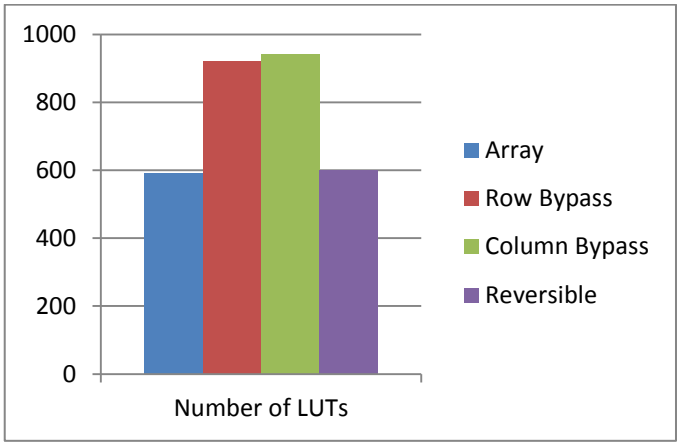

Figure 9: Bar Graph – Number of LUTs

IV. CONCLUSION

According to calculations of switching activity, analysis of area overhead in transistors, the extra transistors also consume more power in the bypassing-based multipliers. In general, more number of additional transistors in the bypassing based multiplier design minimizes the ability of power reduction in low-power designs. Besides that, the ability of the power reduction in the Simple Full adder-based designs, column bypassing designs and Reversible based designs depends on the bit patterns of the tested examples. The experimental results show that column-bypassing design consumes less power in comparison to the extra bypassing logic circuits and Reversible designs. The multiplier with Simple Braun's array has less delay compared to the array bypass multiplier, reversible but the power consumption is higher. The low power bypass multiplier performs best in terms of power consumption but delay performance is comparatively poor. So above discussion among different multiplier architectures low power Bypass column multiplier is better.

V. FUTURE SCOPE

We have seen that bypass techniques used additional logic circuits to reduce the dynamic power consumption. A novel multiplier can be designed by using the concept the resource reuse, in this multiplier only three rows of full adder are required for any size of architecture. All the layers between first layer and last layer in array multiplier is replaced by a single layer of full adder. In this design the first and last row is same as in an array

multiplier but the middle layer of full adder is reused n times, where n is the size of the architecture, i.e. the inputs to the middle layer is changed every time and it is reused. This will reduce area and power consumption, but this will increase latency of the design.

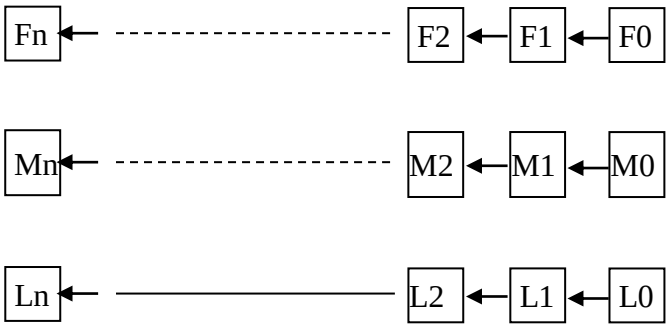

Figure 10 : Novel multiplier with resource reuse

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