© 2016 IJSRSET | Volume 2 | Issue 1 | Print ISSN : 2395-1990 | Online ISSN : 2394-4099
Themed Section: Engineering and Technology

High Speed Area Efficient Vedic Multiplier using Barrel Shifter

Vikram Singh, Yogesh Khandagre
ECE Department, Trinity Institute of Technology & Research, Bhopal, India

ABSTRACT

This paper describes the implementation of an 8-bit Vedic multiplier enhanced in terms of propagation delay when compared with conventional multiplier like array multiplier, Braun multiplier, modified booth multiplier and Wallace tree multiplier. In our design we have utilized 8-bit barrel shifter which requires only one clock cycle for 'n' number of shifts. The propagation delay comparison was extracted from the synthesis report and static timing report as well. The design could achieve propagation delay of 8.547 using barrel shifter in base selection module and multiplier.

Keywords: Barrel Shifter, Base Selection Module, Propagation Delay, Power Index Determinant

I. INTRODUCTION

Vedic mathematics has proved to be the most robust technique for arithmetic operations. In contrast, conventional techniques for multiplication provide significant amount of delay in hardware implementation of n-bit multiplier. Moreover, the combinational delay of the design degrades the performance of the multiplier. Hardware-based multiplication mainly depends upon architecture selection in FPGA or ASIC. [5]

Arithmetic operations like addition, subtraction and multiplication are essential in different digital circuits to boost the process of computation. Vedic mathematics is the great technique for arithmetic operations. Whereas conventional techniques for multiplication gives significant amount of delay in hardware implementation of n-bit multiplier. This delay degrades the performance of the multiplier.

In this work our aim is to reduce the propagation delay of Vedic multiplier using barrel shifter. The "Nikhilam Sutra" implemented is modified. By using the Urdhva Tiryagbhyam barrel shifter in the delay will reduce when compared with conventional multipliers.[8]

Section II System Description
Section III Vedic Multiplier Using Urdhva Sutra Architecture Section IV Barrel Shifter Architecture
Section V Vedic Multiplier Using Barrel Shifter
Section VI Simulation Result
Section VII Conclusion

II. METHODS AND MATERIAL

A. System Description

Assume that the multiplier is 'X' and multiplicand is 'Y'. Though the designation of the numbers is different but the architecture implemented is same to some extent for evaluating both the numbers. The mathematical expression for modified nikhilam sutra is given below.

$$P = A \times B$$
$$P = 2^{k2}(A \pm C2 \times 2^{(k1-k2)}) \pm C1 \times C2 \leftarrow (1)$$

Where k1, k2 are the maximum power index of input numbers A and B respectively. C1 and C2 are the residues in the numbers A and B respectively.
The hardware deployment of the above expression is partitioned into three blocks.

- Base Selection Module
- Power index Determinant Module
- Multiplier.

The base selection module (BSM) is used to select the maximum base with respect to the input numbers.

The second sub-module power index determinant (PID) is used to extract the power index of k1 and k2. The multiplier comprises of base selection module (BSM), power index determinant (PID), subtractor, barrel shifter, adder/subtractor as sub-modules in the architecture.

B. Vedic Multiplier

"Vedic Mathematics" refers to a technique of calculation based on a set of 16 Sutras. Vedic sutras are the gift of ancient Indian mathematics. For large number of mathematical operations they apply. By using these sutras saves a lot of time compared to conventional computations. The faster processing speed is major improvements in processor technologies. The Vedic mathematics technique is totally different.

Many architectures of multiplier have been reported but the performance of multiplier was improved in proposed design. The architecture in [8] is changed using barrel shifter so significant amount of clock cycles are reduced so speed increases. The performance of the proposed multiplier is compared with the previously implemented multipliers.

The calculation is sufficiently able to be employed for the duplication of whole numbers and also binary numbers. The expression "Urdhva Tiryagbhyam " started from two Sanskrit words Urdhva and Tiryagbhyam which mean" vertically" and "crosswise" respective. Fig. 1 represents the general multiplication procedure of the 3x3 multiplication. This process is called as array multiplication technique. It is an efficient multiplication technique when the multiplier and multiplicand lengths are small, for the larger length multiplication this technique is not good because a large amount of propagation delays are involved in these cases. To overcome this problem we are describing Nikhilam sutra for calculating the multiplication of two larger numbers

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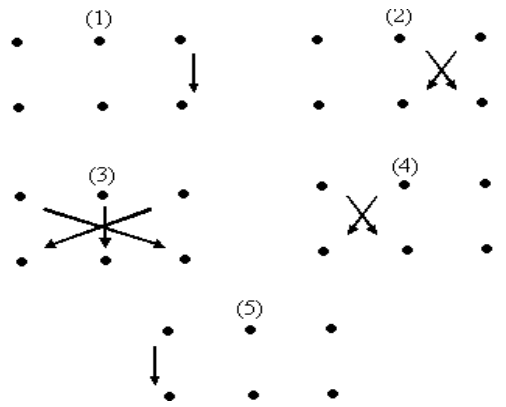


Figure 1 : Multiplication procedure using "Urdhva - Tiryagbhyam" sutra

Example:-

```
      123
    x 456
  ________
    56088
  ________
```

C. Barrel Shifter Architecture

The base selection module and the power index determinant form integral part of multiplier architecture. The architecture computes the mathematical expression in equation1.Barrel shifter used in this architecture.

Barrel shifter takes parallel data input and give shifted output either in left or right direction by a specific shift amount. When shift by input is "000" it will place input data at the output without shifting.

Table 1: Device Summary of Barrel Shifter

Number of slice LUTs	24 out of 218800
Number used as logic	24 out of 218800
Minimum input required time	0.571 nsec
Maximum output required time	1.327 nsec

For specifying shifting direction shift_lt_rt pin is used. When it is '0' the block will perform left shift operation and when it is '1', it will perform right operation.

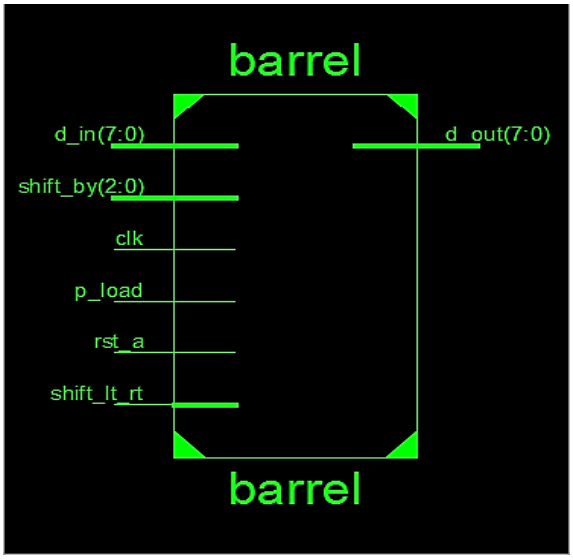


Figure 2: RTL view of barrel Shifter

D. Vedic Multiplier using Barrel Shifter

The base selection module and the power index determinant form integral part of multiplier architecture. The architecture computes the mathematical expression in equation1.Barrel shifter used in this architecture.

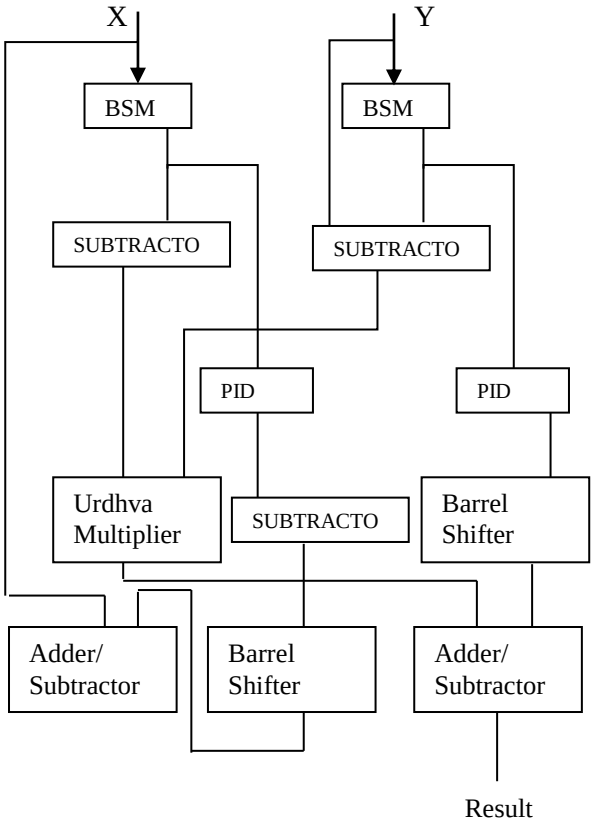


Figure 3: Urdhva Multiplier using Barrel Shifter

The two input numbers are fed to the base selection module from which the base is obtained. The outputs of base selection module (BSM) and the input numbers 'X' and 'Y' are fed to the subtractors. The subtractor blocks are required to extract the residual parts z1 and z2. The inputs to the power index determinant are from base selection module of respective input numbers.

III. RESULTS AND DISCUSSION

SIMULATION RESULT

Comparison between conventional multipliers and proposed design is been projected below. Around 68% of reduction in delay can be observed from the proposed design with respect to array multiplier in Table I. whereas the conventional Vedic multiplier contributes to 54% of reduction in delay with respect to array multiplier. The analysis provides much in depth coverage between conventional multipliers and modified Vedic multiplier architecture.

Table 1: Device Summary

Structure	Number of Slice LUTs	MCPD (maximum combinational path delay)
Array Multiplier	879	43.42
Vedic Multiplier	749	27.00
Base paper	521	16.753
Proposed multiplier	408	8.547

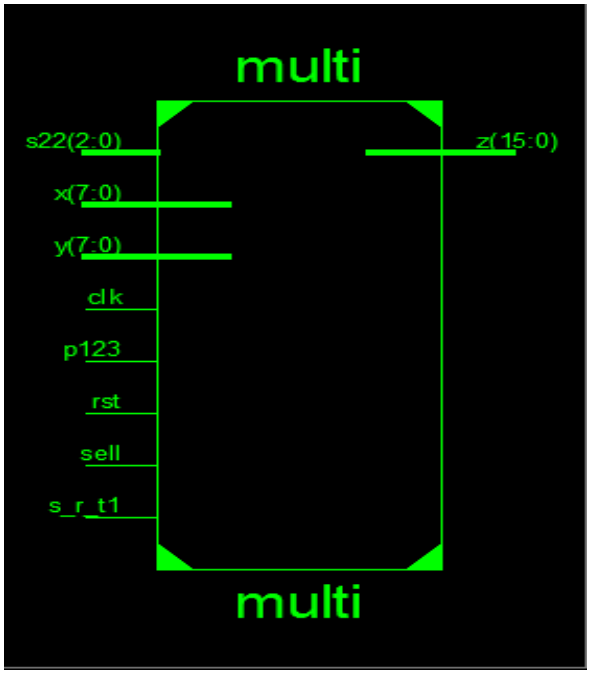


Figure 4: RTL View of Urdhwa Multiplier using Barrel Shifter

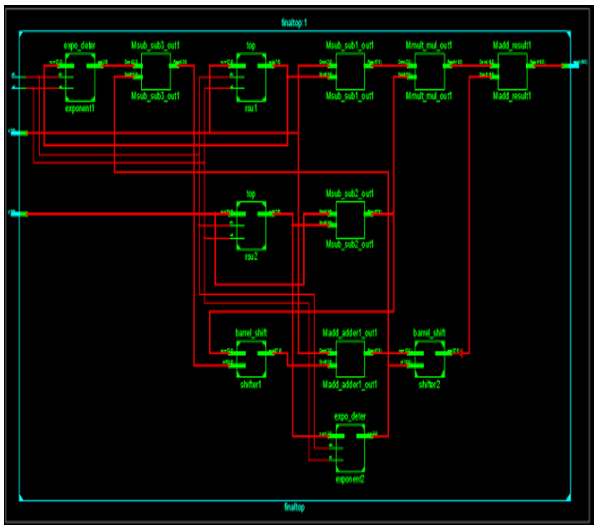
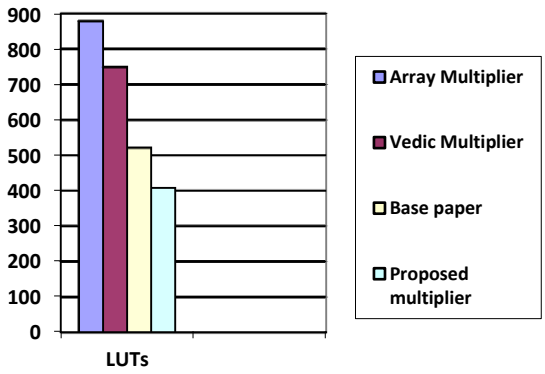
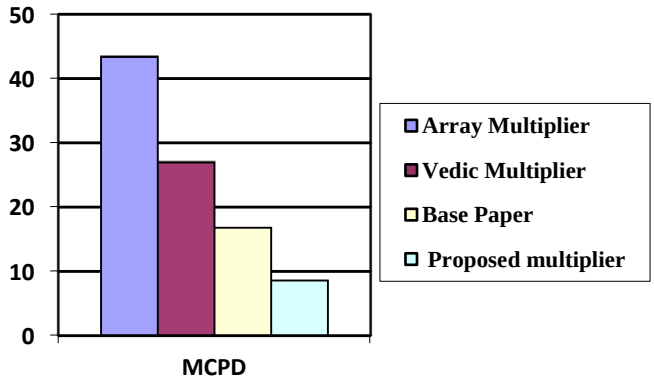


Figure 5: RTL schematic of multiplier





IV. CONCLUSION

In our design, efforts have been made to reduce the propagation delay and achieved an improvement in the reduction of delay with 54% when compared to array multiplier, booth multiplier and conventional Vedic multiplier implementation on FPGA. The high speed implementation of such a multiplier has wide range of applications in image processing, arithmetic logic unit and VLSI

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AUTHOR'S PROFILE

Mr. **Vikram Singh** has obtained his Bachelor of Engineering in Electronics and Communication Engineering) degree from RGPV University Bhopal (M.P.) India in 2012. He is perusing Master of Technology in VLSI from Rajiv Gandhi Technological University, Bhopal (M.P.) India.

Mr. **Yogesh Khandagre** has obtained his Bachelor of Engineering in Electronics and Communication Engineering from RGPV University Bhopal (M.P.) India, in 2006 and Master of Technology in Digital Communication from RGPV University Bhopal (M.P.) India in 2011 respectively. From 2007 to 2009 he was as lecturer in Electronic Department Oriental group Bhopal. He was an Asst. Professor in IIT Kanpur (U.P.) India. He is currently working as an Asst. Professor in Trinity Institute of Technology & Research, Bhopal (M.P.) India.

His current research Interest Include Signal Processing, Wireless Communication and OFDM.