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Low Error Compensation Fixed width RPR Multiplier Design Using in Merging of Images

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ABSTRACT

In area efficient low error compensation multiplier design is using fixed width RPR (Reduced Precision Redundancy). We propose a new method called fixed width RPR for DSP applications. This fixed width multiplier is placed in ANT architecture to meet high speed, low power consumption and area efficiency. The fixed RPR is designed with compensation circuit for minimizing the occurrence of error. The nxn bit is used as a input. The partial product term is used in RPR block for input correction vector and trivial input modification vector to worse the truncation errors. To achieve more precise error compensation. Variable correction value is used the truncation error can be compensation circuit is minimized. This circuit can be used in applications of image processing. By using this multiplier we merge the two images into compressed single image.

Keywords: Algorithmic noise tolerant (ANT), fixed-width multiplier, reduced-precision replica (RPR), voltage overscaling (VOS) and error correction block (EC)

I. INTRODUCTION

To lower the power indulgence, supply voltage scaling is broadly used as an effective low power technique. The power utilization in CMOS circuits is comparative to the square of supply voltage. The ANT architecture contains both main digital processor and error correction block. In ANT design we propose a fixed width RPR instead of full width RPR. RPR stands for reduced precision replica, if the original system computes the error, the RPR output is taken as the corrected output. To achieve more precise compensation, we construct the error compensation circuit mainly using the partial product term with largest weight in the LSB segment. By using compensation circuit we truncate the error with the help of variable correction vector. The disadvantage of the previous method is hardware complexity is high; voltage over scaling is used to reduce the error. This can be overcome by RPR method. If we use this method instead of wherever the multiplier is used in image processing with the help of MATLAB we reduce the pixels size and power consumption

II. METHODS AND MATERIAL

A. ANT Design

ANT can be mainly divided into Prediction based ANT and Reduced Precision Redundancy based ANT. Using ANT technique to recover the concert of DSP algorithms in presence of bit error rates. Therefore ANT can produce more efficient signals. ANT to balance for deprivation in the structure production due to errors from soft computations.

B. Proposed Fixed Width Multiplier

The fixed-width multipliers have been widely used in digital signal processor (DSP) design due to their lower power dissipation and less area. In order to reduce the chip area many fixed width Booth multipliers have been used. They decrease the detection accurateness because of reduced partial products. This method can reduce the truncated error by using variable compensation value. In order to overcome the disadvantages we presented a method of dividing the reduced partial products into the

foremost truncated section and the trivial shortened section.

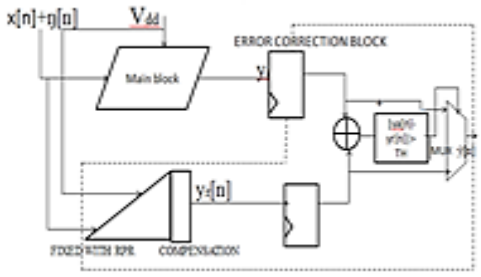


Figure 1 : proposed ANT architecture

The main block is implemented with the help of power supply VDD. The output of the main block is produced and it is denoted by ya[n]. Simultaneously the RPR block also implemented the compensation circuit correct the truncated error and produce the output. The output of this block is denoted by yr[n]. Both the outputs are taken into the decision block. The threshold value is predefined we compare the both outputs ya[n] and yr[n]. The value is less than the threshold value the multiplexer produce the output as main block ya[n].It is consider as error free output. If the value is greater than the threshold value the multiplexer produce the output as yr[n].It is consider as error truncated value. The soft error in the output is minimized.

C. Main Block

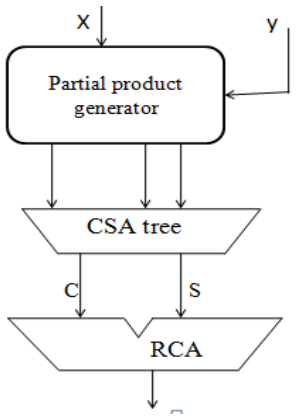


Figure 2 : Main Block diagram for proposed ANT design

In main block we are given nxn inputs to the partial product generator. The generator circuit generate the partial product terms. The output of the circuit is given to the CSA (Carry Save Adder) tree.CSA circuit group the product terms to produce two row outputs carry and sum bits. This process is iterated until all the partial product terms are grouped. Finally the output of CSA tree is given to the RCA (Ripple Carry Adder)circuit. The RCA circuit is processed based on the inputs size they finally produce the output of the main block. is operated with the help of power supply and its output is denoted by ya[n].

D. Multiplication of Images

Multiplication is the primary for all mathematical operations and finds its purpose in calculation system and graphics in digital computer and in signal processing systems. The density of fractal image weakness was analyzed. An image is selected randomly in which the image is compressed and the process is to be taken in three steps. By using MATLAB the pixel values of the image are converted into hexadecimal values is the first step. Using compressor technique in VHDL the hexadecimal values can be compressed is the second step. Finally calculate the compression ratio of the obtained image.

E. Image

Select the RGB image and then it can be converted into gray scale image. It can be represented in decimal values ranges from 0 to 255. The intensity of the each pixel is maintained by gray scale image. Fundamental unit of a computer image is pixel values and depends on resolution of an image. An image pixel has a value “0” it denotes black and value “1” or “255” it denotes white where the intensity level become weakest and strongest, respectively.

F. Flow Chart For Image Multiplication

- Generation of Partial product.
- A Carry Save Adder (CSA) is used to reduce the partial products’ by two rows.
- A final addition with Carry Propagation Adder (CPA) will result one row final value.

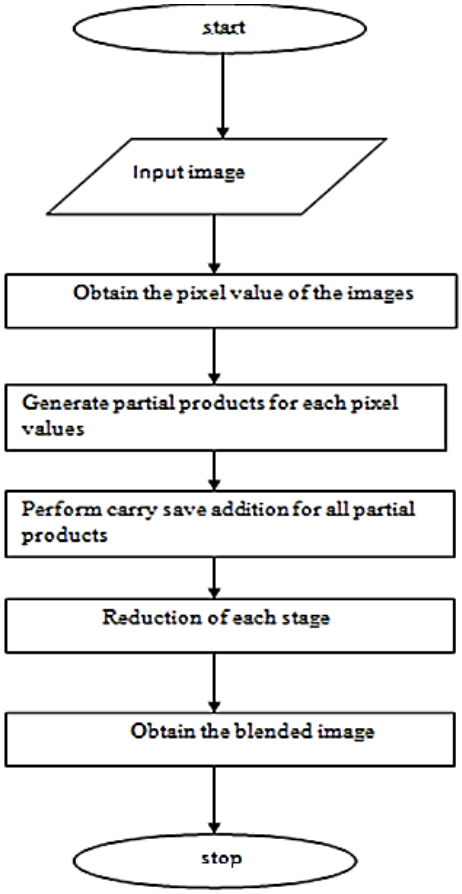
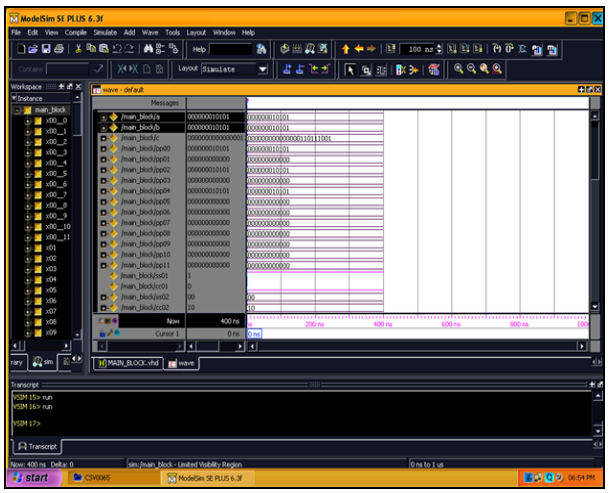


Figure 3 : Image Multiplication

III. RESULTS AND DISCUSSION

A. Simulation Results and Discussion

In this zone, we converse about the concert of the proposed RPR ANT structure. Finally we define whole circuit output waveforms that is simulated by using MODELSIM software



B. Output For Merging of Images

We take the first image as separated moon image and man image. The two images can be combined to get a single image. Pixel value of the images can be taken as binary values and then it can be converted into hexadecimal values in VHDL. The converted values are taken into compressor circuit there the image size is compressed to produce a combined image. Both the images are merged into single image.

First we select the image randomly. Here the image is moon and then read the pixel values of the image.

Second also select the image randomly. Here the image is man and then read the pixel values of the image.

Two images can be merged into single compressed image .Area of the compressed Image is low.

IV. CONCLUSION

In order to evaluate the performance of design, we have to compare the performance of this fixed width RPR design with previous full width RPR design. The design is synthesized by using Xilinx 8.1V.based on this modification soft digital signal processing systems that consume much less power than systems operating error-free at critical supply voltages Soft digital signal processing systems can reduce leakage power and provide robustness to errors caused by leakage currents. As a result the pixels that have high RGB model values such as of a white color or small RGB values such of black color, show a larger imprecision values than other pixels due to the estimated nature of the compressors. However, the error distance of Multiplier is improved.

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