© 2016 IJSRSET | Volume 2 | Issue 2 | Print ISSN : 2395-1990 | Online ISSN : 2394-4099
Themed Section: Engineering and Technology

An Architecture using 3D Lifting Based Scheme DWT

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ABSTRACT

This presents an architecture of the lifting based running 3D discrete wavelet transform (DWT), which is image and video compression algorithm. The proposed design and style is one of the first lifting based total 3-D DWT architectures without group of pictures restriction. The modern computing technique based upon analysis of lifting transmission flow graph minimizes the storage requirement. This structure looks forward to reduced memory referring to and related low power consumption, low latency, and high throughput compared to those of previous reported works. The proposed structure has been successfully executed on Xilinx Virtex-IV series field-programmable gate array, providing a speed of 321 MHz, which makes it well suited for realtime compression even with significant frame dimensions. Moreover, the architecture is fully worldwide beyond the present logical Daubechies filterbank (9, 7).

Keywords: Component; Wavelet Transform; On Line Arithmetic; Compression; FPGA Implementation

I. INTRODUCTION

STILL IMAGE compression technique based on 2-D discrete wavelet transform (DWT) has recently gained superiority above traditional JPEG based upon discrete cosine transform and is standardized in varieties like JPEG2000 [1]. Quite similarly, the use of their 3-D superset, i.e 3-D-DWT on video, beats the current predictive code standards, like H. 261-3, MPEG1-2, 4 by making the quality features just like better peak signal-to-noise rate (PSNR), removal of blocky artifacts in low bit rates. Furthermore, it features the added provisions of highly scalable compression, which is mostly coveted in modern communications over heterogeneous channels like the Net [2].

Successful program of 3-D-DWT has recently been reported inside the literary works in emerging fields just like medical image compression [3], hyper-spectral and space image compression [4], etc. Software-based techniques are played around with to combat the enormous computational complexity and memory space requirement associated with 3-D-DWT realization [5], [6]. Although the processor speed of modern computers soars excessive at the order of GHz, data fetching and communicating with external memories consume several T states, making the computation quite slower at the end. As the speeds of the peripherals are even now far behind the modern day processors, it causes even more problems.

Nowadays, almost all of the applications require real-time DWT engines with large processing potentiality that a fast and dedicated very-large-scale integration (VLSI) architecture shows up to be the best possible solution. Although it ensures excessive resource utilization, that as well in cost effective platforms like field programmable gate arrays (FPGA), designing such structures does offer some flexibilities like speeding up the computation by adopting even more pipelined structures and similar processing, likelihood of reduced memory space consumptions through better process scheduling or low-power and portability features.

To get over one of the most challenging problems associated with 3-D-DWT architectures--viz., the memory necessity, block based [7], [8] or perhaps scan-based architectures [9]-[11] with independent group of photographs (GOP) transform have recently been reported. Nevertheless blocking degrades the PSNR quality when the independent GOPs bring in annoying jerks in online video playback as a result of PSNR drop at transform boundaries [12]. Alternatively, some effective scan-based running transform architectures with convolution filtering have got been reported in [13], [14] staying away from these limitations. Following the development of the lifting structure [15], [16] in 1994, the computation of DWT provides experienced a sea alter. Although providing facilities just like a reduced computational complexness, in-place computation, ease in building nonlinear and inverse wavelets [16], the lifting also reduces the memory requirement. Thus, this has become a highly effective tool to the analysts for calculation of equally 2-D and 3-D-DWT in several applications.

Some lifting-based solely temporal transform approaches with infinite GOPs possess been reported in literatures [12], [17], with reduced memory requirements. Nevertheless, following their make an attempt to regularize the lifting calculation and reduce the storage area requirement thereafter, computation of a lifting step is usually carried out in two stages and performed sequentially. In effect, it increases the memory referencing and related power consumption when increasing the required control speed by two times.

Besides, those are basically temporal transform methods; and clearly, there exists a gap in the literature for the total 3-D-DWT architecture which in turn uses lifting and running change with infinite GOP in its working principle. This kind of paper fulfills the necessity herewith presenting a scan-based complete 3-D architecture having infinite GOP. Among the transform elements involved in three dimensions, the steering column and temporal directional changes are characteristically parallel in nature (for a row-wise scan).

The novelty of this paper lies in introducing an ingenious evaluation of signal flow chart (SFG), which subsequently displays a newer methodology intended for computing those seite a great seite transform elements with reduced storage overhead. Synchronous data flow and memory space arrangements in conjunction with decimated addressing schemes will be proposed later for combining this methodology in components. Thus, the designed processor chip has a minimum memory space requirement and smaller components budget with a twofold throughput and half calculating time, latency or memory space referencing compared to individuals of [12], [17]. Using a single adder in its critical course, the processor achieves a high speed, which is definitely a fruitful effect of pipelining and incorporation of flipping scheme. Inside the processor, the treatments of the signals at the boundary are done with the mirror extensions recommended in [1]. Section II summarizes the theory of flipping as best and newest modification on lifting. The proposed architecture along with the analysed SFG is usually| illustrated in Section 3. Section IV discusses the issues related to setup combined with the obtained results following mapping the design in re-configurable Xilinx FPGAs. Besides, a performance comparison with other related works is usually also furnished in this kind of section. Finally, the conventional paper is concluded in Section V.

II. METHODS AND MATERIAL

A. THEORETICAL FRAMEWORK

As the DWT intrinsically produces a pair of selection operations, an unified manifestation of the polyphase matrix is introduced the following [16]:

$$P(z) = \prod_{i=1}^{m} \begin{pmatrix} h_e(z) & g_e(z) \\ h_o(z) & g_o(z) \end{pmatrix} \qquad (1)$$

where h(z) and g(z) stand intended for the transfer functions to get the low pass and high pass filter banks, respectively, and almost all suffixes e and o in the literature meet even and odd conditions, respectively. Thus, the change is symbolized with the formula

$$\begin{pmatrix}\lambda(z) & \gamma(z)\end{pmatrix} = \begin{pmatrix}x_e(z) & z^{-1}x_o(z)\end{pmatrix} P(z) \qquad (2)$$

with $\lambda(z)$ and $\gamma(z)$ signifying the filtered lowpass and highpass parts of the input $x(z)$.

The lifting scheme [15], [16] factorizes the polyphase rendering into a cascade of upper and lower triangular in shape matrices and a running matrix which subsequently returning a collection of linear algebraic equations inside the time domain name bringing forth the likelihood of pipelined processor.

Several other features of working out with are mentioned in [16]. For instance, the basic Daubechies (9, 7) filterbank can be factorized as

$$P(z) = \begin{pmatrix}1 & \alpha(1+z^{-1})\\ 0 & 1\end{pmatrix}\begin{pmatrix}1 & 0\\ \beta(1+z) & 1\end{pmatrix} \begin{pmatrix}1 & \gamma(1+z^{-1})\\ 0 & 1\end{pmatrix}\begin{pmatrix}1 & 0\\ \delta(1+z) & 1\end{pmatrix}\begin{pmatrix}\zeta & 0\\ 0 & (1/\zeta)\end{pmatrix}. \qquad (3)$$

The related equations are given as:

$$\begin{aligned} s_i^0 &= x_{2i} && \text{(Splitting)}\\ d_i^0 &= x_{2i+1}\\ d_i^1 &= d_i^0 + \alpha \times (s_i^0 + s_{i+1}^0) && \text{(Predict P1)}\\ s_i^1 &= s_i^0 + \beta \times (d_{i-1}^1 + d_i^1) && \text{(Update U1)}\\ d_i^2 &= d_i^1 + \gamma \times (s_i^1 + s_{i+1}^1) && \text{(Predict P2)}\\ s_i^2 &= s_i^1 + \delta \times (d_{i-1}^2 + d_i^2) && \text{(Update U2)}\\ s_i &= \zeta \times s_i^2 && \text{(Scaling S1)}\\ d_i &= (1/\zeta) \times d_i^2 && \text{(Scaling S2)} \end{aligned}$$

where $\alpha = -1.586134342$, $\beta = -0.05298011854$, $\gamma = 0.8829110762$, $\delta = 0.4435068522$, and $\zeta = 1.149604398$ [16], and also $0 \le i \le -1$, L is the data length.

The essential path delay for these lifting equations is 5Tm + 8Ta, where Tm and Ta denote the multiplier and adder hold off, respectively [18]. The main reason behind this significant delay is stacking of multipliers from the advices to outputs. The main reason behind this major delay is stacking of multipliers from the advices to outputs.

To lessen the effect, the system of flipping continues to be presented in [18] which scale the hold off down to 3Tm & 4Ta. As a productive result, the processing rate increases significantly when the flipped equations are planned into hardware. Following the modification on SFG, the final equations for flipping are

$$\begin{aligned} s_i^0 &= x_{2i} && \text{(Splitting)}\\ d_i^0 &= x_{2i+1}\\ d_i^1 &= A \times d_i^0 + (s_i^0 + s_{i+1}^0) && \text{(Predict P1)}\\ s_i^1 &= B \times s_i^0 + \frac{(d_{i-1}^1 + d_i^1)}{16} && \text{(Update U1)}\\ d_i^2 &= C \times d_i^1 + \frac{(s_i^1 + s_{i+1}^1)}{2} && \text{(Predict P2)}\\ s_i^2 &= D \times s_i^1 + \frac{(d_{i-1}^2 + d_i^2)}{2} && \text{(Update U2)}\\ s_i &= K0 \times s_i^2 && \text{(Scaling S1)}\\ d_i &= K1 \times d_i^2 && \text{(Scaling S2)} \end{aligned}$$

where $A = (1/\alpha) = -0.630463$, $B = (1/16\alpha\beta) = 0.743750$, $C = (1/32\beta\gamma) = -0.668067$, $D = (1/4\gamma\delta) = 0.638443$, $K0 = (64\alpha\beta\gamma\delta) = 2.590697$ and $K1 = (32\alpha\beta\gamma/\delta) = 1.929981$ (up to six fractional digits) and also $0 \le i \le L - 1$, L is the data length [18]. To handle the truncation with the signals at boundaries, reflect extension is utilized by simply incorporating corresponding changes in to (5) at the start off and stop of framework sequences and at the individual frame boundaries because well as for the 3-D transforms. Now, through the computation of 3-D wavelets, the order of space and temporal transform elements involved can be interchanged where both the plans adapt the definition of 3-D-DWT. Nevertheless, first temporary and then spatial (t + 2-D) transform go through from certain limitations with spatial scalability or spatio-temporal decomposition structure [2] which restrict its possible future extensions. Thus, during the design with the present program, first spatial and after that temporal (2-D + t) decomposition are chosen even though in due requirement, the reverse method may be similarly mapped into hardware without any difficulty.

prAposed Architecture

Fig. 1 presents the proposed scan-based 1 level 3-D wavelet transform structures with a block level illustration of principal efficient modules. Clearly from

the figure, the proposed structure wills the spatial convert first, used by their temporal counterpart. The following two parts from this section give a detailed look at about hand-in-hand working of the different functional obstructs to know those two enhance components.

1. Spatial Transform

Scanned row-wise with dual clock, the newly arriving frames are fed to the spatial processor (SP) which transform them several dimensionally with all the help of two dedicated functional obstructsviz., the row control elements (RPE) and the column processing {factors} (CPE). As presented inside the figure, the scanned -pixels are primarily fed to RPE for row-transform. Alternatively, CPE remains idle to get the starting frame inside the video sequence right up until the first two rows will be transformed by RPE and the processed coefficient obstructs are accumulated in collection buffers of row Memory space module (RMEM). Using an overall size of 4N/2 for a specified frame size of N x N, RMEM provides enough space intended for the initial two converted rows. As the converted coefficients from the third row come out of RPE, column processing begins computation simultaneously by getting lowpass bands l0 and l1 in the memory with the added l2 group available online. During this kind of phase, the vacant random access memory (RAM) spots of l0 and l1 are assigned to l2 and h2 coefficient hindrances.

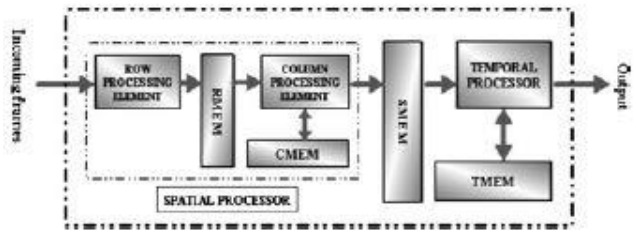


Figure 1. Proposed structure RMEM. Line buffers store row processed data CMEM, and also intermediate results of column processing SMEM. Framework buffers store spatially converted data TMEM, as very well as intermediate benefits of temporal transform to a single row

Thus, after completion of the third row, the fourth one is serially processed, during which the CPE gets busy with the high pass bands of h0, h1, and h2, by fetching all of them from the memory space. As the h0 and h1 bands are certainly not even more utilized in calculation, the individual spots are credited to the storage of l3 and h3 groups. The chronology is maintained henceforth, enabling both control factors to operate best synchronization while spatially modifying each of the support frames in sequence. During the computation, CPE requires storage space for a couple of momentary results, which is definitely provided by 6N/2 {interesting range RAMs of column Memory space module (CMEM).

Thus, the SP utilizes an total memory scale 10N/2. With the previously mentioned twice scanning, two pixels will be fed into SP when two results emerge coming from it in every time cycle, which necessitate a total of (N2/2) periods to complete the calculation of each frame. In case the frames have an even volume of rows, both the processing factors run efficiently without any interruption during the skip from {1|one particular} frame to the following. However, for the structure having a strange amount of rows, the CPE has to remain nonproductive for N/2 cycles at the beginning of each frame to obtain the first two series processed. Importantly, in the second instance too, simply no extra clock cycles happen to be spent by the SP to complete the calculation of individual frame.

2. Temporal Transform

The converted frames, to be deconstructed subsequently in the temporary domain, are primarily placed in two dual slot frame buffers of space Memory module (SMEM), while proven in Fig.1 particular. With two such primary frames already stored, and the third one getting close to the temporal processor (TP) starts computing the last convert component of 3-D-DWT. While at every routine, two pixels of earlier two frames are go through out from SMEM buffers for the computation, the respective spots are useful for the reposition of two newly arriving pixels of the current frame. Nevertheless, the calculation necessitates more; one –pixel of the third framework is usually to be read out once again from memory at one clock rate, which is often achieved throughout the utilization of the second

port from the dual-port RAMs. Thus, the temporal processing proceeds completely while the RAM spots are refreshed in an ongoing manner after passing a N2 time clock cycles, the current phase in the calculation is completed. Additionally, the SMEM buffers are entirely filled up with the pixels in the third and fourth frames. In the very next cycle, the corresponding functions of the next phase start found in a similar manner with the temporal processor finding busy with the calculation in the third, fourth, and fifth frames. The particulars of the cyclic calculation pattern for the temporary and column decompositions will be discussed in Section III-C. To incorporate periodicity inside the data flow connected with SMEM, efficient memory space arrangement and addressing technique are used. The main points are equipped in Section III-E. Just like the CPE, the temporary processor produces several momentary results during its procedure, which are called back later cycles repetitively as well as the temporal memory module (TMEM), which contains three framework buffers inside can be used like a storage space for all those results. Finally, a group of illustrated pictures can be presented in Fig. 2 which helps in understanding the series of functions involved in the control Provisions are open |to get multilevel transform with the current architecture. The most basic possible form will end up being cascading several 1 level architectures where the lll sub-band from one level is passed onto the next. Final output info set in that case needs to be synchronized or reordered in line with the need of a specific encoder. The next sections discuss the in depth design of primary functioning modules in the structures.

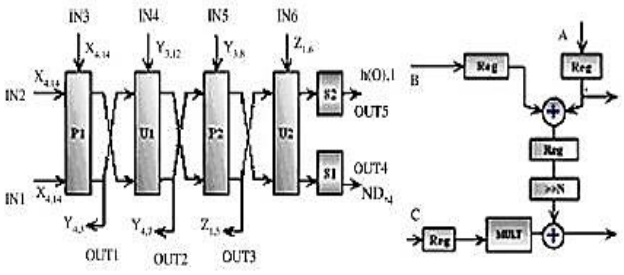


Figure 2. (a) Snapshot of CPE pipeline and (b) detailed P/U module.

A.CPE:

The architecture of CPE, displayed in Fig. 6(a), is quite identical to those of RPE. Fig. 6(b) presents its inside details which has a P/U component. However, the continuity of RPE pipe is purposefully damaged at several places creating a new set of input and output slots which contribute to the aforesaid parallel computation. Amongst all the ports, IN 1-3 and OUT 4-5 are linked to RMEM and SMEM respectively and help creating an efficient dataflow from spatial processor chip to temporal processor, because depicted in the key structure (refer to Fig. 1). The other ports, IN 4-6 and OUT 1-3 from RPE are applied to change intermediate coefficients with the 6 CMEM buffers which is the main element to slice-wise computation. Expecting to explain the computing technique mentioned in the past section, a snapshot of the CPE is shown in Fig. 2(a) to get lucidity. The snapshot is usually captured while column control of slice 3 can be ongoing to get a random framework of the incoming online video sequence. The coefficient directories beside each from the slots in the snapshot reveal the respective spots of those coefficients in the row processed frame matrix. Subsequent those indices, the snapshot can be immediately mapped on to slice several in SFG. In a similar way, the overview could be updated for the next couple of parts and so it helps to visualize the carrying out of the slice smart computing pattern by the CPE as a complete. To maintain the calculation, the aforesaid memory space need of five nodes (refer to Section III-C) may be mapped here onto five N/2 depth coefficient obstructions .However, considering the simple fact that CPE must procedure the two l and h bands after the row transform, the need is doubled to N/2 which can always be retained in the design and style of RMEM and CMEM.

B. SMEM

Once converted spatially, the frames happen to be directed to SMEM (refer to Fig. 1), which will requires a minimum of two frame buffers to get the information management. While the first two frames can easily be given room found in those two frame buffers easily, complexity arises once the third frame comes from SP and the computation is simultaneously began by the TP. When in every clock routine a pixel pair of frame 2 can come to be allocate into the empty memory spots from the place that the two pixels of the frames 0 and one particular have already been read out intended for the computation, the temporary processing methodology demands a great extra set with the examine procedure to

be taken out; for collecting the corresponding pixels of framework 2 which act because the third set Fig. 3.

Importantly, this second set of information cannot be provided online to the TP, because the frames area unit inbound at double rate and computation desires them at single clock. So, all that's needed is to browse them back from memory with a [*fr1] information rate. Thus, the memory arrangement of Fig. seven is followed where port A of the twin port RAMs is employed for reading older frames from memory still as storing the newer ones in those locations once the Port B remains dedicated for the second set of browse operations. Thus, the primary reasonably operations in impact refreshes the memory with the consecutive duos of frames 0, 1 and 2, three so on, whereas the second operations area unit solely chargeable for providing the extra pixels of frame 2i throughout computations involving slice i (i = one, 2, 3, . . .).As portrayed in shot one of Fig. 8, the frames zero and one, being divided in components L and H, wherever L and H signify the fact that those pixels emerge from the lowpass and highpass ports of CPE, at first organize themselves in buffers of SMEM.

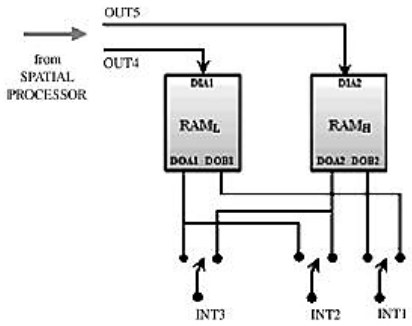


Figure 3. Arrangement of SMEM frame buffers.

Once the computation progresses, the pixels of the 2 frames are replaced with those of frame two and as a matter of fact, the new frame gets decimated within the RAMs because the pixels of the new frame area unit allotted to memory locations, just discharged off the older frames anytime. Thus, as the computation of slice two is completed, the new frames two and three reposit themselves in line with the topography delineated in snapshot two of that figure. The order of destruction will increase as the computation moves ahead following a fashion terribly similar to that of quick Fourier rework addressing. The pattern repeats itself once log2N2 cycles.Fig. nine helps U.S.A. to see the addressing pattern for a sample RAM depth of 8. The dual port BlockRAMs of Xilinx FPGA that is employed as target platform for the planned design provides the facility of "read before write" operations within the same clock cycle at the memory locations.

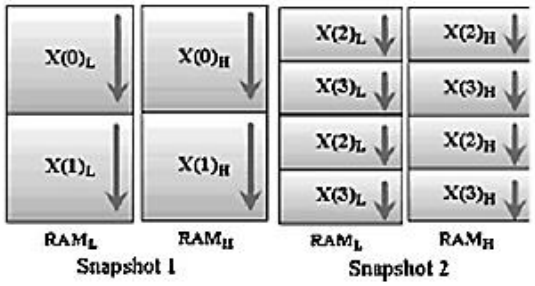


Figure 4. Two snapshots of the SMEM

Utilizing it, coinciding browse and write operations square measure performed by associate address in port A through the channels DIA and DOA, per the wants. The address in port B follows identical observe, only dynamical at a [*fr1] speed, as they at the same time decide up 2 pixels from the RAM pairs during a clock cycle that are more multiplexed to feed INT two of TP at singleclockrate.

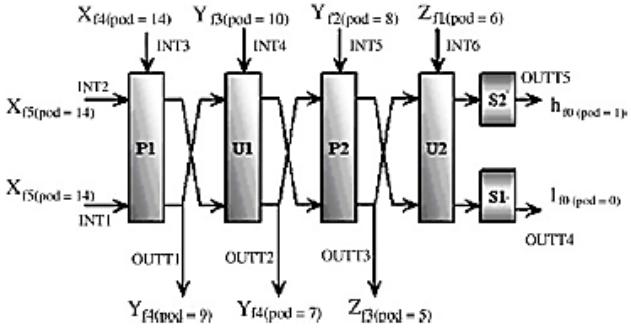


Figure 5. Snapshot of the TP.

D.TPandTMEM

The design of Temporal Processor is a twin of that of CPE as each follow the slice-wise computation strategy described in Section III-C. Fig. ten clarifies identical with a snapshot of pipelined TP unit. The notation Xfi (p×l = j) adopted within the snap symbolizes the constant X in SFG admire the jth component in frame i. Thus, comparison of these frame indices with the SFG reveals the activity of TP in computing the slice three nodes at the snapshot instant. Thepipelined-TP design attributes to the distinction of component numbers across the ports. While the inputs INT 1-3 square measure received from SMEM, the TMEM buffers that act as a storage place for temporary

results exchange these intermediate coefficients with the CPE through ports INT 4-6 and OUT 1-3. The pattern for addressing those frame buffers is easy because the serial-addressing theme will handle the information transferproperly.

G. Arrangement to Avoid Latency in Inter-Frame TransitionfortheSP

At the start of computation by SP, that is largely a 2-D-DWT processor, the beginning of CPE gets delayed by 2 rows than RPE. However, massive worth of accumulative delays for ordered frames is to be avoided because it affects the web computation. Within the gift design, this delay is avoided by a processor programming arrangement. For the purpose of illustration, a frame depth of five has been taken. In the planned processor programming, the CPE should sit idle at the row one of all the frames ranging from frame one (F1), to collect enough information for column process. However, the RPE runs swish, as shown in processor programming, indicating no delay between the frames. this is often specific to frames containing odd range of rows solely. For frames having an excellent row count, each the CPE and RPE run swimmingly over the transition. In that case, the sliced SFG are often extended over to ensuing frame, and also the CPE computes in slices while not interruption. Thus, for every of the cases, inter-frame latency is eliminated.

H. LATENCY AND COMPLETE MEMORY DEMAND

Following the SFG of lifting (refer to Fig. 5), the minimum number of inputs needed for computing a wave constant is restricted to 5. Thus, with the supply of the fifth input to arrive on-line throughout the computation, the CPE and TP, respectively, want a minimum wait time of 4 rows (2N clock cycles) and 4 frames (2N2 cycles) to supply the vital path for the processor consists of single adder, making it quite quick. a quick counter based mostly controller was designed that handles all the address generation and different switching operations at the high speed of main data-path.

Such controllers square measure programmable and might synchronize the management signal generation in line with totally different video frame sizes. So other than customary N × N, they'll handle customary quarter common intermediate format or common intermediate format or numerous totally different side ratios. The adders from the library and device twin port block RAMs are utilised because the principal resources for the designed processor. Simulation is performed by ModelSim XE III 6.0a, that yields a collection of finish results utterly matching the results from MATLAB seven.0.0, wherever a model of the hardware is made.

The overall design report can be formulated as

Custom frame size 256×256
Group of frames (GOP) Infinite
Maximum clock frequency 321 MHz
Throughput Two results/cycle
Initial latency $2N2 + 2N\psi + 47$ clock cycles
Number of occupied slices 1776 (2%)
Total number four input
LUTs 2188 (1%)
Number of block RAMs 350 (63%).

III. RESULTS AND DISCUSSION

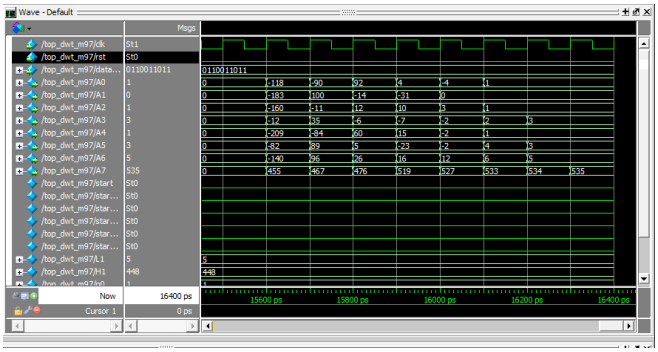
PERFORMANCE ANALYSIS

Among the few dedicated architectures for 3-D-DWT reportable in literature till date, the inherent issues associated with the styles following block based mostly approaches [7], [8], or having finite GOPs [9]–[11] square measure already mentioned. Amidst the running rework strategies, [14] was quite roaring being convolution based mostly, whereas [12], [17], tho' promisingly formulated upon lifting, limit their discussions within the temporal processing methodology alone. solely this style is one of the primary lifting based mostly complete 3-D-DWT architectures which fancy no restriction on GOP. it's price mentioning that though [9], [10], having finite GOPs, don't represent ideal temporal rework.

The memory demand of the bestowed design is found. Demand is a smaller amount for frame sizes right down to the order of 800 pixels. Even so, design in necessitates 4N2off-chip reminiscences with higher read-write latency. Memoryconsumption is low . However, it implements a lower length D-4 filter bank. The styles referred in [12], [17] have an equivalent temporal buffer demand because the planned one. all the

same, in both the cases, dynamic change of buffers knowledge is completed with the arrival of every frame .The planned methodology succeeds in doing the transform by doing the computations once when the arrival of every 2 frames solely. the next enhancements square measure a halved latency and procedure time throughout process and a doubled turnout. Moreover, whereas operating with an equivalent frame rate, the speed burden of the planned processor and memory referencing become common.

These along, for such computation intensive process such as 3-D-DWT, impact the facility consumptions to an excellent extent. Thus, the results indicate the wide prospects of the planned design in applications requiring low power consumptions like medical imaging. Also, the computing time is near seventy fifth of that needed for big GOPs too. Largely attributable to the very fact that the vital path delay corresponds to one adder, the utmost operational speed of the design reaches 321 MHz that makes it quickest among all. At customary rates of thirty FPS with a frame size of 256×256, any DWT processor with a turnout of two needs a minimum one.09 MHz for period one level process. Thus, at 321 MHz, this style offers quite massive computing potentials. As the spacial processor module is essentially a 2-D-DWT engine, comparison of this half is distributed with 3 different standard 2-D-DWT architectures on the market within the literatures and bestowed in Table II. It shows that this style has very cheap memory demand among all and latency is lower than that of [20]. Moreover, the planned design is much quicker than the remainder. The device resource consumption of the present style is additionally less.



IV. CONCLUSION

The proposed payment system combines the Iris recognition with the visual cryptography by which customer data privacy can be obtained and prevents theft through phishing attack [8]. This method provides best for legitimate user identification. This method can also be implemented in computers using external iris recognition devices.

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