AMBA-APB RTL Implementation using Efficient Power and Constructs through Verilog

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ABSTRACT

The challenge in engineering VLSI based IC design to find an optimum solution for chip which will satisfy the needs of Power, area and efficiency. The aim of this paper is to design and AMBA-APB RTL which is highly efficient in power and size issues. The reusability of design and easy configurability are the focus area of this paper through which design will be implemented. The Design specification is based on ARM based AMBA_APB specification version V2.0. For the simulation task, ModelSim Version 10.3 has been used. For the synthesisation purpose, design utilization summary and power details Xilinx-ISE design software has been used. Power report is introduced for developing better and clear understanding of the power utilization and distribution in any system. The power report gives the power consumption summary.The total clocks power consumption in chip is of 0.38mW, total hierarchy power consumption of 0.52 mW and total on chip logical power consumption of 0.111 W have been extracted from Xilinx XPower analyser tool when APB Bridge is designed under the proposed design approach.
Keywords: RTL Constructs, Xilinx ISE 14.1, Efficient Power, Modelsim, SoC

I. INTRODUCTION

While designing a block or an Intellectual Property (IP) of SoC, specific set of recommendations should be planned. As architectures of SoC have been shifted to advanced design approaches, more complexities get introduced into the design considerations and power consumption gets introduced into picture. So, the guidelines should be planned in such a way that it provides less integration efforts and helps to the designers for designing a successful SoC with a well-structured and synthesizable RTL code with efficient in energy and optimized in power consumption.AMBA. which is known as advanced microcontroller bus architecture is a well-known name in system on chip design considerations in VLSI domain. Modern portable mobile devices like Smartphone, hard disk and various ASIC products cannot even imagine without AMBA buses (advanced microcontroller bus architectures). Simple AMBA Architecture plan is as following:

This block diagram represents the various blocks in on-chip protocol. It shows the connectivity between different submodules and various bridges,their connectivity.
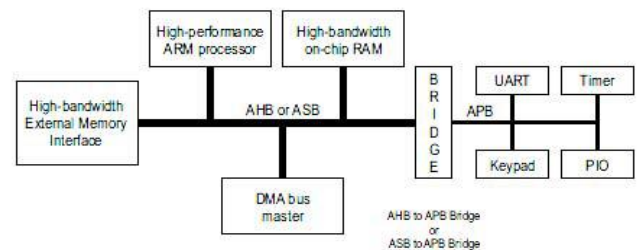

Figure 1: AMBA Architecture plan
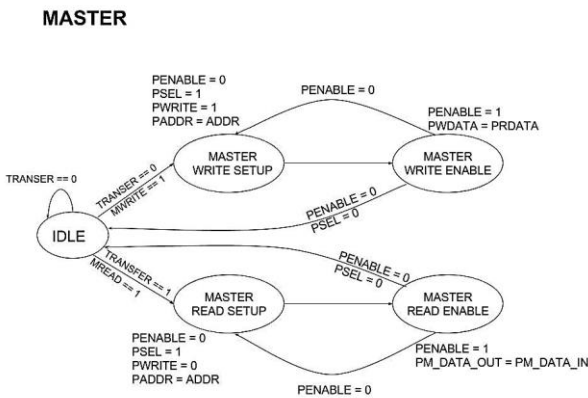
II. METHODS AND MATERIAL

System Model And Assumptions

A. Transition Minimization through efficient State Model

We start with identifying clock signals and their transition details. We examined the each and every clock precisely and tried to find interrelation between them. The unused clock transitions have been identified and then the state diagram has been designed as per module. We focussed on designing state diagram for all units like master slave and arbiter. We designed signals as per the standard datasheet and then tried to find the interrelated

relations. we started writing specifications as per the desired protocol. We started with special constructs like parameterised constructs which provide flexibility in designing and reuse.
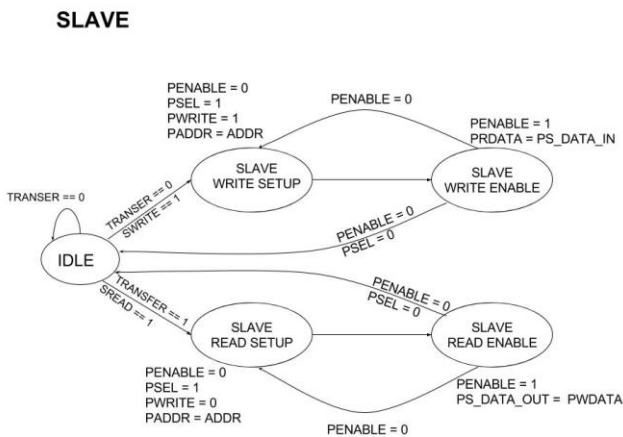

Figure 2: State Diagram for Master

I have defined the decoder master slave multiplexer section separately and a hierarchal pattern has been formed for designing a top module. I designed a memory for simulating the read and write operations and applying the results with the desired protocol. The simulation has been done and the clock variation and timing calculation has been calculated.

Figure 2 : State Diagram for Slave

B. Design of APB Bridge

Advanced Peripheral Bus (APB) Bridge is an essential part in AMBA shown in Figure 1. It performs some operations like address, data and control signal latching for connected peripherals. APB Bridge behaves as single master for the APB bus. APB Bridge performs two important operations: read and write transfers. Control signal gives the necessary information whether a read or write transfer is required for the desired operation. It is used to decode the 5 bit input into corresponding 32 bits of code and responsible for generating a signal to select a particular slave. Here we used 5X32 decoder for decoding coming address for the slave select. The synthesis of proposed and resulted design is synthesised with Xilinx Synthesis tool. It is designed with Tcl scripts which run precision RTL synthesis. The RTL views consist of various parts like Master, Slave, Flip-flops and other basic modules as per design.

III. RESULTS AND DISCUSSION

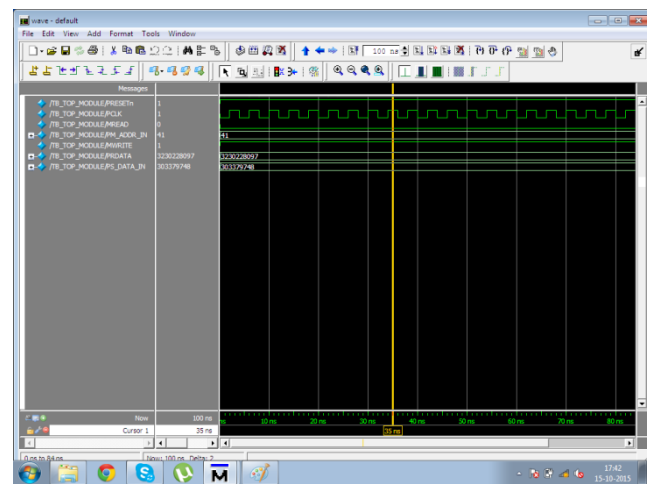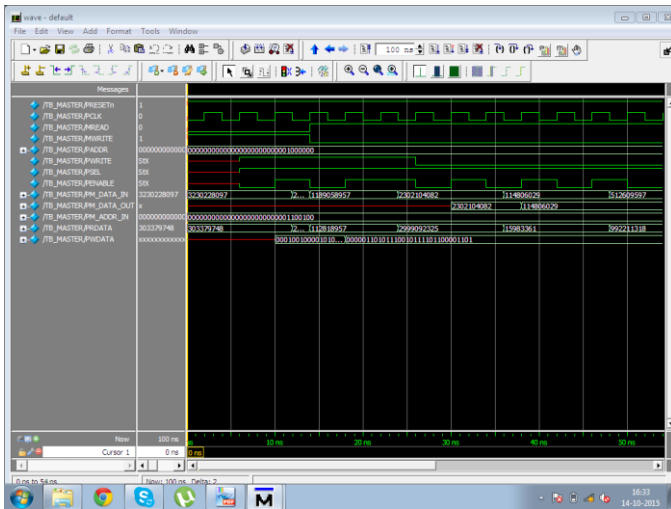### Simulation Results and Discussions

The proposed design and techniques has been coded in simple Gvim editor and then simulate using Modelsim as well as Xilinx ISE tool. The steps has been explained in the above chapter. In this chapter present the result on the GUI. I show the results of various sub modules on the simulation window. I separately show the read and write operations Graphical user interface approach
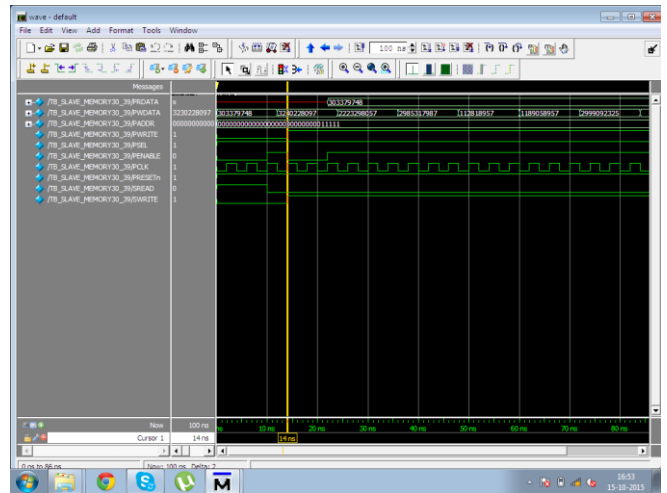

Figure 4: Top Module simulation result.

Various reports like Design summary, synthesis report and other power report has been generated in this section.

**Figure 5:** Master-Slave Read and write transfer

Figure 6 : Synthesis Report of Design

Hence proposed design is used to minimize the clock skew and also provides the less power consumption. We use various FPGA families to simulate the results and then a comparison chart of various results has been listed.

Figure 7: Decoder Simulation results

This result shows the decoder simulation. It is used to decode the 5 bit input into corresponding 32 bits of code and responsible for generating a signal to select a particular slave. Here we used 5X32 decoder for decoding coming address for the slave select.Final synthesised RTL view is given below.
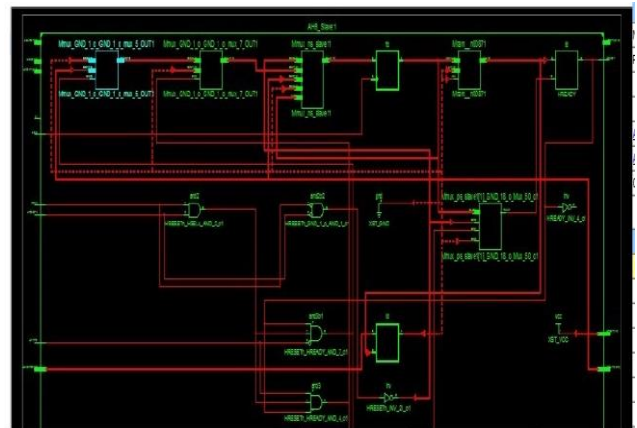
IV. CONCLUSION

I have worked on concept of using parameterized modelling technique which can be useful in reuse the design, implementing small modules in big designs. This work is mainly focus on creating a pre-power assumption of desired chip so we can optimise the required power before the actual backend design. In Previous works many works has been done towards this approach but my work is different mainly in the sense of using language constructs and reducing power requirements by using clock skews. I have simulated this protocol by use of memory and shows the master slave read write operation by simulation tool. I synthesize the

design and produced the RTL view of the design to show the exact structure of implemented Design.

Frequency(MHz)	Previous design results(Power Report in W)	Current Design Results(Power Report in W)
50	Total Clock Domain = 0.00039	Total Clock Domain = 0.00037
50	Total Hierarchy Power =0.00057	Total Hierarchy Power =0.00054
50	Total On-chip power = 0.113	Total On-chip power = 0.110

V. REFERENCES

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