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Constant Delay Logic Based Timing Analysis of Adder Circuits Using C5 Process Technology

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ABSTRACT

A full custom logic design for adders and their timing analysis followed by FFT plots is proposed in this paper targeting high speed applications using MOSIS C5 process for CMOS. The characteristic of this logic style regardless of the logic type makes it suitable for implementing complicated arithmetic and logic circuits preferably adders and multipliers. A carry-look ahead adder (CLA) or fast adder is a type of adder used in digital logic and is presented for design and analysis. A carry-look ahead adder improves speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower, ripple carry adder for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bits. The carry-look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits. Carry Propagator and Carry Generator FFT results are compared in terms of their amplitude, phase and group delays. Several design considerations including timing window width adjustment and output distribution namely sum are discussed. Sum outputs are tabulated for multibit adders namely 4 bits and 16 bits. Their timing analysis is done using suitable SPICE code and C5 process technology.

Keywords : CMOS, Adders, VLSI Design, CAD, process technology, delay analysis

I. INTRODUCTION

In this paper, a full adder designemploying both complementary metal–oxide–semiconductor (CMOS) logic and transmission gate logic is reported. The designwas reviewed firstly implemented for 1 bit and then extended for 32 bit also.The circuit was implemented using many professional VLSI CAD such as Cadence Virtuoso tools in 180-and 90-nm technology. Performance parameters such as power,delay, and layout area were compared with the existing designssuch as complementary pass-transistor logic, transmission gateadder, transmission function adder, hybrid pass-logic with staticCMOS output drive full adder, and so on. For low power voltage supply at process technology below 180-nm technology, the average power consumption few µWless than fewer µWwas found to be extremely low with moderately low delay less than generally of the order of ps resulting from the deliberate incorporation of very weak CMOS inverters coupled with strong transmission gates. Correspondingvalues of the same were of the order of the deepsubmicron and µW .The design wasfurther extended for implementing 32-bit full adder also, and wasfound to be working efficiently with only variable and constant delay logic styles and power tabulated at 180-nm and 90-nm and MOSIS C5 models for scalable CMOS transistors below the mentioned technologyfor 1.8-V or 1.2-V supply voltage. In comparison with the existingfull adder designs, the present implementations were found to offersignificant improvement in terms of power and speed and overall performance as well.

With the advent of Very Large Scale Integration (VLSI) and ULSI (Ultra Large Scale Integration) after that, rapid advances took place in circuit integration technologies; the electronics industry has achieved a phenomenal growth overthe last two decades. Various applications of VLSI CMOS circuits in high-performance computing, telecommunications, and consumer electronics has been expanding progressively,

and at avery hasty pace.Steady advances in semi-conductor technology and in the integration levelof Integrated circuits (ICs) have enhanced many features, increased theperformance,improved reliability of electronic equipment, and at the same time reduce the cost, powerconsumption and the system size.With the increase in the size and the complexity of the analog and digital systems, Computer Aided Design (CAD) tools are introduced into the hardwaredesign process.Design Methodologies are necessary for a systematic design. [1,8]The chip design process enforced the automation of process, automation of simulation based verification i.e. replacing of traditional breadboard techniques through HDL (hardware description language) development. The various modular hierarchical techniques of design created the scenario that CAD tools are inevitable.

II. METHODS AND MATERIAL

1. VLSI Technology and Design

A VLSI System integrates millions and millions of electronic components in a small area. The main objective is to make the analog or digital system as compact as possible with the required functionalities. Tens and thousands of transistors are fabricated on a small piece of wafer. The circuits are tested and fabricated becauseonce an error is created the whole design is waste and it costs million andmillions of dollars. Therefore CAD tools came into the picture. CAD tools are inevitable.[9] This chip design forced automation of process, automation of simulation based verification. This CAD assistance has lead to Electronic Design Automation which may be further classified in to frontend and backend design.

2. Design Methods

Systematic design methods or the design methodologies are necessary for successfully designing complex digital hardware.

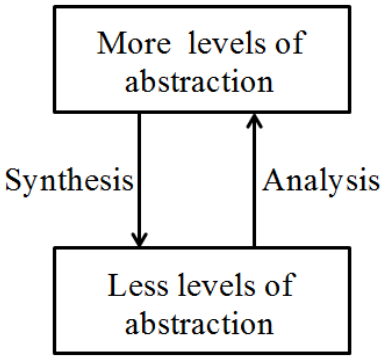

Figure 1. Abstraction Hierarchy for VLSI Adders 1

Our design methods usually differ by the number of abstraction levels and the complexities involved.

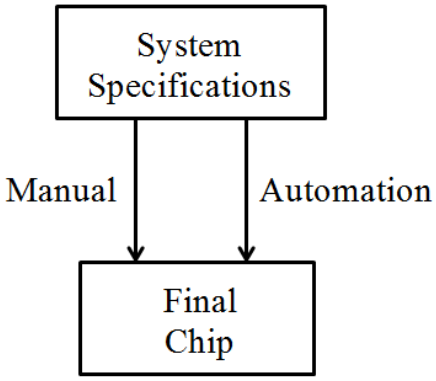

Figure 2. Abstraction Hierarchy of VLSI Adders 2

Comparing structurally different views of a VLSI Design include divide and conquer techniques which includes sorting by structure and sorting by issues. The design hierarchy that uses existing techniques has an unacceptable restriction that they use identical hierarchies. Structurally hierarchy transformation is the first step and hierarchy base comparison is the last step.

A. Structured Design Techniques
B. Programmable Logic Design
C. Gate Array and Sea of Gates Design
D. Cell Based Design
E. Full Custom and Semi-custom Design
F. Platform based Design and SOC

3. Adder Design Methodology

Digital design is an amazing and very broad field. The applications of digital design are present in our daily life, including Computers, calculators, video cameras etc. In fact, there will be always need for high speed and low

power digital products which makes digital design a future growing business. Adders are critical component of a microprocessor and are the core component of central processing unit. Furthermore, it is the heart of the instruction execution portion of every computer. Adders comprise the combinational logic that implements logic operations, such as AND and OR, and arithmetic operations, such as ADD and SUBTRACT.

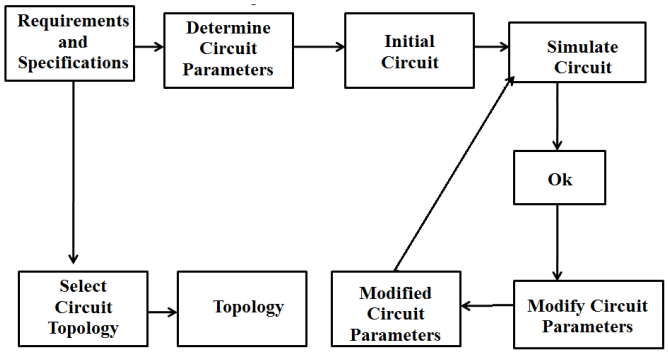

Figure 3. Presented Methodology and Planning for Adder Circuit design

Methodology and Planning of Work:
The design methodology can be clear from following

1. Defining the requirements and setting the specifications.
2. Design according to the Tool flow (EDA based).
3. Design of the Test circuits.
4. Simulating the Test results and optimization of the parameters

The design methodology can be summarized as

1. Choosing the basic structure of the Adders.
2. Selection of the computational model using appropriate process technology.
3. Measurement and Optimization of Design parameters
4. Physical model implementationof the design.

III. RESULTS AND DISCUSSION

4. Simulation Results and Experimental Data

A regrious effort has been to implement the presented design. The presented design isa full custom integrated circuit design with all design rules and network consistency Checks verified. The project aims to design the combinational circuits and simulatethe designed circuits. The designed schematic views and icon views along with thesimulation results are shown one by one along with one final integrated design. AnNCC (Network consistency check) report is attached for the complete design.

There are numerous topologies and designs exist in literature. This paper presents a full custom design of multi bit adders and simulation results are as shown

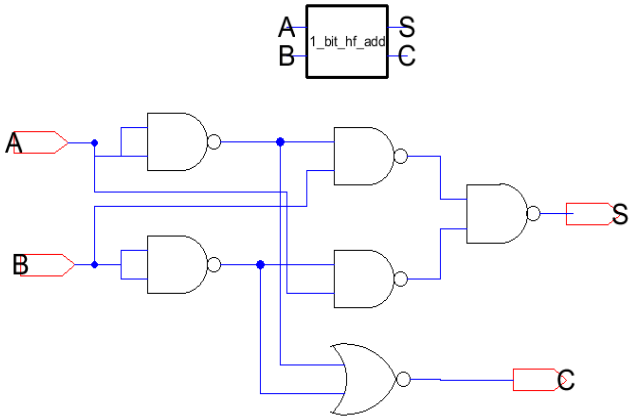

Figure 4.1. Schematic and icon view of1 bit half adder

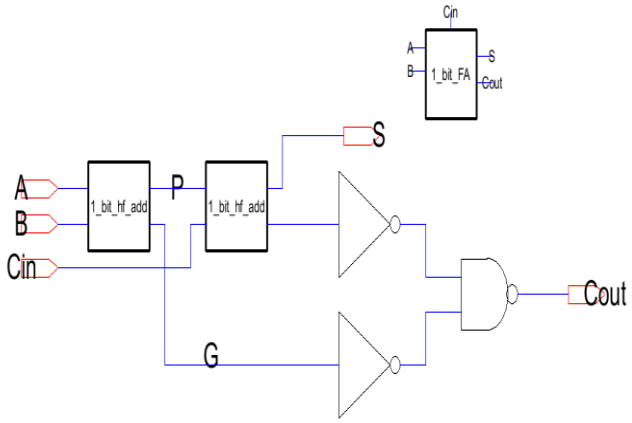

Figure 4.2. Schematic and icon view of 1 bit Full adder

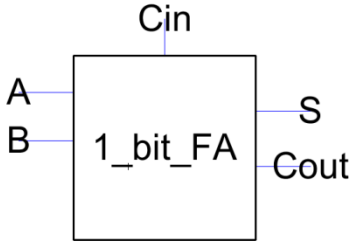

Figure 4.3. icon view of 1 bit Full adder with signals marked

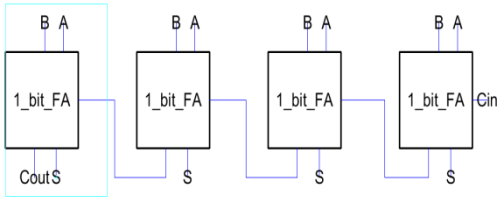

Figure 4.4. Front end view for 4 bit Full Adder

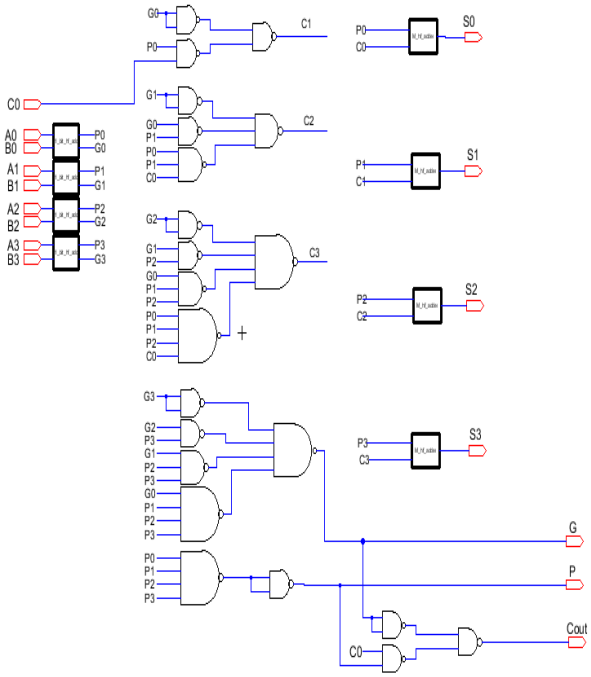

Figure 4.5. Schematic design for 4 bit Carry lookahead adder

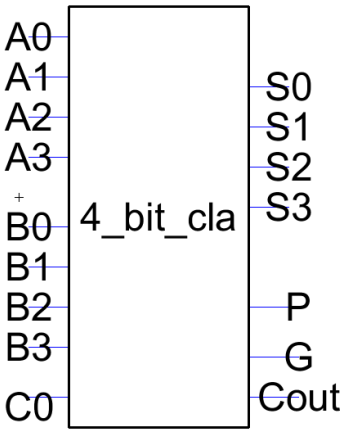

Figure 4.6. Icon for design for 4 bit Carrylookahead adder with inputs $A_{0.3}$ and $B_{0.3}$ and Sum outputs Propagate, Generate and Carry out with sum $S_{0.3}$

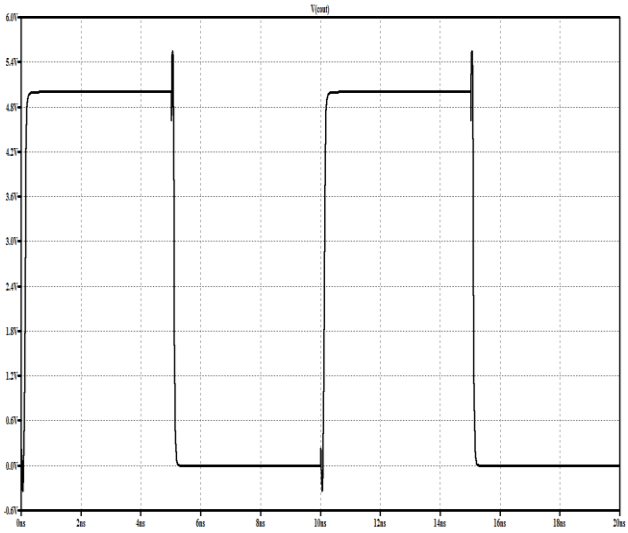

Figure 4.7. Transient Analysis plot for Cout for 4 bit CLA

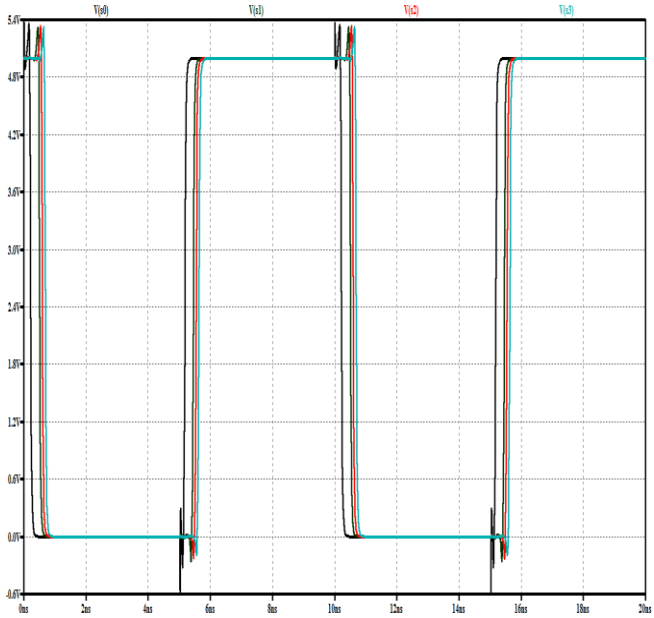

Figure 4.8. Transient plot for Sum signals in 4 bit CLA

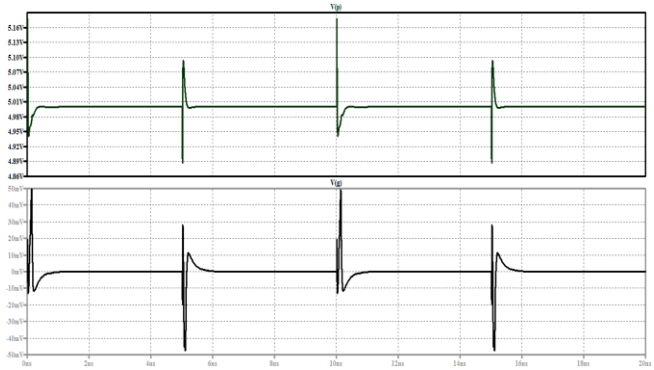

Figure 4.9. Transient plot for propagate and generate signals in 4 bit CLA Adder

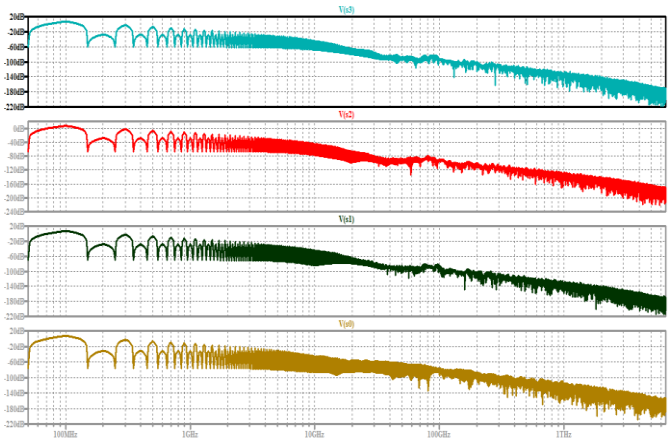

Figure 4.10. FFT plots for sum signals in 4 bit CLA

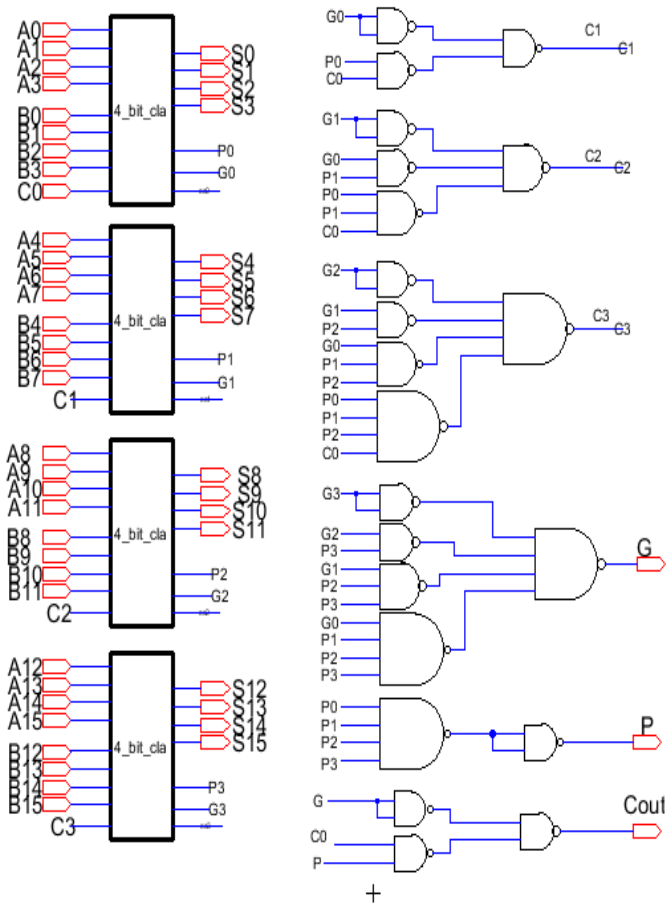

Figure 4.11. Schematic design for 16 bit Carrylookahead adder

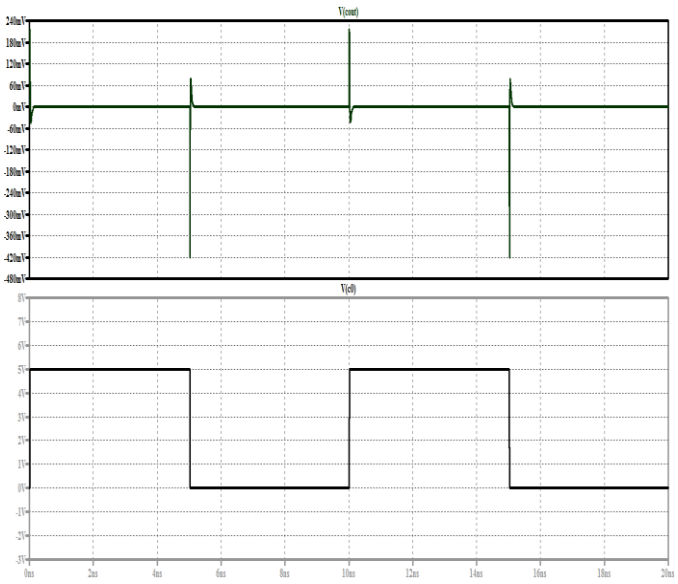

Figure 4.12. Transient analysis plot for Carryout

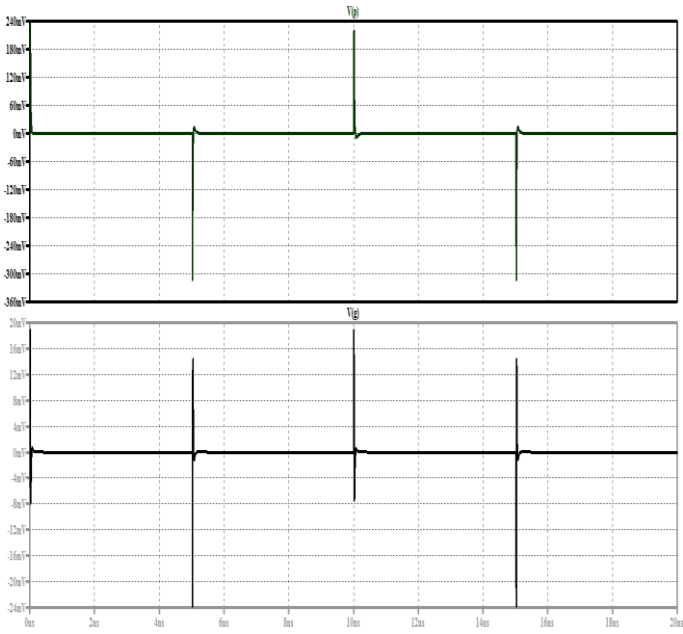

Figure 4.13. Transient analysis plot for propagate and generate signals in 16 bit CLA

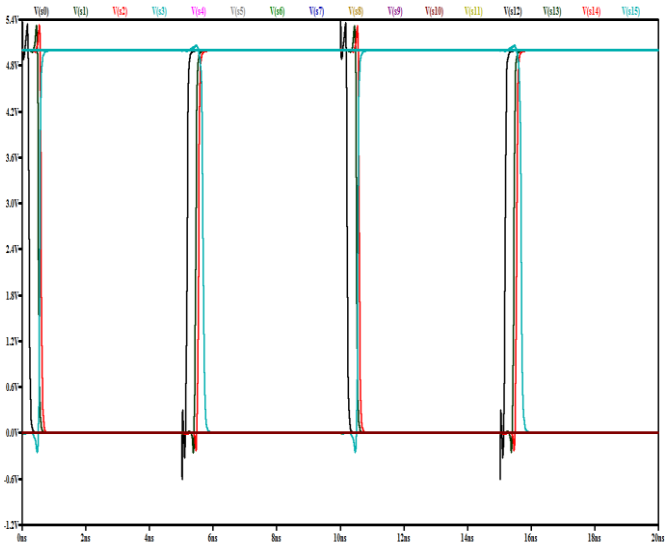

Figure 4.16. Transient plot for Sum signals in 4 bit CLA

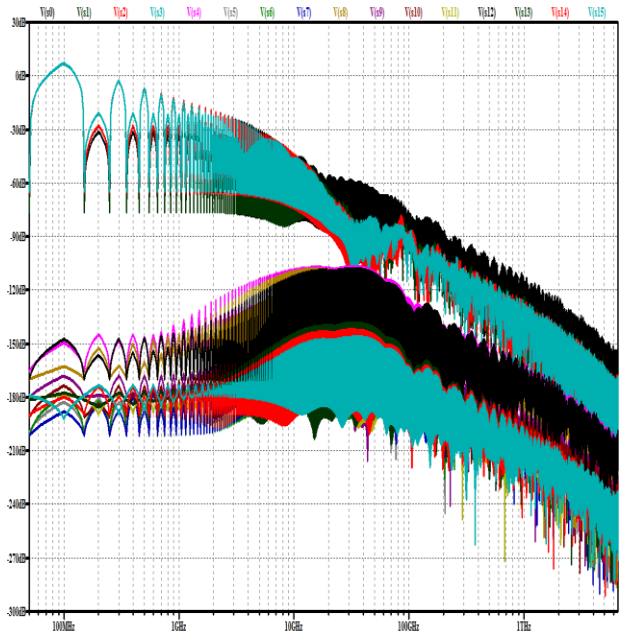

Figure 4.17. FFT plots or Noise index plot for Sum Signals in 16 bit CLA design

5. FFT plots comparison between 4 bit CLA and 16 bit CLA

The performance analysis of adders 4 bits and 16 bits in terms of their FFT profile is shown in above section and tabulation and comparison of FFT and transient parameters is illustrated here and drawn in table- 1, shows different,. thus, there exist tradeoffbetween these parameters. the results are helpful in selectionof an adder according to desired result and application.

Table 1
FFT Index Results for 4 bit CLA (Sum Signals)

FFT plot parameters for signal S_0			
S.No.	**Frequency**	**Magnitude**	**Delay**
1.	10MHz	94.59 dB	213.17 ps
	100 MHz	6.27 dB	49.76 ns
	1 GHz	94.46 dB	1.01 ns
	10 GHZ	100.16 dB	203.09 ps
	100 GHz	111.9 dB	179.90 ps
FFT plot parameters for signal S_1			
2.	**Frequency**	**Magnitude**	**Delay**
	10MHz	91.13 dB	522.8 ps
	100 MHz	6.27 dB	7.82 ns
	1 GHz	91.24 dB	486.96 ps
	10 GHZ	102.49 dB	551.8 ps
	100 GHz	115.57 dB	567.45 ps
FFT plot parameters for signal S_2			
3.	**Frequency**	**Magnitude**	**Delay**
	10MHz	86.51 dB	603.75 ps
	100 MHz	6.277 dB	49.30 ns
	1 GHz	86.59 dB	2.85 ns
	10 GHZ	96.32 dB	570.08 ps
	100 GHz	12.43 dB	116.10 ps
FFT plot parameters for signal S_3			
4.	**Frequency**	**Magnitude**	**Delay**
	10MHz	81.8 dB	698.35 ps
	100 MHz	6.277 dB	49.20 ns
	1 GHz	81.88 dB	3.04 ns
	10 GHZ	88.53 dB	677.06 ps
	100 GHz	109.98 dB	808.22 ps

Table 2
FFT Index Results for 16 bit CLA (Sum Signals)

FFT plot parameters for signal S_0			
S.No.	**Frequency**	**Magnitude**	**Delay**
1.	100MHz	6.99 dB	4.78 ns
	1THz	127.32 dB	2.5 ns
FFT plot parameters for signal S_1			
2.	**Frequency**	**Magnitude**	**Delay**
	100MHz	6.96 dB	4.46 ns
	1THz	131.55dB	457.57 ps
FFT plot parameters for signal S_2			
3.	**Frequency**	**Magnitude**	**Delay**
	100MHz	6.99 dB	4.39 ns
	1THz	131.36 dB	2.7 ns
FFT plot parameters for signal S_3			
4.	**Frequency**	**Magnitude**	**Delay**
	100MHz	7.02 dB	575.40ps
	1THz	138.157 dB	1.05 ns
FFT plot parameters for signal S_4			
	Frequency	**Magnitude**	**Delay**
5.	100MHz	149.10	149.89 ps
	1THz	166.049 dB	1.89 ns
FFT plot parameters for signal S_5			
6.	**Frequency**	**Magnitude**	**Delay**

	100MHz	186.98 dB	101.89 ps
	1THz	199.19 dB	386.01 ps
FFT plot parameters for signal S_6			
7.	**Frequency**	**Magnitude**	**Delay**
	100MHz	179.27 dB	5.05 ns
	1THz	202.24 dB	3.26 ns
FFT plot parameters for signal S_7			
8.	**Frequency**	**Magnitude**	**Delay**
	100MHz	188.17 dB	5.04 ns
	1THz	208.60 dB	153.78 ps
FFT plot parameters for signal S_8			
	Frequency	**Magnitude**	**Delay**
9.	100MHz	162.83 dB	66.49 ps
	1THz	175.61 dB	3.88 ns
FFT plot parameters for signal S_9			
10.	**Frequency**	**Magnitude**	**Delay**
	100MHz	168.09 dB	5.09 ns
	1THz	196.16 dB	2.77 ns
FFT plot parameters for signal S_{10}			
11.	**Frequency**	**Magnitude**	**Delay**
	100MHz	174.05 dB	4.53 ns
	1THz	199.97 dB	3.99 ns
FFT plot parameters for signal S_{11}			
12.	**Frequency**	**Magnitude**	**Delay**
	100MHz	100.07 dB	58.34 ps
	1THz	204.57 dB	186.18 ps
FFT plot parameters for signal S_{12}			
	Frequency	**Magnitude**	**Delay**
13.	100MHz	147.51 dB	5.081 ns
	1THz	176.16 dB	3.17 ns
FFT plot parameters for signal S_{13}			
14.	**Frequency**	**Magnitude**	**Delay**
	100MHz	177.68 dB	56.266 ps
	1THz	206.44 dB	3.08 ns
FFT plot parameters for signal S_{14}			
15.	**Frequency**	**Magnitude**	**Delay**
	100MHz	179.96 dB	5.09 ns
	1THz	211.35 dB	2.73 ns
FFT plot parameters for signal S_{15}			
16.	**Frequency**	**Magnitude**	**Delay**
	100MHz	192.05 dB	75.21 ps
	1THz	217.46 dB	1.01 ns

IV. CONCLUSION

With design technology, it would be possible to implement, verify and test the complex integrated circuits like adders which is the basic unit of all arithmetic circuits... This paper explains design quality metrics from aAdder design perspective, simulation and analysis of the same namely in terms of its FFT profile. Average delay for a 4 bit CLA is 30.02 ns and average delay for 16 bit CLA is 2.468 ns at 100 MHz frequency. The logic style helps to improve the overall design and delay changes by 91.77% in a 16 bit CLA over 4 bit CLA design. Various shortcomings of the current designsand methodologies to tackle the VLSI design challenges were discussed and several promising remedies and their implications on design and methodologies are explored using c5 process technology.

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