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Cascaded Two-Level Inverter-Based Multi-Level Inverter for High Power Applications by Using Statcom with Fuzzy Logic Control

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ABSTRACT

This paper presents a simple STATCOM scheme using a cascaded two-level inverter-based multilevel inverter. The proposed topologies have two VSI based two-level inverters are connected in cascade through open-end windings of a three-phase transformer and filter elements. Converter fed dc-link voltages are regulates at different levels to obtain four-level operation. The proposed STATCOM multilevel inverter has operates under MATLAB/SIMULINK environment and the results are verified in balanced and unbalanced conditions. Further, stability behavior of the topology is investigated. The system behaviors are analyzing under various operating conditions using fuzzy logic control.

Keywords : DC-link voltage balance, multilevel inverter, power quality (PQ), static compensator (STATCOM).

I. INTRODUCTION

The application of flexible ac transmission systems(FACTS) controllers, such as static compensator(STATCOM) and static synchronous series compensator(SSSC) is increasing in power systems. This is due to theirability to stabilize the transmission systems and to improve power quality (PQ) in distribution systems. STATCOM is popularly accepted as a reliable reactive power controller replacing conventional var compensators, such as the thyristor-switchedcapacitor (TSC) and thyristor-controlled reactor (TCR). This device provides reactive power compensation, active power oscillation damping, flicker attenuation, voltage regulation, etc.[1].

Generally, in high-power applications, var compensation is achieved using multilevel inverters [2]. These inverters consist of a large number of dc sources which are usually realized by capacitors. Hence, the converters draw a small amount of activepower to maintain dc voltage of capacitors and to compensate the losses in the converter. However, due to mismatch in conduction and switching losses of the switching devices, the capacitors voltages are unbalanced. Balancing these voltages is a major research challenge in multilevel inverters. Various control schemes using different topologies are reported in [3]–[7].

Among the three conventional multilevel inverter topologies.cascade H-bridge is the most popular for static var compensation [5], [6]. However, the aforementioned topology requires a large number of dc capacitors. The control of individual dc-link voltage of the capacitors is difficult. Static var compensation by cascading conventional multilevel/two level inverters is an attractive solution for high-power applications. The topology consists of standard multilevel/two level inverters connected in cascade through open-end windings of a three-phase transformer. Such topologies are popular in high-power drives [8]. One of the advantages of this topologyis that by maintaining asymmetric voltages at the dc links of the inverters, the number of levels in the output voltage waveform can be increased. This improves PQ [8]. Therefore, overall control is simple compared to conventional multilevel inverters.Various var compensation schemes based on this topology are reported in [10]–[12]. In [10], a three-level inverter and two level inverter are connected on either side of the transformer low-voltage winding. The dc-link voltages are maintained by separate converters. In [11], three-level operation is obtained by using standard two-level inverters. The dc-link voltage balance between the inverters is affected by the reactive power supplied to the grid.

In this paper, a static var compensation scheme is proposed for a cascaded two-level inverter-based

multilevel inverter. The topology uses standard two-level inverters to achieve multilevel operation. The dc-link voltages of the inverters are regulated at asymmetrical levels to obtain four-level operation. To verify the efficiency of the proposed control strategy, the simulation study is carried out for balanced and unbalanced supply-voltage conditions.

II. METHODS AND MATERIAL

1. Cascaded Two-Level Inverter-Basedmultilevel Statcom

Fig.1 shows the power system model considered in this paper [13]. Fig. 2 shows the circuit topology of the cascaded two-level inverter-based multilevel STATCOM using standard two-level inverters. The inverters are connected on the low-voltage (LV) side of the transformer and the high-voltage (HV) side is connected to the grid. The dc-link voltages of the inverters are maintained constant and modulation indices are controlled to achievethe required objective. The proposed control scheme is derived from the ac side of the equivalent circuit which is shown in Fig. 3. In the figure V_a', V_b' and V_c' are the source voltages referred to LV side of the transformer r_a,r_b and r_c are the resistances which represent the losses in the transformer and two inverters, La, L_b and Lc are leakage inductances of transformer windings, and e_{a1},e_{b1},e_{c1} and e_{a2},e_{b2},e_{c2} are the output voltages of inverters 1 and 2, respectively r_1,$r_2$are the leakage resistances of dc-link capacitors c_1 and c_2, respectively. Assuming r_a=r_b=r_c=r, L_a=L_b=L_c=L and applying KVL on the ac side, the dynamic model can be derived using [14] as

$$\begin{bmatrix} \frac{di_a'}{dt} \\ \frac{di_b'}{dt} \\ \frac{di_c'}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r}{L} & 0 & 0 \\ 0 & \frac{-r}{L} & 0 \\ 0 & 0 & \frac{-r}{L} \end{bmatrix} \begin{bmatrix} i_a' \\ i_b' \\ i_c' \end{bmatrix} + \frac{1}{L} \begin{bmatrix} v_a' - (e_{a1} - e_{a2}) \\ v_b' - (e_{b1} - e_{b2}) \\ v_c' - (e_{c1} - e_{c2}) \end{bmatrix} \quad ....(1)$$

Equation (1) represents the mathematical model of the cascaded two-level inverter-based multilevel STATCOM in the stationary reference frame. This model is transformed to the synchronously rotating reference frame [14]. The d-q axes reference voltage components of the converter e_d* and e_q* are controlled as

$$e_d^* = -x_1 + \omega L i_q' + v_d' \qquad (2)$$

$$e_q^* = -x_2 - \omega L i_d' + v_q' \qquad (3)$$

where v_d^1 is the d-axis voltage component of the ac source and i_d^1,i_q^1 are d-q axes current components of the cascaded inverter, respectively. The synchronously rotating frame is aligned with source voltage vector so that the q-component of the source voltage v_q^1 is made zero. The control parameters x_1 and x_2 are controlled as follows:

$$x_1 = (k_{p1} + \frac{k_{i1}}{s})(i_d^* - i_d') \qquad (4)$$

$$x_2 = (k_{p2} + \frac{k_{i2}}{s})(i_q^* - i_q') \qquad (5)$$

The d-axis reference current is obtained as

$$i_d^* = (k_{p3} + \frac{k_{i3}}{s})[(v_{dc1}^* + v_{dc2}^*) - (v_{dc1} + v_{dc2}) \qquad (6)$$

Where v_{dc1}^*, v_{dc2}^* and v_{dc1}, v_{dc2} are the reference and actual dc-link voltages of inverters 1 and 2, respectively. The q-axis reference current i_q^* is obtained either from an outer voltage regulation loop when the converter is used in transmission-line voltage support or from the load in case of load compensation.

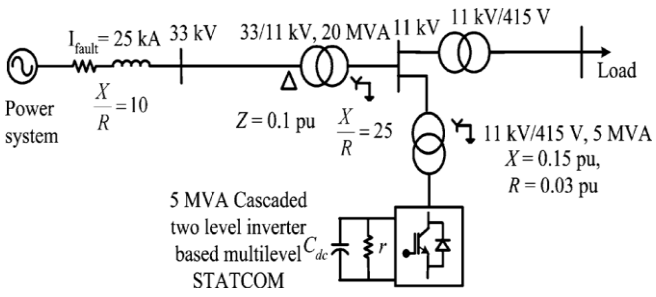

Figure 1. Power system and the STATCOM model.

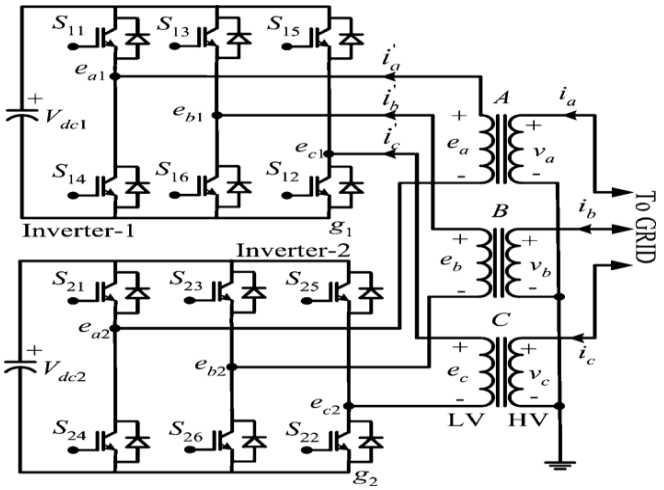

Figure 2. Cascaded two-level inverter-based multilevel STATCOM

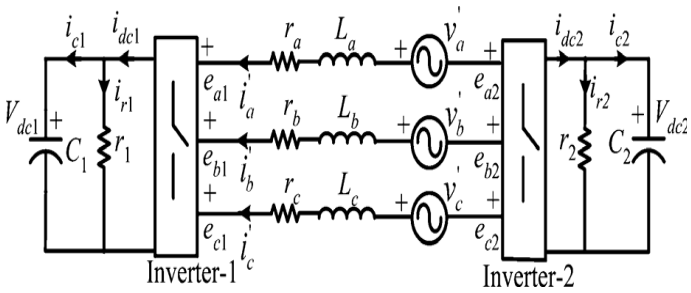

Figure 3. Equivalent circuit of the cascaded two-level inverter-based multilevel STATCOM.

2. Control Strategy

The control block diagram is shown in Fig.5. The unit signals $\cos(\omega t)$ and $\sin(\omega t)$ are generated from the phase-locked loop (PLL) using three-phase supply voltages (V_a,V_b,V_c) [14]. The converter currents (i'_a,i'_b,i'_c) are transformed to the synchronous rotating reference frame using the unit signals. The switching frequency ripple in the converter current components is eliminated using a low-pass filter (LPF). From (v^*_{dc1}+v^*_{dc2}) and i_q^* loops, the controller generates d-q axes reference voltages, e^*_d and e^*_q for the cascaded inverter. With these reference voltages, the inverter supplies the desired reactive current (i_q^*) and draws required active current (i_d^*) to regulate total dc-link voltage $v^*_{dc1}+v^*_{dc2}$. However, this will not ensure that individual dc-link voltages are controlled at their respective reference values. Hence, additional control is required to regulate individual dc-link voltages of the inverters.

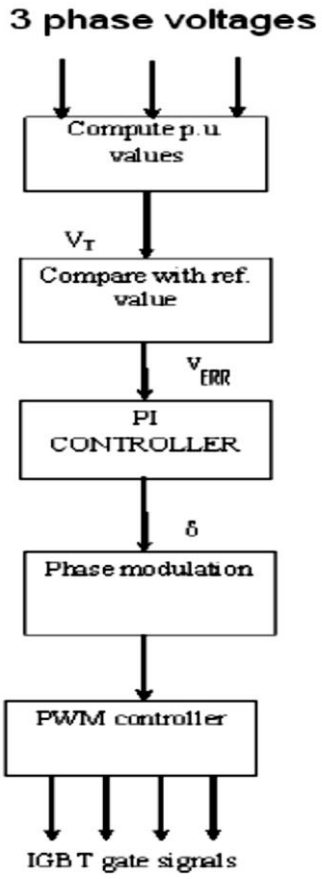

Figure 4. Control algorithm of STATCOM with PI controller

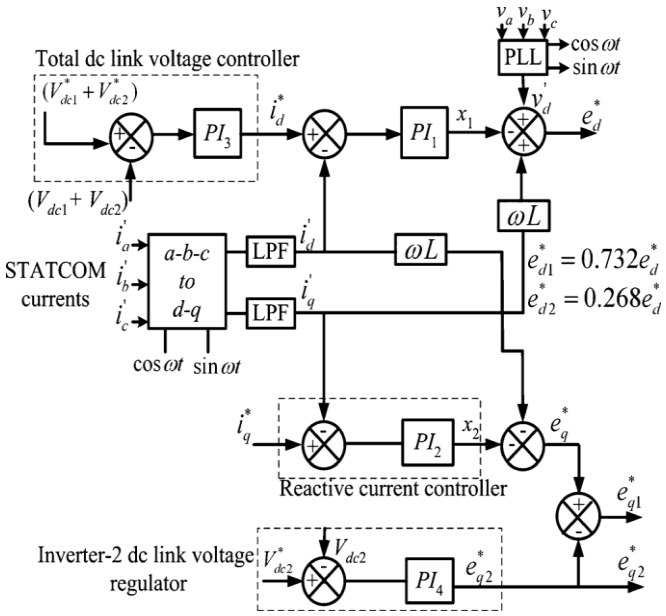

Figure 5. Control Block Diagram

3. DC-Link Balance Controller

The resulting voltage of the cascaded converter can be given as e_i at an angle δ where $e_i = \sqrt{e_d^2 + e_q^2}$,

$\delta = \tan^{-1}\left(\frac{e_q}{e_d}\right)$.The active power transfer between the source and inverter depends on δ and is usually small in the inverters supplying var to the grid [1]. Hence, δ can be assumed to be proportional to e_q. Therefore, the q-axis reference voltage component of inverter-2 e^*_{q2} is derived to control the dc-link voltage of inverter-2 as

$$e^*_{q2} = (k_{p4} + \frac{k_{i4}}{s})(v^*_{dc1} - v^*_{dc2}) \quad (7)$$

The q-axis reference voltage component of inverter-1 e^*_{q1} is obtained as

$$e^*_{q1} = e^*_q - e^*_{q2} \quad (8)$$

The dc-link voltage of inverter-2 V_{dc2} is controlled at 0.366 times the dc-link voltage of inverter-1 V_{dc1} [9]. It results in four-level operation in the output voltage and improves the harmonic spectrum. Expressing dc-link voltages of inverter-1 and inverter-2 in terms of total dc-link voltage, V_{dc} as

$$V_{dc2} = 0.268V_{dc} \quad (9)$$

$$V_{dc1} = 0.732V_{dc} \quad (10)$$

Since the dc-link voltages of the two inverters are regulated, the reference d-axis voltage component e^*_d is divided in between the two inverters in proportion to their respective dc-link voltage as

$$e^*_{d1} = 0.732e^*_d \quad (11)$$

$$e^*_{d2} = 0.268e^*_d \quad (12)$$

For a given power, if $V_{dc2} < V^*_{dc2}$, $\delta_2 = \tan^{-1}\left(\frac{e^*_{q2}}{e^*_{d2}}\right)$ increases and $\delta_1 = \tan^{-1}\left(\frac{e^*_{q1}}{e^*_{d1}}\right)$ decreases. Therefore, power transfer to inverter-2 increases, while it decreases for inverter-1. The power transfer to inverter-2 is directly controlled, while for inverter-1, it is controlled indirectly. Therefore, during disturbances, the dc-link voltage of inverter-2 is restored to its reference quickly compared to that of inverter-1. Using e^*_{d1} and e^*_{q1}, the reference voltages are generated in stationary reference frame for inverter-1 and using e^*_{d2} and e^*_{q2} for inverter-2. The reference voltages generated for inverter-2 are in phase opposition to that of inverter-1. From the reference voltages, gate signals are generated using the sinusoidal pulse-width modulation (PWM) technique [15]. Since the two inverters' reference voltages are in phase opposition, the predominant harmonic appears at double the switching frequency.

4. Unbalanced Conditions

Network voltages are unbalanced due to asymmetric faults or unbalanced loads [16]. As a result, negative-sequence voltage appears in the supply voltage. This causes a double supply frequency component in the dc-link voltage of the inverter. This double frequency component injects the third harmonic component in the ac side [17]. Moreover, due to negative-sequence voltage, large negative-sequence current flows through the inverter which may cause the STATCOM to trip [16]. Therefore, during unbalance, the inverter voltages are controlled in sucha way that either negative-sequence current flowing into the inverter is eliminated or reduces the unbalance in the grid voltage. In the latter case, STATCOM needs to supply large currents since the interfacing impedance is small. This may lead to tripping of the converter. The negative-sequence reference voltage components of the inverter e^*_{dn} and e^*_{qn} are controlled similar to positive-sequence components in the negative synchronous rotating frame as

$$e^*_{dn} = -x_3 + (-\omega L)i'_{qn} + v'_{dn} \quad (13)$$

$$e^*_{qn} = -x_3 - (-\omega L)i'_{dn} + v'_{qn} \quad (14)$$

Where v'_{dn},v'_{qn} are d-q axes negative-sequence voltage components of the supply and i'_{dn} ,i'_{qn} are d-q axes negative-sequence current components of the inverter, respectively. The control parameters x_3 and x_4 are controlled as follows:

$$x_3 = (k_{p5} + \frac{k_{i5}}{s})(i^*_{dn} - i'_{dn}) \quad (15)$$

$$x_4 = (k_{p6} + \frac{k_{i6}}{s})(i^*_{qn} - i'_{qn}) \quad (16)$$

The reference values for negative-sequence current components i^*_{dn} and i^*_{qn} are set at zero to block

negative-sequence current from flowing through the inverter.

5. Stability Analysis

Considering the dc side of the two inverters in Fig.3, the complete dynamics of the system are derived in the Appendix. The transfer function is as follows:

$$\frac{\Delta V_{dc1}(s)}{\Delta \delta_1(s)} = \frac{num_1(s)}{den(s)} \tag{17}$$

$$\frac{\Delta V_{dc2}(s)}{\Delta \delta_2(s)} = \frac{num_1(s)}{den(s)} \tag{18}$$

Hence, the poles of transfer function always lie on the left half of the s-plane. However, numerators of the transfer functions are functions of the operating conditions. The positions of zeros primarily dependent. The sign of these variables changes according to the mode of operation. Therefore, zeros of the transfer functions shift to the right half of the s-plane for certain operating conditions. This system is said to be non-minimum phase and there is a limit on achievable dynamic response[19]. The system may exhibit oscillatory instability when there is a step change in reference for high controller gains. Therefore, the controller gains should be designed suitably to avoid the instability. This behavior is similar to that of the two-level inverter-based STATCOM.

When STATCOM is in inductive mode of operation. The reactive component is set at 0.75 p.u. and proportional gain is varied from 0 to 10. It can be seen that all poles lie on the left half of the s-plane for this case as well. However, one zero shift to the right half and three zeros lie on the left half of the s-plane. Moreover, it can be seen that closed-loop poles of the system shift to the right half of the s-plane for high controller gains.

III. RESULTS AND DISCUSSION

The system configuration shown in Fig.1 is considered for simulation. The simulation study is carried out using MATLAB/SIMULINK. The system parameters are given in Table I.

Table I : Simulation System Parameters

Rated power	5 MVA
Transformer voltage rating	11kV/400
AC supply frequency, f	50 Hz
Inverter-1 dc link voltage, V_{dc1}	659 V
Inverter-2 dc link voltage, V_{dc2}	241 V
Transformer leakage reactance, X_l	15%
Transformer resistance, R	3%
DC link capacitances, C_1, C_2	50 mF
Switching frequency	1200 Hz

1. Simulation diagram for Reactive power control:

In this case, reactive power is directly injected into the grid by setting the reference reactive current component i_q* at a particular value. Initially, i_q* is set at 0.5 p.u. At t=2.0 s, i_q* is changed to 0.5 p.u. Fig.7 shows the source voltage and converter current of the A phase. Fig.8 shows the dc-link voltages of two inverters. From the figure, it can be seen that the dc-link voltages of the inverters are regulated at their respective reference values when the STATCOM model is changed from capacitive to inductive. Moreover, the dc-link voltage of inverter 2 attains its reference value faster compared to that of inverter 1

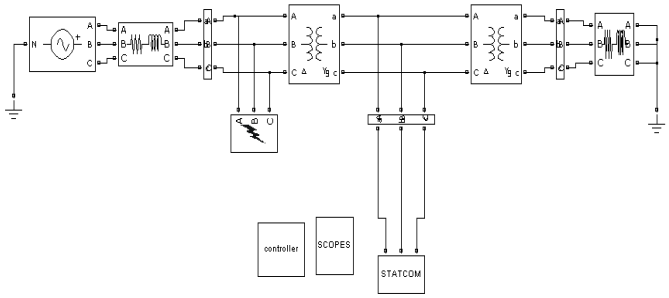

Figure 6. Simulation diagram for Reactive power control

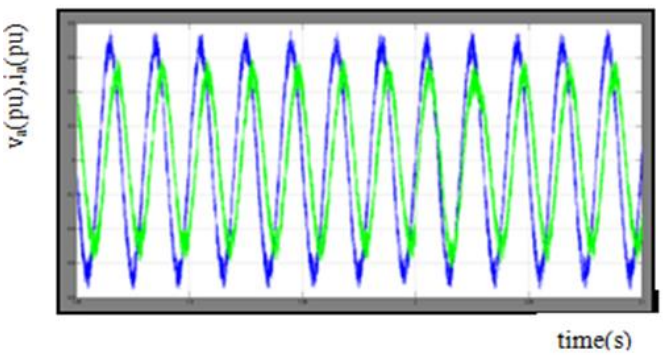

Figure 7. Source voltage and current

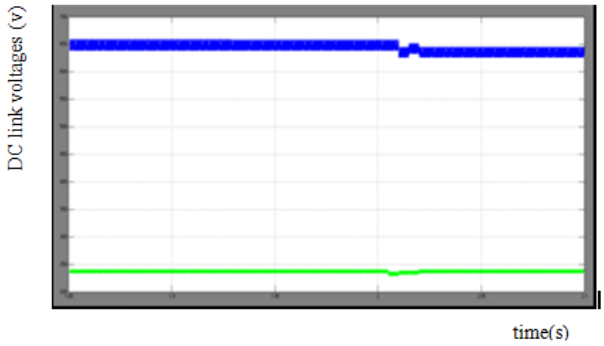

Figure 8. DC-Link Voltage

2. Simulation diagram of Load Compensation

In this case, the STATCOM compensates the reactive power of the load. Initially, STATCOM is supplying a current of 0.5p.u. At t = 2.0 s, the load current is increased so that STATCOM supplies its rated current of 1p.u. Fig.10 shows source voltage and converter current, while Fig.11 shows the dc-link voltages of two inverters. The dc-link voltages are maintained at their respective reference values when the operating conditions are changed.

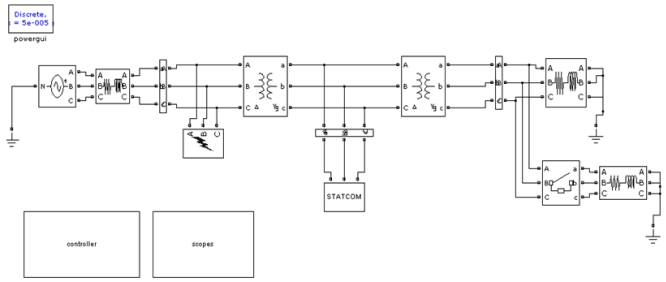

Figure 9. Simulation diagram of LOAD COMPENSATION

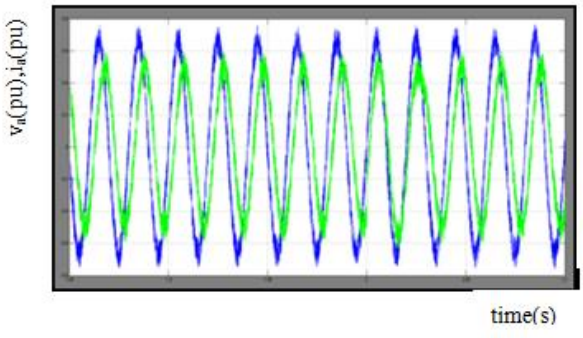

Figure 10. Source Voltage and Current

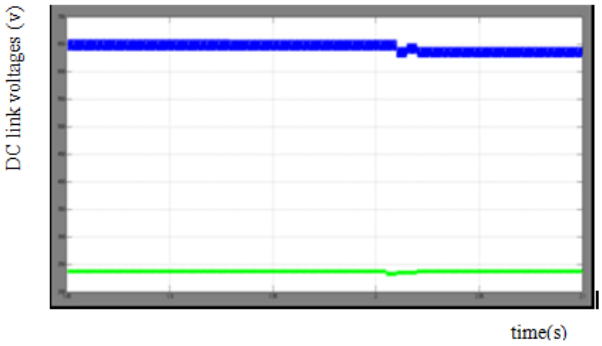

Figure 11. DC Link Voltages

3. Simulation diagram for Operation During Fault

In this case, a single-phase-to-ground fault is created at t=0.2s, on the phase of the HV side of the 33/11-kVtransformer. The fault is cleared after 200ms. Fig. 13 shows voltages across the LV side of the 33/11-kV transformer. Fig.14 shows the - axes components of negative-sequence current of the converter. These currents are regulated at zero during the fault condition.

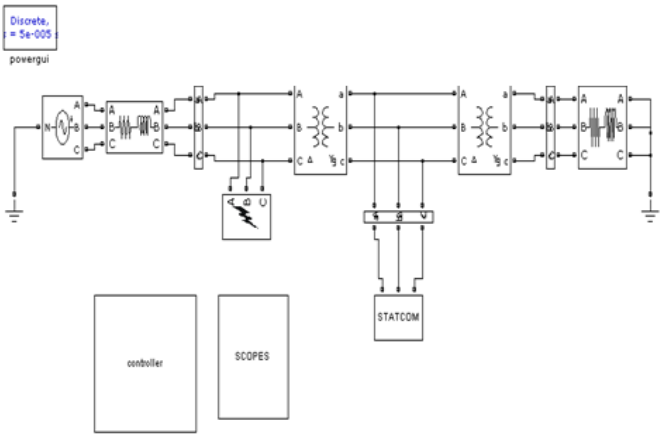

Figure 12. Simulation diagram for Operation During Fault

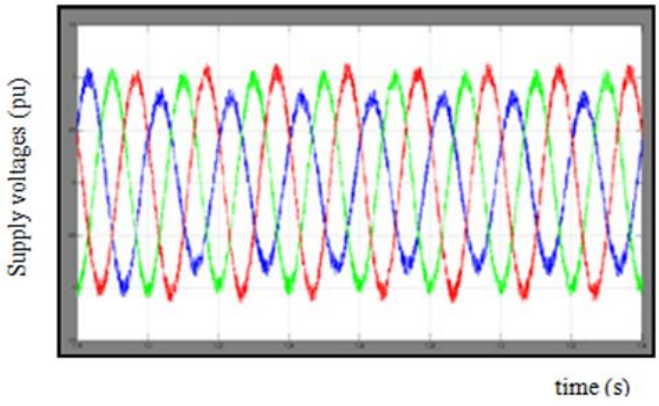

Figure 13. Grid Voltages on the LV side of the Transformer

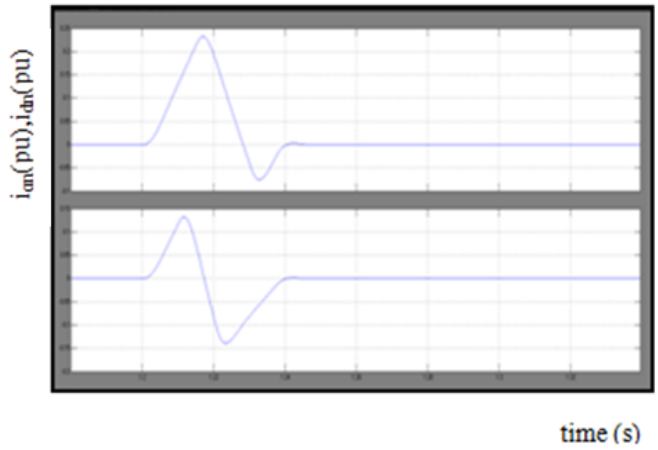

Figure 14. d-axis negative-sequence current component $i'_{dn}$and q-axis negative sequence current component i'_{qn}

4. Fuzzy Logic Controller

The Fuzzy Logic Toolbox extends the MATLAB technical computing environment with tools for designing systems based on fuzzy logic. Graphical user interfaces (GUIs) guide you through the steps of fuzzy inference system design. Functions are provided for many common fuzzy logic methods, including fuzzy clustering and adaptive neuro fuzzy learning. The toolbox lets you model complex system behaviors using simple logic rules and then implements these rules in a fuzzy inference system. You can use the toolbox as a standalone fuzzy inference engine. Alternatively, you can use fuzzy inference blocks in Simulink and simulate the fuzzy systems within a comprehensive model of the entire dynamic system.

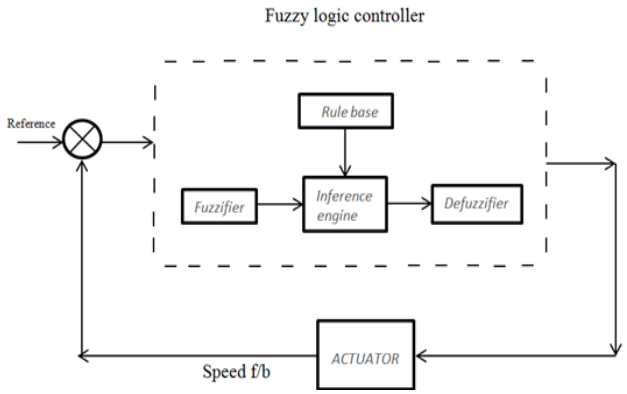

Figure 15. Fuzzy logic controller

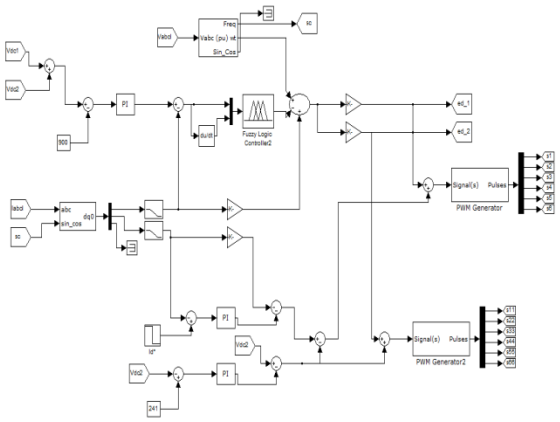

Figure 16. control strategy using Fuzzy logic

5. Simulation diagram for Reactive power control using Fuzzy logic

In this case, reactive power is directly injected into the grid by setting the reference reactive current component i_q* at a particular value. Initially, i_q* is set at 0.5p.u. At t=2.0 s, i_q* is changed to 0.5 p.u. Fig.18 shows the source voltage and converter current of the A phase. Fig.19 shows the dc-link voltages of two inverters. From the figure, it can be seen that the dc-link voltages of the inverters are regulated at their respective reference values when the STATCOM model is changed from capacitive to inductive. Moreover, the dc-link voltage of inverter2 attains its reference value faster compared to that of inverter1.

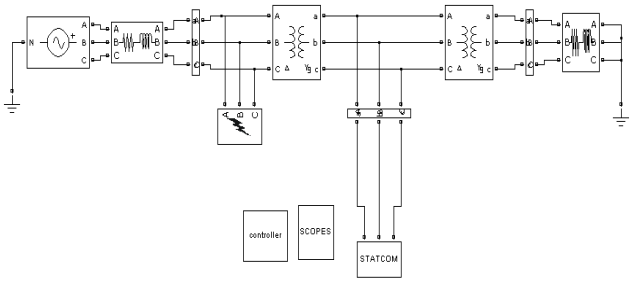

Figure 17. Simulation diagram for Reactive power control using Fuzzy logic

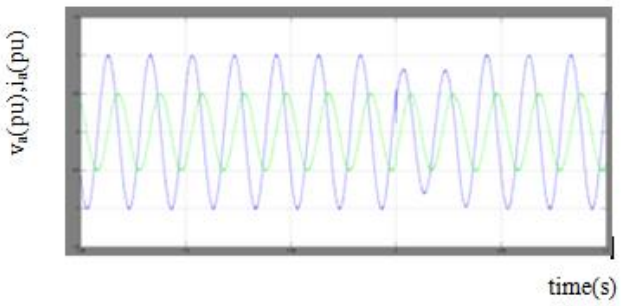

Figure 18. voltage and current source

Figure 19. DC link voltages

6. Simulation diagram of Load Compensation using Fuzzy logic:

In this case, the STATCOM compensates the reactive power of the load. Initially, STATCOM is supplying a current of 0.5 p.u. At t = 2.0 s, the load current is increased so that STATCOM supplies its rated current of 1 p.u. Fig.21 shows source voltage and converter current, while Fig.22 shows the dc-link voltages of two inverters. The dc-link voltages are maintained at their respective reference values when the operating conditions are changed.

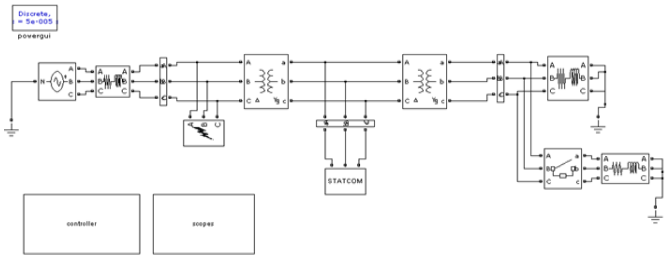

Figure 20. Simulation diagram of LOAD COMPENSATION using Fuzzy logic

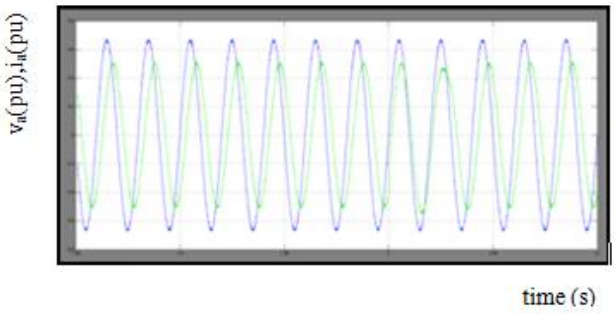

Figure 21. Source Voltage and Current

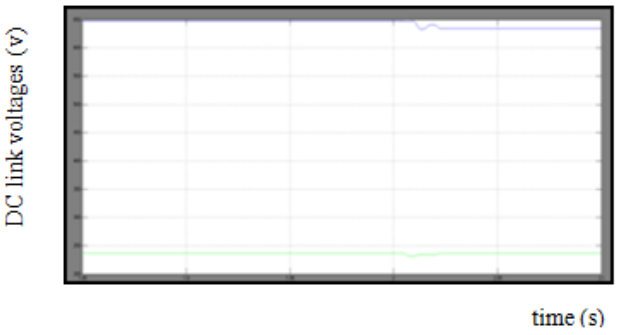

Figure 22. DC link Voltages

7. Simulation diagram for Operation During Fault using Fuzzy logic:

In this case, a single-phase-to-ground fault is created at t=0.2s, on the phase of the HV side of the 33/11-kVtransformer. The fault is cleared after 200 ms. Fig.24 shows voltages across the LV side of the 33/11-kV transformer. Fig.25 shows the d-q axes components of negative-sequence current of the converter. These currents are regulated at zero during the fault condition.

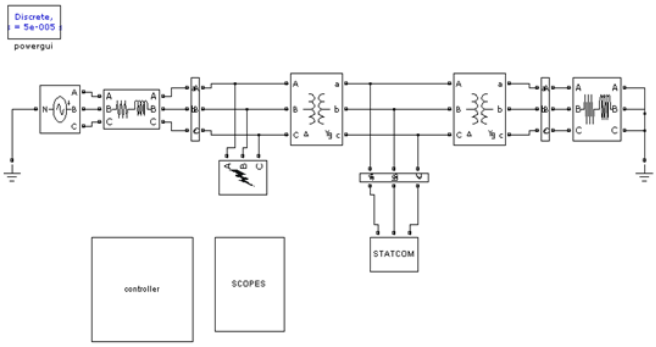

Figure 23. Simulation diagram for OPERATION DURING FAULT using Fuzzy logic

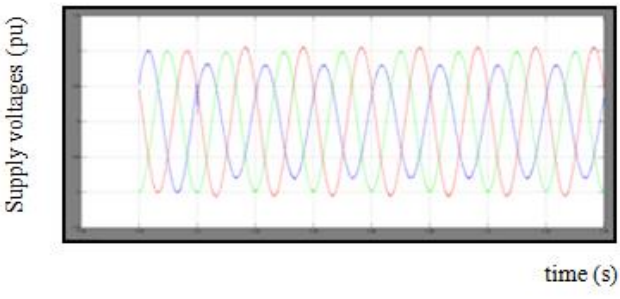

Figure 24. Grid Voltages on the LV side of the Transformer

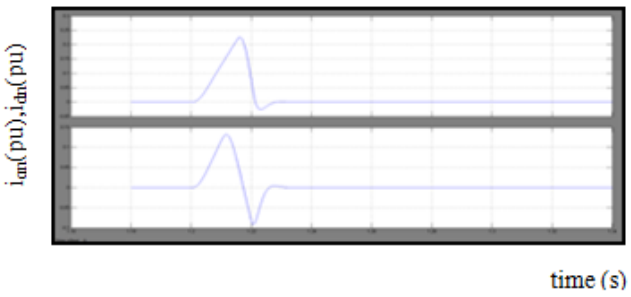

Figure 25. d-axis negative-sequence current component i'_{dn} and q-axis negative sequence current component i'_{qn}

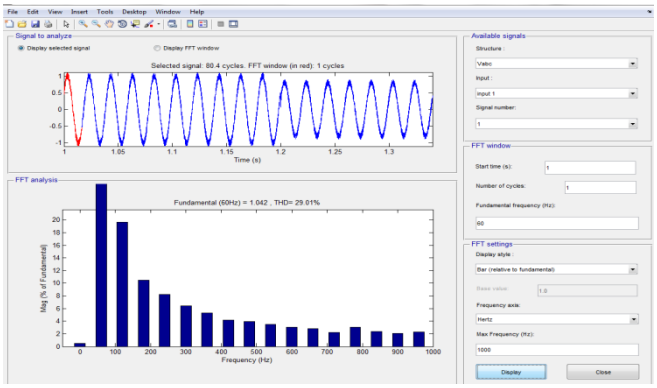

Figure 26. THD of Operation During Fault Condition Using PI Controller

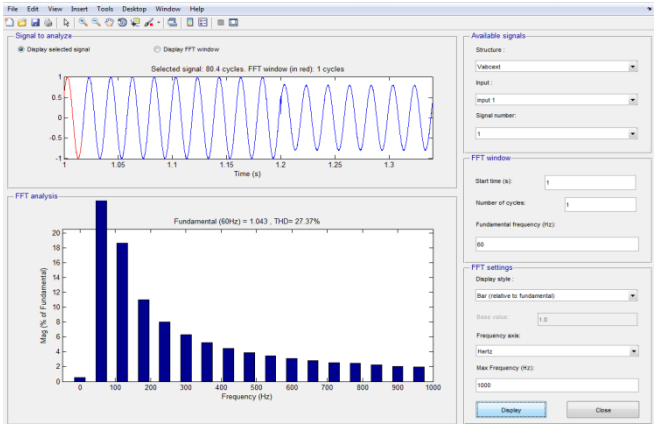

Figure 27. THD of Operation During Fault Condition Using Fuzzy Controller

Fuzzy logic controller can be used in place of PI controllers. Then the performance of the system increases, transients decrease and the stability of the system increases and also the power quality is improved. Recent advanced techniques fuzzy controller based controllers can be implemented so that the ripple content can be further reduced and system performance can be improved.

IV. CONCLUSION

The proposed payment system combines the Iris recognition with the visual cryptography by which customer data privacy can be obtained and prevents theft through phishing attack [8]. This method provides best for legitimate user identification. This method can also be implemented in computers using external iris recognition devices.

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