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Protection Scheme for HVDC Converters to Limit Fault Current against Dc-Side Faults

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ABSTRACT

This paper presents a protection scheme for HVDC converters against DC-side faults with current suppression capability by combining and connecting double thyristor switch scheme across ac output terminals of the HVDC converter. The severity of dc-side faults can be limited by connecting double thyristor switches across the semiconductor devices By turning them on, the ac current contribution into the dc side is eliminated and the dc-link current will freely decay to zero. This protection scheme provides advantages, such as lower dv/dt stresses and lower voltage rating of thyristor switches in addition to providing full separation between the converter semiconductor devices and ac grid during dc-side faults. A simulation case study has been carried out to demonstrate the effectiveness of the proposed scheme.

Keywords : DC-side faults, double thyristor switch, fault current suppression, protection of HVDC converters.

I. INTRODUCTION

Grid integration of renewable energy sources has become essential with increase in energy demand. Among the different renewable energy sources, off-shore wind energy benefits from HVDC technology for power transmission performance improvement.There are several advantages of classical voltage source converter-based-HVDC (VSC-HVDC) and modular multilevel converter-based-HVDC (MMC-HVDC) systems. These systems are expected to be the technology of choice for efficient grid integration. These systems provide: 1) fast and independent control of active and reactive power flow in both directions and 2) low harmonic generation hence the requirement of large filters is minimized. In addition, MMC-HVDC systems also have inherent salient features , such as low switching losses, low total harmonic distortion, modularity, and scalability (scalable to different power and voltage levels).

DC-fault current is the main factor which is severely damaging HVDC systems. In HVDC systems limiting fault currents is important to protect the converter semiconductor devices, which are the most sensitive components in the HVDC systems.

Unfortunately, the classical VSCs and MMCs are defenceless against dc-side faults since, Their freewheeling diodes function as an uncontrolled rectifier bridge and feed the dc fault, even if the semiconductor devices returned off.

During the dc fault, the ac-side current contribution into the dc fault passes through the freewheeling diodes. As a result, the diodes may be damaged due to high fault current. This rectification mode of operation is shown in Fig. 1(a) and (b) for the two-level VSC and MMC during a dc-side fault. In Fig. 1(a), the dc fault current in two-level VSC-HVDC systems emanates from the contribution of the ac grid along with the discharging current of the dc-link capacitor. The discharging current has a large first peak that decays with time. In an MMC-HVDC system, the common dc-link capacitors not utilized, which helps suppress the discharge current. However, the fault current contribution from the acside still exists, that is, there is no separation between thedc and ac sides during dc faults in this topology.

A solid statedc circuit breaker (CB) may be used to overcome the dc-side problems in HVDC converters. Its main drawbacks, however, are cost and the relatively high conduction losses.AC CBs (ACCBs) may be used to achieve the required dc protection, but the free-wheeling diodes used with insulated-gate bipolar transistors (IGBTs) are fast recovery diodes characterized by low surge current withstand capability. These freewheeling diodes should

withstand the fault current until the CB trips. Hence, there is a risk in depending on ACCBs protection only since the semiconductor devices may be damaged due to high fault currents. To enhance the reliability of ac CBsin dc protection, converter-embedded devices may be used in conjunction with the ac CBs.

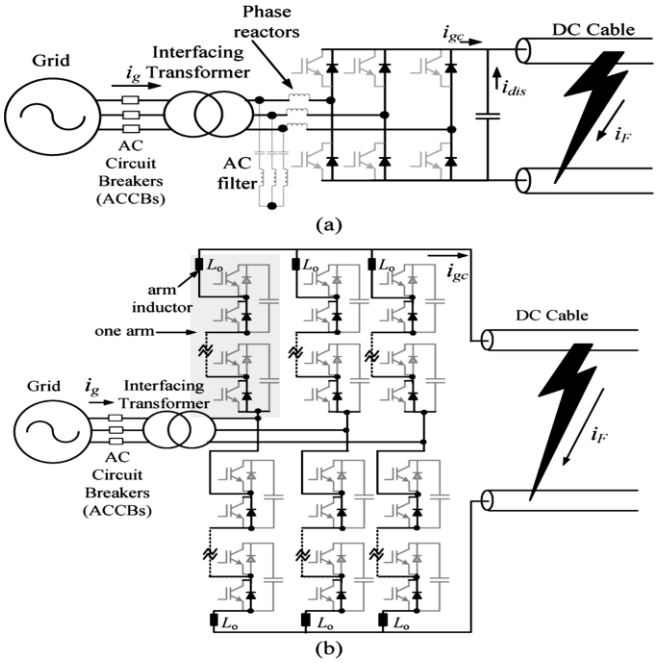

Figure 1. HVDC converters during dc-side faults: (a) 2-level VSC and (b) MMC

In this paper as the severity of fault current is the main factor damaging HVDC systems so to limit fault current the protection scheme is connected across ac output terminals of HVDC systems. This protection scheme is providing lower dv/dt stresses and lower voltage rating of thermistor switches in addition to providing full separation between the converter semiconductor devices and ac grid during dc-side faults.

II. METHODS AND MATERIAL

A. Converter-Embedded Device Protection Scheme

In the single-thyristor switch scheme (STSS), asing lethyristor switch is connected in each submodule of the MMC as shown in Fig. 2(a).The thyristor is used to share the fault current with freewheeling diode, or in other words, to reduce the overcurrent stresses on semiconductor devices pending the tripping of the ACCBs. This can be realized by turning the thyristors on when a dc-side fault is detected. The thyristor has higher capability for withstanding the surge current compared to the freewheeling diode. As a result, most of the fault current flows through the thyristor and not through the diode. Since the STSS protects the semiconductor devices but cannot prevent the grid current contribution into the dc fault, an evolution was later introduced in the literature to address this shortcoming.

The double-thyristor switch scheme (DTSS) proposed in can be used to protect the semiconductor devices by sharing the current with the freewheeling diodes and simultaneously prevent the grid current contribution which allows the dc-link current to freely decay. In this scheme, a double-thyristor switch (back-to-back thyristor) is connected across the semiconductor devices as shown in Fig. 2(b).

The STSS and DTSS can also be applied to the classical VSC configuration by connecting the thyristor across each semiconductor device as shown in Fig. 2(c) and (d), respectively. This paper proposes a new protection scheme for HVDC converters (classical VSCs as well as MMCs). In this scheme, instead of connecting the double-thyristor switches across the semiconductor devices, they are combined and connected across the ac output terminals of the HVDC converter and for on-off control these thyristors PI controller is used. By employing the proposed configuration, all of the aforementioned limitations are mitigated. This paper is organized in six sections. Following the introduction, Section II introduces the architecture of the proposed protection scheme. Section III compares the proposed scheme with other existing schemes (STSS, and DTSS) in terms of stresses, voltage rating, and current rating of the needed thyristors. Section IV illustrates the performance of the dc side during dc faults in two-level VSC-HVDC as well as MMC-HVDC systems considering different types of protection schemes. Section V presents a simulated case study for an HVDC system. Two system models have been developed: one based on a classical 2-level VSC and the other based on an MMC. Four different protective schemes are applied to each model (dc protection with ACCBs only, STSS, DTSS, and connecting protection scheme at output terminals using PI controller scheme). The simulation results show the superiority of the proposed concept with respect to other concepts. Finally, Section VI recaps the main conclusions of this paper.

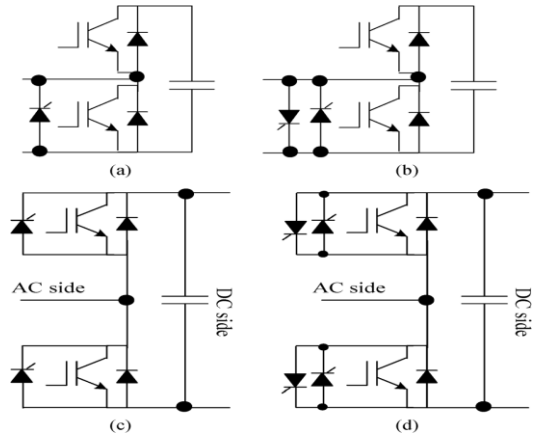

Figure 2. Converter-embedded device protection scheme: (a) STSS for theMMC submodule, (b) DTSS for the MMC submodule, (c) STSS for one leg of two-level VSC topology, and (d) DTSS for one leg of two-level VSC topology).

The main drawbacks of this method are as follows:

- Both thyristors have to withstand high dv/dt during normal operation (high may produce capacitive displacement current in the device, which can cause undesirable turn on).
- A snubber circuit is also essential to prevent damage due to overvoltage spikes and.
- The freewheeling diodes are still sharing the fault current with the thyristors.
- The complexity of implementing an embedded double thyristor switch in each MMC submodule.

B. Protection Scheme Provided Across Ac Output Terminals Of Hvdc Converter

In this scheme, the double-thyristor switches are combined and connected across the ac output terminals of theHVDC converter as shown in Fig. 3. Normally, the thyristors are turned off.When a dc-side fault is initiated, the thyristors are turned on to segregate the HVDC converter from the ac side.

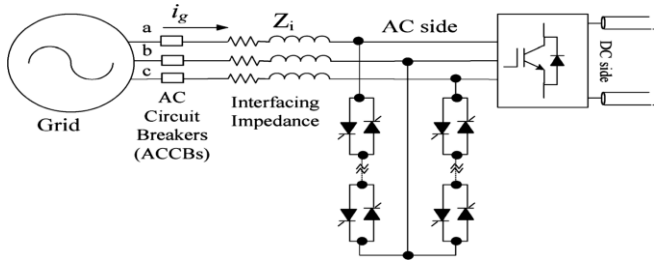

Figure 3. Proposed protection scheme against DC-side faults

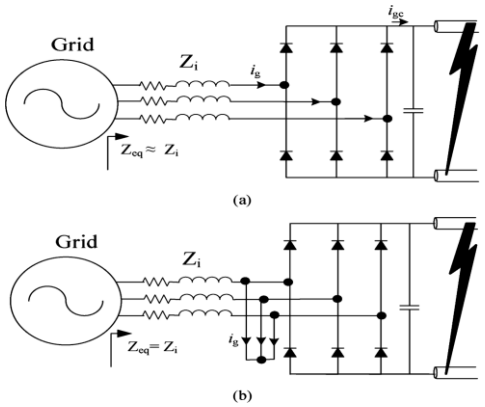

Figure 4. Effect of thyristors firing on the equivalent impedance seen by the grid,in two-level VSC configuration: (a) before and (b) after thyristors firing.

Whenever fault occurs until the tripping of the ACCBs, the proposed scheme can provide the needed protection for the semiconductor devices of the HVDC converter as well as complete segregation between the ac grid and dc side (i.e., grid current contribution is eliminated).In case of a classical two-level VSC, the equivalent impedance seen by the grid during the dc-side fault before and after firing the thyristors is the same, which is equal to the impedance of the interfacing impedance as shown in Fig. 4. Thus, by firing the thyristors, the necessary segregation will be achieved without increasing the magnitude of ac fault Currents.

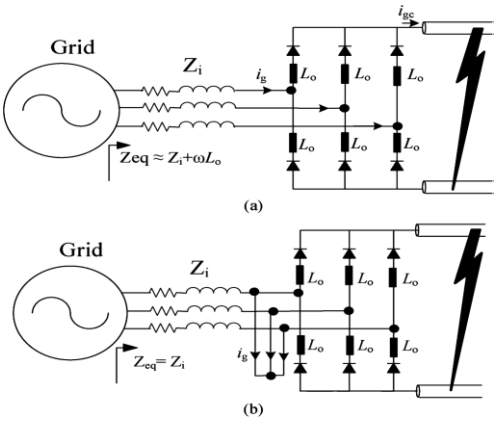

Figure 5. Effect of thyristors firing on the equivalent impedance seen by the grid in MMC configuration: (a) before and (b) after thyristors firing.

In MMC case, the equivalent impedance during a dc-side fault after firing the thyristors[Fig. 5(b)] is lower than its value before firing [Fig. 5(a)] because the arm inductors are no longer part of the circuit during faults when utilizing the proposed scheme as shown in Fig. 5(b).

The main two functions of the arm inductors are .suppression of circulating currents and limiting fault currents. When the proposed scheme is employed, the latter is nolonger a need since the ac current magnitude is not significantly affected during faults; hence, a lower value inductor will suffice.

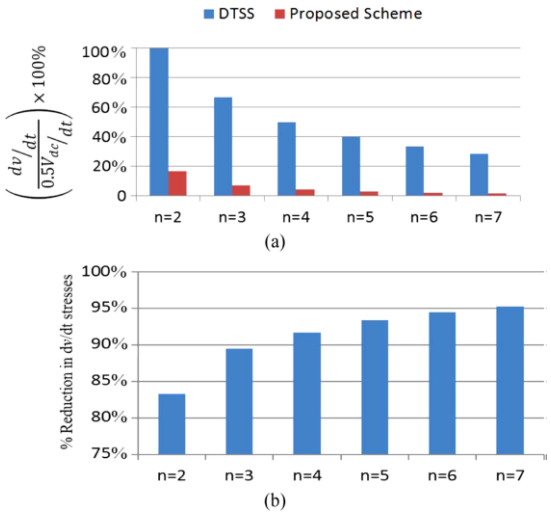

Figure 6. Effect of the proposed scheme on in the MMC configurationfor different numbers of submodules per converter arm: (a) thyristorsstresses for DTSS and the proposed scheme and (b) corresponding percentage
reduction in stresses.

By turning on the combined thyristors on the ac side, the following benefits are gained:

- Complete segregation between the ac grid and converter during dc faults (there is no ac current contribution into the dcfault, that is, there is no high current passing through the freewheeling diodes).
- The ac currents will not be affected by turning the thyristorson, that is, the same ac current magnitudes exist before and after firing of the thyristors.
- The dc-link current will decay freely to zero.once the fault current is zero, the dc side should be disconnected from the dc terminals of the converter; at this instant, the thyristorsmay be turned off and the ac grid current will decrease automatically to zero, since the uncontrolled bridge rectifier is connected to an open circuit after disconnecting the dc side; but if the time needed for fault current to decay to zero is larger than the tripping time of ACCBs (at least three cycles), the ACCBs will disconnect the system from the grid to protect the interfacing transformer and the thyristorswitches, while the dc-link current continues its decay.
- The proposed scheme can provide lower across dv/dt stress across thyristors (this will be discussed in the following section).
- No complicated dc CB is needed in conjunction with this topology since the dc-link current is able to decay freely to zero.
-

$$dv/dt|_{single,VSC}=\pm V_{sw}/T_{on/off}=\pm V_{dc}/T_{on/off} \quad (1)$$

$$dv/dt|_{single,MMC}=\pm(V_{dc}/n)/T_{on/off} \quad (2)$$

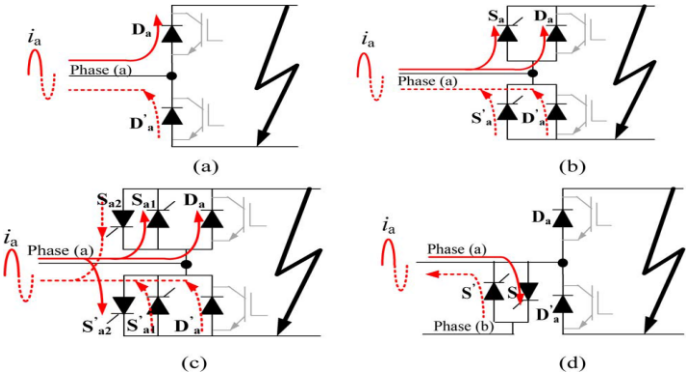

Figure 7. AC current paths during the dc-side fault: (a) ACCBs only, (b) STSS,(c) DTSS, and (d) the proposed scheme

Abovestagesshown existing with two-level VSC and MMC. Among those stages MMC with DTSS type HVDC converter scheme we can completely avoid capacitor discharge current and grid side current feeding.

1. Comparison Between Protection Provided Across Output Terminals of Converter with STSS And DTSS

In this section compares the proposed scheme to other schemes (STSS, and DTSS) in terms of thyristor dv/dt stress, voltage rating, and current rating.

✓ DV/DT Stress and Voltage Rating of the Necessary Thyristors

Thyristors are often subjected to a high rate of voltage change during operation. This produces a capacitive displacement current in the device, which can cause undesirable turn on. This is known as dv/dt the effect, and the maximum dv/dt, for which the device maintains its blocking capability, is known as its dv/dt capability. In this section, a comparison between the thyristors'

dv/dt stresses for the aforementioned protective schemes (STSS, DTSS, and the proposed scheme) is conducted.

Single Thyristor Switch Scheme (STSS)

In the STSS, the thyristor is connected across the semiconductor device.During normal operating conditions, the voltage across semiconductor devices changes between 0 and V_{sw}. In case of a two-level VSC, V_{sw} is equal to the dc-link voltage V_{dc}, while it is equal to the voltage of each sub module's capacitor V_{dc}/n in case of the MMC; where is the number of submodules per arm. The dv/dt on the single-thyristor switch for the two-level VSC and MMC is given by (1) and (2), respectively. Where Ton/off is the time needed for the semiconductor device to change its state from ON to OFF or vice-versa. Six and 6n single-thyristor switches with a voltage rating of $V_{dc}$and V_{dc}/n will be needed for the two-level VSC andMMC configurations, respectively.

Double-Thyristor Switch Scheme (DTSS*):*

In the DTSS, a back-to-back thyristor switch is also connected across each semiconductor device, that is, it will have the same dv/dt as the STSS as follows:

$$dv/dt\ |_{Double,VSC}=\pm V_{sw}/T_{on/off}=\pm V_{dc}/T_{on/off} \quad (3)$$

$$dv/dt\ |_{Double,MMC}=\pm(V_{dc}/n)/T_{on/off} \quad (4)$$

Similarly, six and 6n double-thyristor switches with a voltage rating of V_{dc} and V_{dc}/n will be needed for two-level VSC and MMC configurations, respectively.

Proposed Scheme

In the proposed scheme, the back-tobackthyristors used in the DTSS are combined and divided into two groups (i.e., there are 3 and 3n back-to-back thyristor switches per group for the two-level VSC and MMC, respectively). Each group is connected across the ac terminals of the converter as shown in Fig. 3. As a result, the converter line voltage is applied across each group.

In the classical two-level VSC case, there is a voltage step of $\pm V_{dc}$in each change in converter line voltage. Since, the voltage step is shared between three series back-to-back thyristor switches; the corresponding dv/dt across each thyristor in the proposed scheme can be calculated from

$$dv/dt\ |_{Proposed,VSC}=\pm(V_{dc}/3)/T_{on/off} \quad (5)$$

Comparing (3) and (5) shows that the thyristor dv/dt decreases by 66% using the proposed scheme. In addition, the thyristors with a lower voltage rating may be used. During normal conditions, the highest instantaneous value of line voltage V_{dc} is shared between three series back-to-back thyristor switches, which means a thyristor with a voltage rating of $V_{dc}/3$ may be used, that is, the voltage rating of thyristors also decreases by 66% with the proposed configuration.

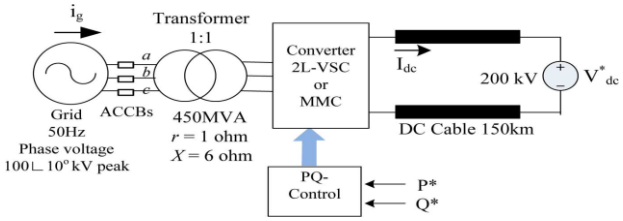

Figure 8. Description of the simulated case study

In the MMC case, there is a voltage step of $\pm V_{dc}$ with each change in the converter line voltage. Since, the voltage step is shared between 3n series back-to-back thyristor switches, the corresponding dv/dt across each thyristor of the proposed scheme is expressed using

$$\frac{dv}{dt}|_{Proposed,MMC}=\pm(V_{sw}/3n)/T_{on/off}=\pm(V_{dc}/3n^2)/T_{on/off} \quad (6)$$

By comparing (4) and (6), the dv/dt across each thyristor is shown to have decreased by ([(3n-1)/3n]*100%) with the proposed scheme. Based on (4) and (6), Fig. 6(a) shows the variation of dv/dt stresses of each thyristor with the number of submodules per arm (n) considering two different protection schemes (DTSS and the proposed scheme). Fig. 6(b) shows the corresponding percentage reduction in dv/dt stresses for each thyristor when the proposed scheme is applied. The highest instantaneous value of line voltage (V_{dc}) is shared between 3n series back-to-back thyristor switches, which means a thyristor with a voltage rating of ($V_{dc}/3n$) may be used instead of (V_{dc}/n), that is, the voltage rating of thyristors also decreases by 66% in the MMC configuration.

✓ **Current Rating of the Necessary Thyristors**

Fig. 7.shows the per-phase paths of ac current during dc-side faults for different types of dc protection schemes (ACCBs only, STSS, DTSS, and the proposed scheme). Fig. 7(a) shows that if ACCBs are used for

protection during dc-side faults, full ac current passes through the freewheeling diodes, which increases the probability of semiconductor devices' damage. The diode currents in this scheme are given by

$$i_{Da}=i_a^+,\ i_{Da}'=i_a^- \quad (6a)$$

Where i_a^+ and i_a^- are the positive and the negative currents of phase "a".

In the STSS, the per-phase ac current will be shared between thethyristors and diodes [Fig. 7(b)] and is split into the terms as

$$i_a^+=i_{Da}+i_{Sa},\ i_a^-=i_{Da}'+i_{Sa}' \quad (7)$$

In the DTSS, the per-phase ac current will be shared between thethyristors and diodes [Fig. 7(c)] and can be divided into three terms as

$$i_a^+=i_{Da}+i_{Sa1}+i_{Sa2}',\ i_a^-=i_{Da}'+i_{Sa1}'+i_{Sa2}' \quad (8)$$

Finally, in the proposed scheme, the full ac current passes through thethyristors as shown in Fig. 7(d).

The steady-state currents of thyristors and diodes during a dc fault in the proposed scheme are given by (9) and (10), respectively

$$i_S=i_a^+,\ i_S'=i_a^- \quad (9)$$
$$i_{Da}=0,\ i_{Da}'=0. \quad (10)$$

It is clear that the thyristorsassociatedwith the proposed scheme will have a higher current rating (because they carry the full ac current). On the other hand, the involved thyristors in the STSS and DTSS are sharing the current with the freewheeling diodes as shown in Fig. 7(b) and (c), respectively; hence, lower current rating devices will be sufficient (approximately half of current).

From the previous subsections, the following points can be concluded:

- The proposed scheme requires thyristors with lower voltage ratings (33% compared to the other schemes).
- The proposed scheme requires thyristors with a higher current rating (200% compared to the other schemes).

For example, if DTSS is applied to the two-level VSC configuration, six double-thyristor switches will be needed with voltage and current ratings of V_{dc} and approximately $0.5I_{sc}$,whereI_{sc} is the magnitude of ac current during the dc fault. On the other hand, six double-thyristor switches will be needed for the proposed scheme with voltage and current ratings of $V_{dc}/3$ and I_{sc}, respectively.

✓ DC Fault Current

In this section illustrates the dc-side performance during dc faults in two-level VSC-based HVDC as well as MMC-HVDC systems. DTSS and the proposed scheme provide complete segregation between the ac and dc sides during dc-side faults; however, dc-side protection with ACCBs only or STSS does not provide this segregation.

➢ Two-Level VSC

1) With Grid Contribution (STSS or AC BeakersOnly):

When the dc fault occurs, the dc fault current goes through three different stages, which can be summarized as follows.

Stage I. Capacitor discharge stage: During this stage, the dc-link capacitor starts discharging. The discharge current has a high peak and decays with time (natural response).

Stage II. Diode freewheel stage: This stage is initiated as the dc fault commutates to the converter freewheeling diodes when the dc-link voltage reaches zero and the cable inductance drives the current around the freewheeling path (each converter leg carries one-third of the fault current). At this stage, the initial diode currents are high which may damage them, then the current decays with time.

Stage III. Grid-side current feeding stage (forced response): During this stage, the dc-link capacitor and cable inductor have a forced current source response, where the grid current contribution into the dc fault (i_{gc}) is the summation of the positive three-phase fault currents.

2) Without Grid Contribution (DTSS or Proposed Scheme):

In this case, the dc fault current will behave as in stage I and II from before. This allows the dc-link current to decay freely to zero (dc fault current suppression capability).

- **MMC**

Due to the MMC topology, the dc-link capacitors are no longer connected to the dc side during dc faults [Fig. 1(b)], that is, no discharge currents are flowing under dc fault conditions.

Without Grid Contribution (DTSS or the Proposed Scheme)

Upon fault inception, the diode freewheeling stage (Stage II) is initiated as the cable inductance drives the current around the freewheeling path dissipating its energy in the cable resistance. It should be noted that there are three freewheeling paths and that each one carries one-third of the fault current and consists of two freewheeling diodes in series with two arm inductors. The current will have an exponential current decay until reaching zero (dc fault current suppression capability).

With Grid Contribution (STSS or ACCBs Only):

The dc fault current will behave as in Stage IIIof the aforementioned three stages, that is, the dc-link current will increase to a value equal to the summation of the positive three-phase fault currents after incidence of the fault. The performance of the dc side during dc-side faults for all of the aforementioned cases is discussed.

C. Fuzzy Logic Controller

A Fuzzy Logic Control System is a control system based on fuzzy logic "a mathematical system that analyzes analog input values in terms of logical variables that take on continuous values between 0 and 1 and gives the requisite response according to the defined rules, in contrast to classical or digital logic, which operates on discrete values of either 1 or 0 (true or false, respectively)".Among the various intelligent controllers, fuzzy logic controller (FLC) is the simplest , robust and better than others in terms of quick response time, also insensitivity to parameter and load variations etc. Thus, here a FLC is implemented as another velocity (speed) and displacement controller of an actuation system and also to study the performance comparison of an actuator with PID controller based drive in MATLAB/Simulink environment.

The outer loops such as velocity loop (speed loop) and displacement loop affects the system performance. Proportional plus integral plus derivative (PID) controllers are usually preferred, but because of its fixed proportional gain constant, integral time constant and derivative constant, the behavior of the PID controllers are suffers from settling time and overshoot of response. These problems can be overcome by the fuzzy logic controllers, which do not require any mathematical model and are based on the linguistic control law obtained from the experience of the system operator. Also the problem of time settling and overshoot can be alleviate by FLC.

The Fuzzy Logic Controller (FLC) is the rule based, non-linear controller which takes the analog inputs and analyses it by converting it to logical variables and gives the output by defuzzification. In this case we are considering the speed error (e) as input for the controller. But the performance of the fuzzy controller as compared to the PID controller is superior mainly under transient conditions.

There are four important elements in the fuzzy logic controller system structure which are fuzzifier, rule base, inference engine anddefuzzifier as shown in fig.9. Firstly, a crisp set of input data are gathered and converted to a fuzzy set using fuzzy linguistic variables, fuzzy linguistic terms and membership functions. This step also known as fuzzification. Afterwards, an inference is made base on a set of rules. Lastly, the resulting fuzzy output is mapped to a crisp output using the membership functions, in the defuzzificationstep.The fuzzy Logic Toolbox extends the MATLAB technical computing environment with tools for designing systems based on fuzzy logic. Graphical user interfaces (GUIs) guide you through the steps of fuzzy inference system design. Functions are provided for many common fuzzy logic methods, including fuzzy clustering and adaptive neuro fuzzy learning. The toolbox lets you model complex system behaviors using simple logic rules and then implements these rules in a fuzzy inference system. You can use the

toolbox as a standalone fuzzy inference engine. Alternatively, you can use fuzzy inference blocks in Simulink and simulate the fuzzy systems withina comprehensive model of the entire dynamic system.

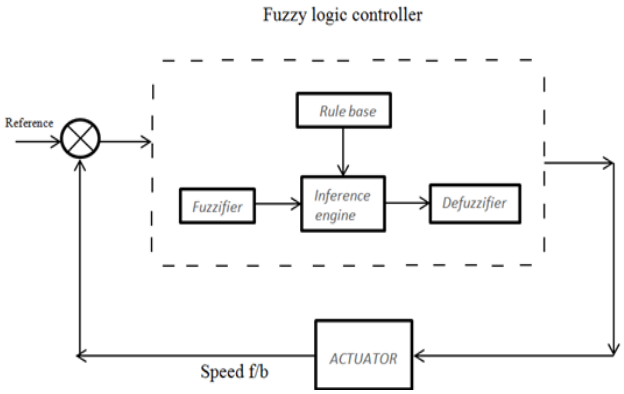

Figure 9. Fuzzy logic controller

RULE BASE

Fuzzy logic's linguistic terms are most often expressed in the form of logical implications, such as If-Then rules. These rules define a range of values.Different membership functions used are,

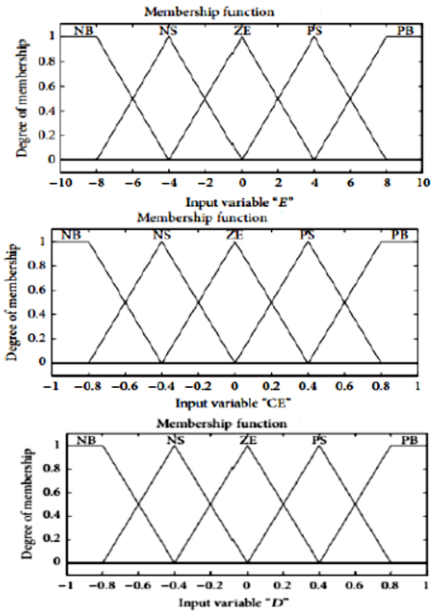

Fig.8: The membership functions of E, CE, and D.

Truth Table : Twenty-Five Fuzzy Rule Subset

↓ E /CE→	NB	NS	ZE	PS	PB
NB	ZE	ZE	PB	PB	PB
NS	ZE	ZE	PS	PS	PS
ZE	PS	ZE	ZE	ZE	NS
PS	NS	NS	ZE	ZE	ZE
PB	NB	NB	ZE	ZE	ZE

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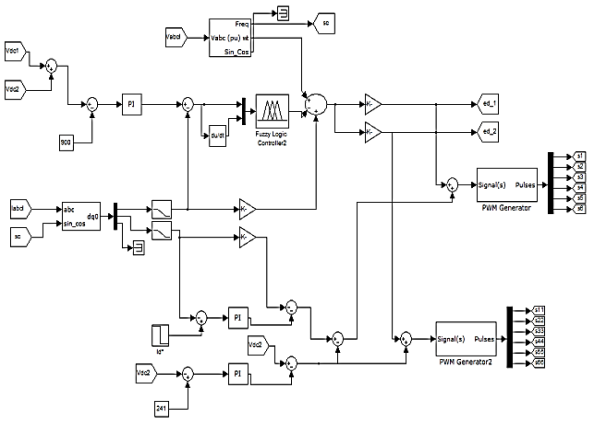


Figure 10. Control strategy using Fuzzy logic

III. RESULTS AND DISCUSSION

A. Simulation Results

The system configuration shown in Fig.8 is considered for simulation. The simulation study is carried out using MATLAB/SIMULINK. The system parameters are given in table.

TABLE 1
SIMULATION SYSTEM PARAMETER

AC Side	
Rated(Base) Power	450MVA
Grid phase voltage	100KV(peak)
Rated(Base) AC phase current	3000A(peak)
Three-phase transformer ratio	1:1
Active power reference	430MW
Reactive power reference	-100MVAR
Transformer resistance	1Ω

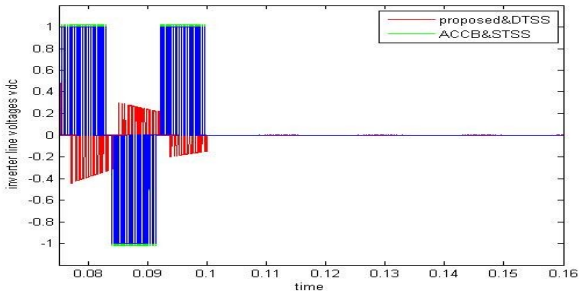
Transformer reactance	6Ω
DC Side	
Rated(base)DC voltage,V_{dc}^{*}	200kv
Rated(base)DC current	2250A
DC cable length	150km
DC cable resistance	14 mΩ/km
DC cable inductance	0.1 mH/km
2-level VSC	
DC-link capacitor	100μF
MMC	
Arm inductor,L_O	3mH

B. Simulation Results for Protection Schemes Usingpi Controller

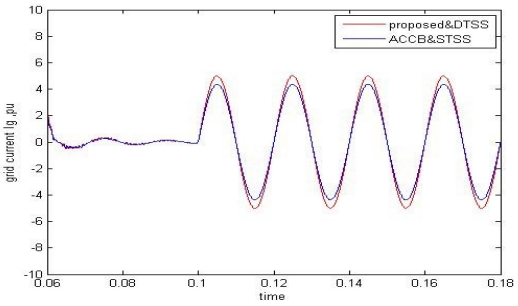
Proportional integral controller is a proportional gain in parallel with an integrator; both in series with a lead controller. The proportional gain provides fast error response. The integrator drives the system to a 0 steady-state error.

1. Two level VSC converter

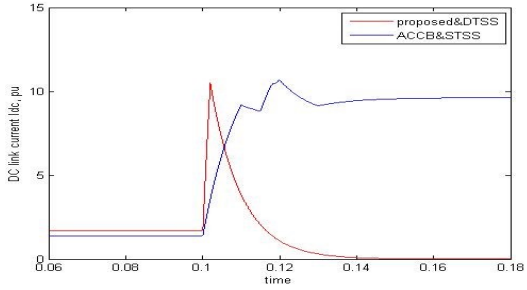
The simulation of configuration system is done by considering fault at time t=0.1 sec,main aim of this paper is decreasing dv/dt stress across each semiconductor device of converter.For protection scheme connected across output terminals of two level VSC converter using PI controller is getting dv/dt stress value 66.6kv/us which is better low value compared with other schemes in two level inverter.



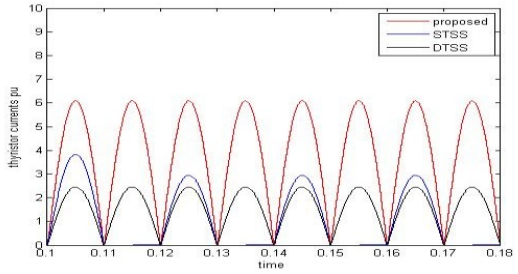
(a) Converter line voltage characteristics



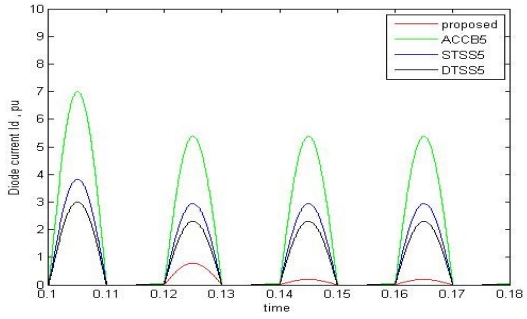
(b) Grid current characteristics



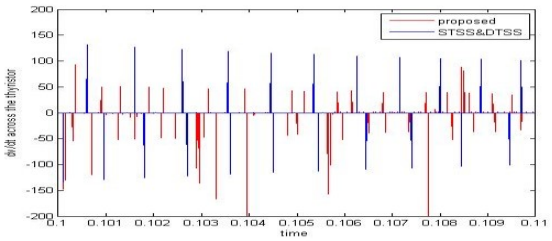
(c) DC-link current characteristics



(d)Thyristor current characteristics



(e) Diode current characteristics



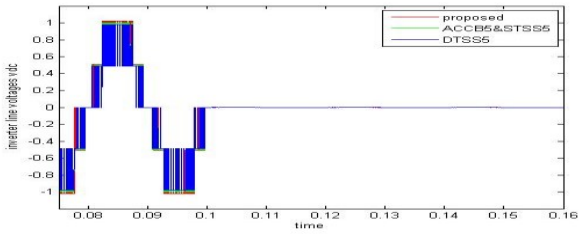
(f) dv/dt stresses characteristics

Figure 11. Simulation results for the two-level VSC case: (a) converter line voltage, (b) per-phase grid current, (c) dc-link current, (d) thyristors currents for differentprotection schemes during the dc fault, (e)

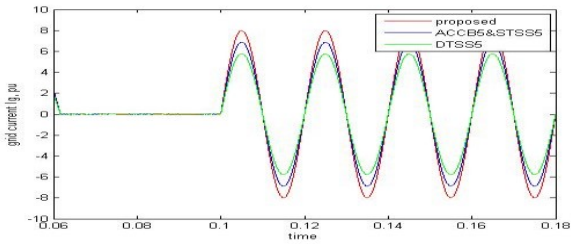
freewheeling diode current for different protection schemes during the dc fault, and (f) dv/dtstresses across each thyristorfor different protection schemes during normal operating conditions.

2. Three level MMC converter

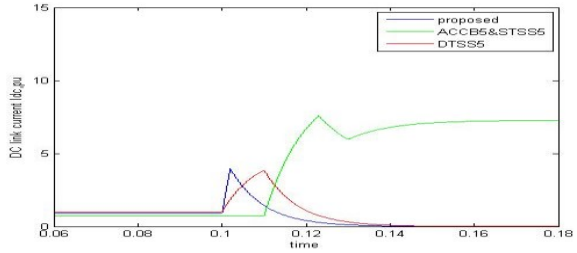
The simulation of configuration system is done by considering fault at time t=0.1 sec,main aim of this paper is decreasing dv/dt stress across each semiconductor device of converter.For protection scheme connected across output terminals of three level MMC converter using PI controller is getting dv/dt stress value 16.6kv/us which is better low value compared with other schemes in two level inverter.



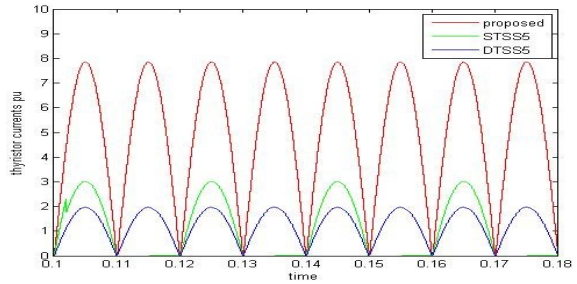
(a) Converter line voltage characteristics



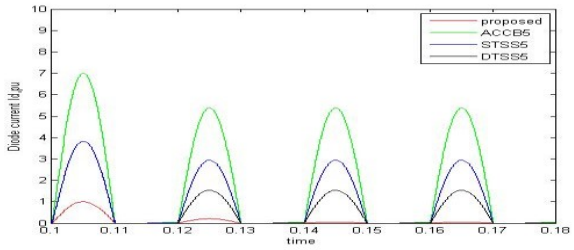
(b) Grid current characteristics



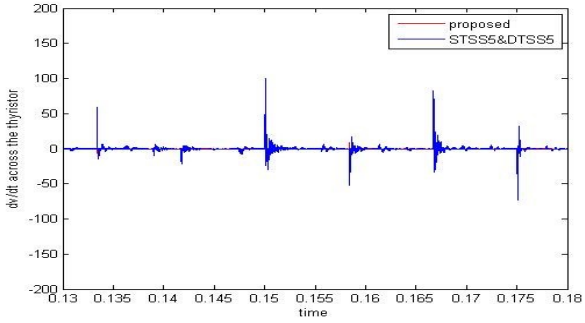
(c) DC-link current characteristics



(d) Thyristor current characteristics



(e) Diode current characteristics



(f) dv/dt stresses characteristics

Figure 12. Simulation results for three-level MMC : (a) converter line voltage, (b) per-phase grid current, (c) dc-link current, (d) thyristor currents fordifferent protection schemes during the dc fault, (e) freewheeling diode current for different protection schemes during the dc fault, and (f)dv/dt stresses across each thyristor for different protection schemes during normal operating conditions.

Drawbacks of PI controller:

1. Applicable only for constant loads.
2. Mathematical calculations are more so time taken is more.
3. Speed of operation is low.

Advantages of fuzzy controller:
1. Applicable for variable loads
2. Mathematical calculations are less so time taken is less
3. Speed of operation is more when compared to PI controller.

C. Simulation Results For Protection Schemes uising Fuzzy Controller

In the converter embedded device protection scheme the protection scheme is connected across each semiconductor device of converter.In this paper the PI controllers are used in generating reference voltage which is used for thyristor firing pulses generation. But

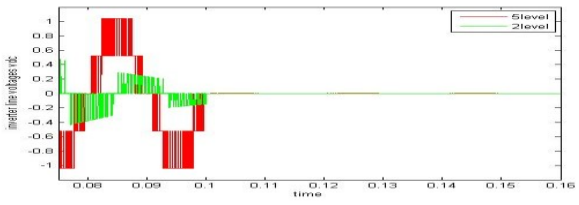
PI controller is applicable only for constant loads. Fuzzy logic controller can be used in place of PI controllers. Then the performance of the system increases, transients decrease and the stability of the system increases and also the power quality is improved. Recent advanced techniquesfuzzy controller based controllers can be implemented so that theripple content can be further reduced and system performance can be improved.

Two level VSC converter

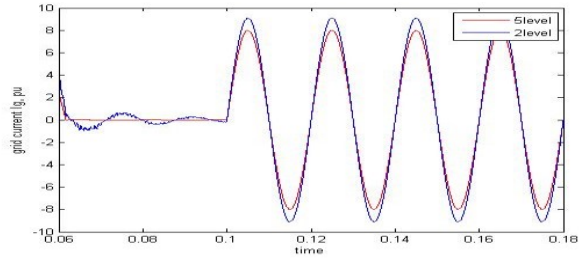
The simulation of configuration system is done by considering fault at time t=0.1 sec,main aim of this paper is decreasing dv/dt stress across each semiconductor device of converter.For protection scheme connected across output terminals of two level VSC converter using fuzzy controller is getting dv/dt stress value 44.7kv/us which is better low value compared with other schemes in two level inverter.

Three level MMC converter

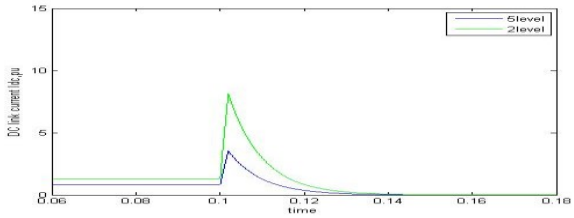
The simulation of configuration system is done by considering fault at time t=0.1 sec,main aim of this paper is decreasing dv/dt stress across each semiconductor device of converter.For protection scheme connected across output terminals of three level MMC converter using fuzzy controller is getting dv/dt stress value 15.2kv/us which is better low value compared with other schemes in two level inverter.



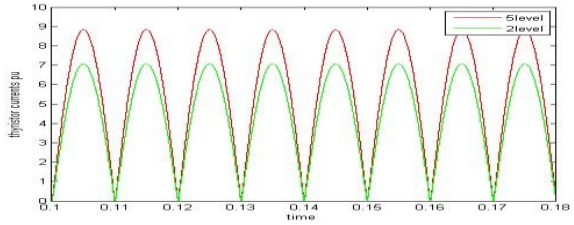
(a) Converter line voltage characteristics



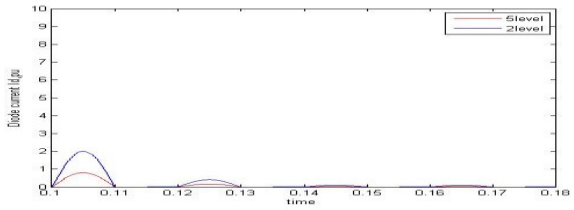
(b) Grid current characteristics



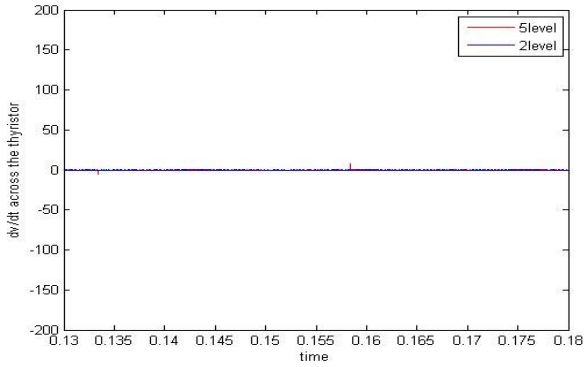
(c) DC-link current



(d) Thyristor current characteristics



(e) Diode current characteristics



(f) dv/dt stresses characteristics

Figure 13. Simulation results for two-level and three level converters (a) converter line voltage, (b) per-phase grid current, (c) dc-link current, (d) thyristors currents for differentprotection schemes during the dc fault, (e) freewheeling diode current for different protection schemes during the dc fault, and (f) dv/dt stresses across each thyristor for different protection schemes during normal operating conditions.

IV. CONCLUSION

By connecting protection scheme with fuzzy controller across each semiconductor device of converter the peak magnitude of DC-link current and dv/dt stress across each semi conductor device is reduced to minimum

value so that converters are protected during DC-side faults and also that withstanding capability for higher thyristor currents is also increased.

Seven cells per arm are used in this paper in order to achieve acceptable simulation times without compromising result accuracy, as each system component is represented in detailed. Also, the hybrid converter with seven H-bridge cells per phase, which is the same as the two-switch modular multilevel converter, for the same dc link voltage such that devices in both converters experience the same voltage stresses.

The converters are configured to regulate active power exchange and dc link voltage, and ac voltage magnitudes respectively.

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