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BIST Schemes for Low Power High Fault Test Pattern Generation

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ABSTRACT

BIST is a viable approach to test today's digital systems. During self-test, the switching activity of the Circuit under Test (CUT) is significantly increased compared to normal operation and leads to an increased power consumption which often exceeds specified limits. The proposed method generates Multiple Single Input Change (MSIC) vectors in a pattern. The each generated vectors are applied to a scan chain is an SIC vector. A class of minimum transition sequences is generated by the use of a reconfigurable Johnson counter and a scalable SIC counters. The proposed TPG method is flexible to both the test-per-scan schemes and the test-per-clock. A theory is also developed to represent and analyse the sequences and to extract a class of MSIC sequences. The proposed BIST TPG decreases transitions that occur at scan inputs during scan shift operations and hence reduces switching activity in the CUT. As the switching activity is reduced, the power consumption of the circuit will also be reduced.

Keywords : Built-in self-test (BIST), Circuit Under Test (CUT), Low Power, Single-Input Change (SIC), Test Pattern Generator (TPG), Linear Feedback Shift Register (LFSR).

I. INTRODUCTION

A digital system is tested and diagnosed during its lifetime for several times. Test and diagnosis techniques applied to the system must be speedy and have very high fault coverage. One method to ensure this is to specify test as system functions, so it becomes Built In Self Test. It reduces the complexity and difficulty in VLSI testing, and thereby decreases the cost and reduces reliance upon external (pattern-programmed) test equipment. Test pattern generators (TPGs) comprising of linear feedback shift register (LFSR) are used in the conventional BIST architectures. The major negative aspect of these architectures is that the pseudorandom patterns generated by the LFSR results in the high switching activities in the CUT. It can damage the circuit and the lifetime, product yield will be reduced. In addition, the target fault coverage is achieved by generating very long pseudorandom sequences by LFSR.

A. Prior Work

Several advanced BIST techniques have been studied and applied. The first class is the LFSR tuning. Girard et al. analyzed the impact of an LFSR's polynomial and seed selection on the CUT's switching activity, and proposed a method to select the LFSR seed for energy reduction.

The second class is low-power TPGs. One approach is to design low-transition TPGs. Wang and Gupta used two LFSRs of different speeds to control those inputs that have elevated transition densities [5]. Cornoetal. Provided a low power TPG based on the cellular automata to reduce the test power in combinational circuits [6]. Another approach focuses on modifying LFSRs. The scheme in [7] reduces the

power in the CUT in general and clock tree in particular. In [8], a low-power BIST for data path architecture is proposed, which is circuit dependent. So the nondetecting subsequences must be determined for each circuit test sequence. Bonhomme et al. [9] used a clock gating technique where two no overlapping clocks control the odd and even scan cells of the scan chain so that the shift power dissipation is reduced by a factor of two. The ring generator [10] can generate a single-input change (SIC) sequence which can effectively reduce test power. The third approach focuses on reducing the dynamic power dissipation during scan shift through gating of the outputs of a portion of the scan cells. Bhuniaetal. [11] inserted blocking logic into the stimulus path of the scan flip-flops to prevent the propagation of the scan ripple effect to logic gates. The need for transistors insertion, however, makes it difficult to use with standard cell libraries that do not have power-gated cells. In [12], the efficient selection of the most suitable subset of scan cells for gating along with their gating values is studied.

The third class makes use of the prevention of pseudorandom patterns that do not have new fault detecting abilities [13]–[15]. These architectures apply the minimum number of test vectors required to attain the target fault coverage and therefore reduce the power. However, these methods have high area overhead, need to be customized for the CUT, and start with a specific seed. Gerstendorfer et al. also proposed to filter out non detecting patterns using gate-based blocking logics [16], which, however, add significant delay in the signal propagation path from the scan flip-flop to logic. Several low-power approaches have also been proposed for scan-based BIST. The architecture in [17] modifies scan-path structures, and lets the CUT inputs remain unchanged during a shift operation. Using multiple scan chains with many scan -enable (SE) Inputs to activate one scan chain at a time, the TPG proposed in [18] can reduce average power consumption during scan -based tests and the peak power in the CUT. In [19], a pseudorandom BIST scheme was proposed to reduce switching activities in scan chains. Other approaches include LT-LFSR [20], a low-transition random TPG [21], and the weighted LFSR [22]. The TPG in [20] can reduce the transitions in the scan inputs by assigning the same value to most neighbouring bits in the scan chain. In [21], power reduction is achieved by increasing the correlation between consecutive test patterns. The weighted LFSR in [22] decreases energy consumption and increases fault coverage by adding weights to tune the pseudorandom vectors for various probabilities.

B. Contribution and Paper Organization

This paper presents the theory and application of a class of minimum transition sequences. The proposed method generates SIC sequences, and converts them to low transition sequences for each scan chain. This can decrease the switching activity in scan cells during scan-in shifting. The advantages of the proposed sequence can be summarized as follows.

1. Minimum transitions
2. Uniqueness of patterns
3. Uniform distribution of patterns
4. Low hardware overhead consumed by extra TPGs

The rest of this paper is organized as follows. In Section II, the proposed MSIC-TPG scheme is presented. The principle of the new MSIC sequences is described in Section III. In Section IV, the properties of the MSIC sequences are analyzed. In Section V, experimental methods and results on test power, fault coverage, and area overhead are provided to demonstrate the performance of the proposed MSIC-TPGs. Conclusions are given in Section VI.

II. PROPOSED MSIC-TPG SCHEME

This section develops a TPG scheme that can convert an SIC vector to unique low transition vectors for multiple scan chains. First, the SIC vector is decompressed to its multiple code words. Meanwhile, the generated code words will bit-XOR with a same seed vector in turn. Hence, a test pattern with similar test vectors will be applied to all scan chains.

The proposed MSIC-TPG consists of an SIC generator, a seed generator, an XOR gate network, and a clock and control block.

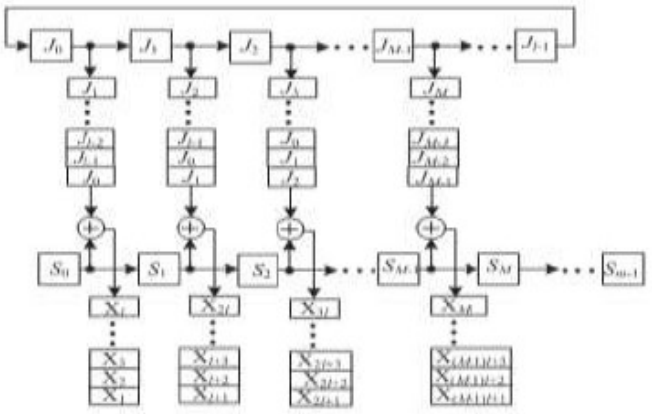


Figure 1. Symbolic simulation of an MSIC pattern for scan chains

I.Test Pattern Generation Method

Assume there are m primary inputs (PIs) and M scan chains in a full scan design, and each scan chain has l scan cells. Fig. 1 shows the symbolic simulation for one generated pattern. The vector generated by an m-bit LFSR with the primitive polynomial can be expressed as S(t) = S0(t)S1(t)S2(t), . . . , Sm–1(t) (hereinafter referred to as the seed), and the vector generated by an l-bit Johnson counter can be expressed as J (t) = J0(t)J1(t)J2(t), . . . , Jl–1(t).

Since the circular Johnson counter can generate l unique Johnson code words through circular shifting a Johnson vector, the circular Johnson counter and XOR gates in Figure 1 actually constitute a linear sequential de compressor.

II. Reconfigurable Johnson counter

According to the different scenarios of scan length, this paper develops two kinds of SIC generators to generate Johnson vectors and Johnson code words, i.e., the reconfigurable Johnson counter and the scalable SIC counter.

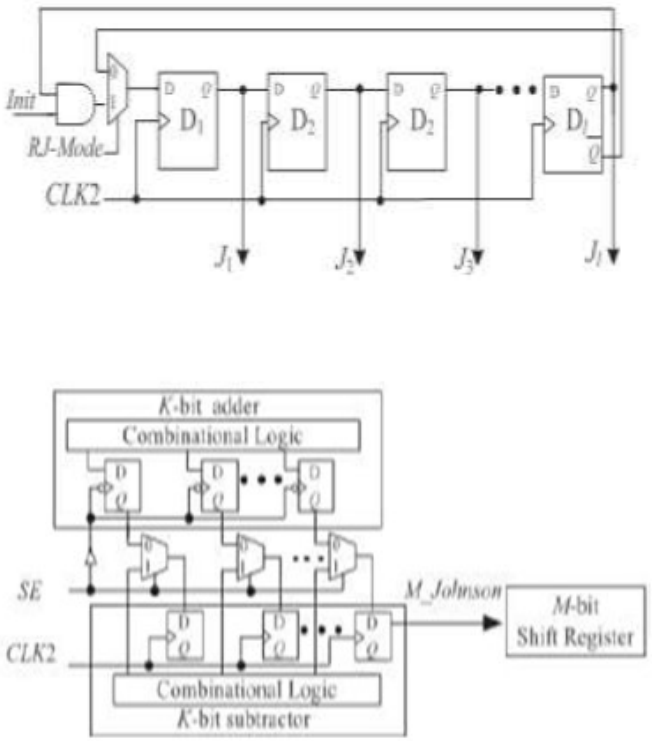


Figure 2. SIC generators. (a) Reconfigurable Johnson counter. (b) Scalable SIC counter.

For a short scan length, we develop a reconfigurable Johnson counter to generate an SIC sequence in time domain. As shown in Fig. 2(a), it can operate in three modes.

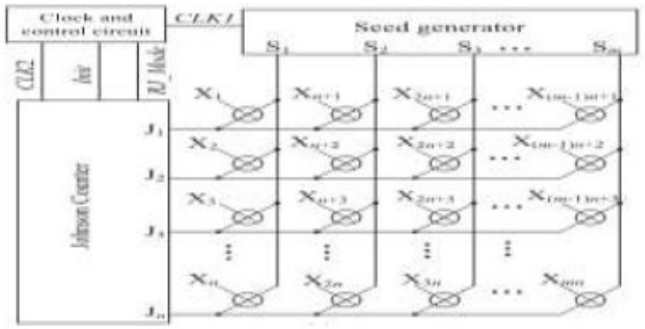
1. **Initialization:** When RJ_Mode is set to one and Init is set to logic zero, the reconfigurable Johnson counter will be initialized to all zero states by clocking CLK2 more than l times.
2. **Circular shift register mode:** When RJ_Mode and Init are set to logic one, each stage of the Johnson counter will output a Johnson codeword by clocking CLK2 l times.
3. **Normal mode:** When RJ_Mode is set to logic zero, the reconfigurable Johnson counter will generate 2l unique SIC vectors by clocking CLK2 2l times.

III. Scalable SIC Counter

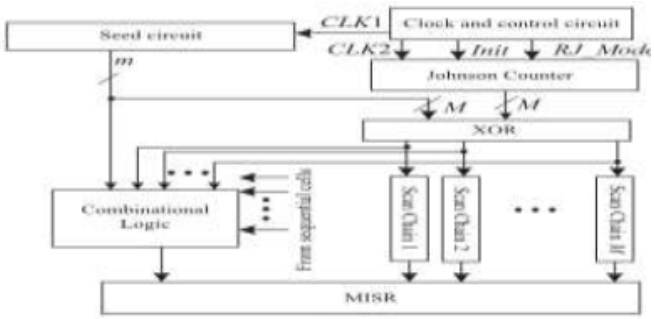
When the maximal scan chain length l is much larger than the scan chain number M, we develop an SIC counter named the–scalable SIC counter.‖ As shown in Fig. 2(b), it contains a k-bit adder clocked by the rising SE signal, a k-bit subtractor

clocked by test clock CLK2, an M-bit shift register clocked by test clock CLK2, and k multiplexers. The value of k is the integer of log2 (l–M). The waveforms of the scalable SIC counter are shown in Fig. 2(c). The k-bit adder is clocked by the falling SE signal, and generates a new count that is the number of 1s (0s) to fill into the shift register. As shown in Fig. 2(b), it can operate in three modes.

1. If SE = 0, the count from the adder is stored to the k-bit subtractor. During SE = 1, the contents of the k-bit subtractor will be decreased from the stored count to all zeros gradually.
2. If SE = 1 and the contents of the k-bit subtractor are not all zeros, M-Johnson will be kept at logic 1 (0).
3. Otherwise, it will be kept at logic 0 (1). Thus, the needed 1s (0s) will be shifted into the M-bit shift register by clocking CLK2 ltimes, and unique Johnson codewords will be applied into different scan chains.



(a)



(b)

Figure 3. MSIC-TPGs for (a) test-per-clock and (b) test- per-scan schemes

IV. MSIC-TPGs for Test-per-Clock Schemes

The MSIC-TPG for test-per-clock schemes is illustrated in Fig. 3(a). The CUT's PIs X1 – Xmn are arranged as an nxm SRAM-like grid structure. Each grid has a two-input XOR gate whose inputs are tapped from a seed output and an output of the Johnson counter. The outputs of the XOR gates are applied to the CUT's PIs. A seed generator is an m stage conventional LFSR, and operates at low

Frequency CLK1. The test procedure is as follows.

1. The seed generator produces a new seed by clocking CLK1 one time.
2. The Johnson counter generates a new vector by clocking CLK2 one time.
3. Repeat 2 until 2l Johnson vectors are generated.
4. Repeat 1–3 until the expected fault coverage or test length is achieved.

V. MSIC-TPGs for Test-per-Scan Schemes

The MSIC-TPG for test-per-scan schemes is illustrated in Fig. 3(b). The stage of the SIC generator is the same as the maximum scan length, and the width of a seed generator is not smaller than the scan chain number. The seed generator and the SIC counter produces the vectors which are given as the inputs of the XOR gates and their outputs are applied to M scan chains, respectively. The outputs produced by the seed generator and XOR gates are given to the CUT's PIs, respectively. The test procedure is as follows.

1. The seed circuit generates a new vector by clocking CLK1 one time.
2. RJ_Mode is set to –0‖. The reconfigurable Johnson counter will operate in the Johnson counter mode and generate a Johnson vector by clocking CLK2 one time.
3. After a new Johnson vector is generated, RJ_Mode and Init are set to one. The reconfigurable Johnson counter will operates as a circular shift register, and generates l codewords by clocking CLK2 l times.

4. Repeat the 2–3 steps until 2l times of Johnson vectors are generated.
5. Repeat 1–4 until the expected fault coverage or test length is achieved.

III. PRINCIPLE OF MSIC SEQUENCES

The main objective of the proposed algorithm is to reduce the switching activity. In order to reduce the hardware overhead, the
linear relations are selected with consecutive vectors or within a pattern, which can generate a sequence with a sequential de compressor, facilitating hardware implementation.
Finally, uniformly distributed patterns are desired to reduce the test length (number of patterns required to achieve a target fault coverage) [21]. This section aims to extract a class of test sequences that meets these requirements.

IV. PROPERTIES OF MSIC SEQUENCES

A. Switching Activity Reduction

For test-per-clock schemes, M segments of the CUT's primary inputs are applied with M unique SIC vectors. The mean input transition density of the CUT is close to 1/l. For test-per-scan schemes, the CUT's PIs are kept unchanged during 2l2 shifting-in clock cycles, and the transitions of a Johnson codeword are not greater than 2. Therefore, the mean input transition density of the CUT during scan-in operations is less than 2/l.

B. Uniform Distribution of MSIC Patterns

If test patterns are not uniformly distributed, there might be some inputs that are assigned the same values in most test patterns.
Hence, faults that can only be detected by patterns that are not generated may escape, leading to low fault coverage. Therefore, uniformly distributed test patterns are desired for most circuits in order to achieve higher fault coverage [5].

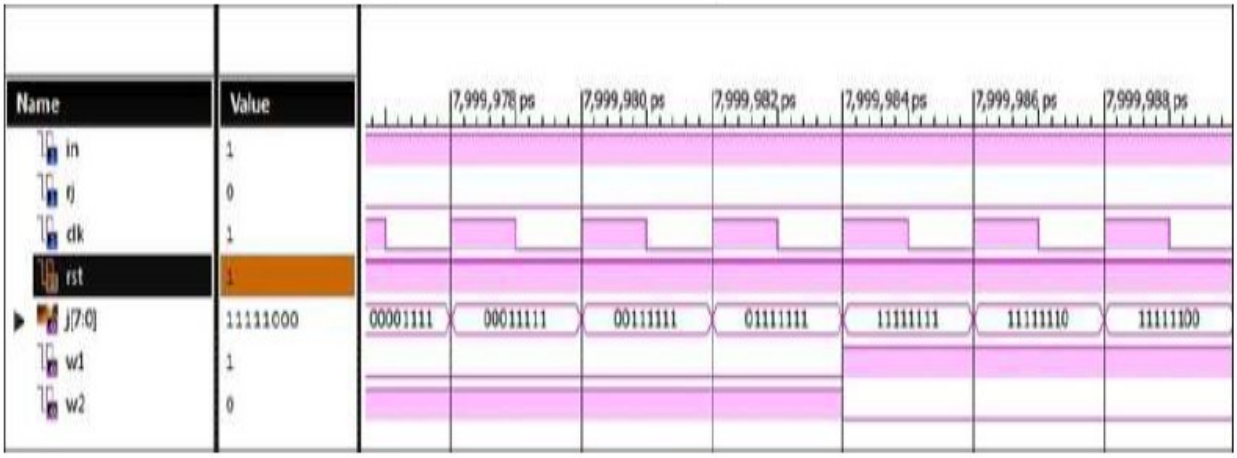
C. Relationship Between Test Length and Fault Coverage

The test length of conventional LFSR methods is related to the initial test vector. In other words, the number of patterns to hit the target fault coverage depends on the initial vector in conventional LFSR TPGs [21].

V. PERFORMANCE ANALYSIS

To analyze the performance of the proposed MSIC-TPG, experiments on ISCAS'85 benchmarks and standard full-scan designs of ISCAS'89 benchmarks are conducted. The performance simulations are carried out with the Xilinx ISE 12.3 and ISIM Simulator. Fault simulations are carried out with ISIM Simulator. Synthesis is carried out with Xilinx ISE 12.3 based on 45-nm typical technology. The test frequency is 100 MHz, and the power supply voltage is 1.1 V. The test application method is test-per-clock for ISCAS'85 benchmarks.

(a)



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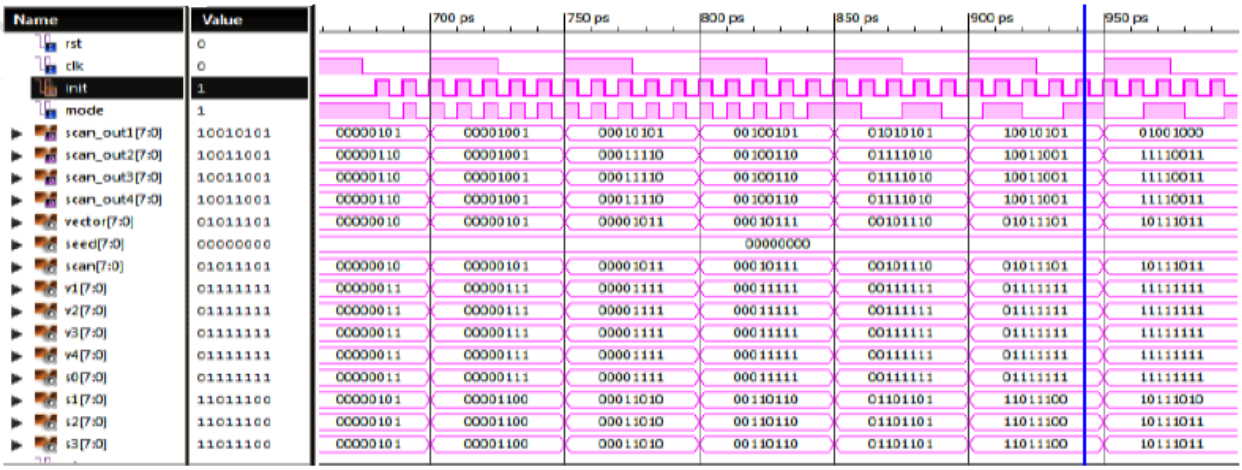

(c)

Figure 4. Waveforms of (a) LFSR (b) Reconfigurable Johnson counter (C) Multiple Single Input Change.

Table 1: Total and Peak power Reduction of CUTs

CUT	Total Power µW		Peak Power µW	
	MSIC	LFSR	MSIC	LFSR
C2670	19.9	38.55	312.4	433.1
C3540	46.6	81.44	755.5	918.3
C5315	55.1	110	821.8	1157
C6288	274.8	366.2	1994	2363
C7552	69.6	137	1012	1502

VI. CONCLUSION

This paper has proposed a low-power test pattern generation method that could be easily implemented by hardware. It also developed a theory to express a sequence generated by linear sequential architectures, and extracted a class of SIC sequences named MSIC. Analysis results showed that an MSIC sequence had the favorable features of uniform distribution, low input transition density, and low dependency relationship between the test length and the TPG's initial states. Combined with the proposed reconfigurable Johnson counter or scalable SIC

counter, the MSIC-TPG can be easily implemented, and is flexible to test-per-clock schemes and test-per-scan schemes. For a test-per-clock scheme, the MSIC-TPG applies SIC sequences to the CUT with the SRAM-like grid. For a test-per scan scheme, the MSIC-TPG converts an SIC vector to low transition vectors for all scan chains. Experimental results and analysis results demonstrate that the MSIC-TPG is scalable to scan length, and has negligible impact on the test overhead.

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