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SFCL with 5 – Level Inverter Using Four Types of HVDC Circuit Breakers

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ABSTRACT

In this paper, an application of superconducting fault current limiter (SFCL) is proposed to limit the fault current that occurs in power system, SFCL is a device that uses superconductors to instantaneously limit or reduce unanticipated electrical surges that may occur on utility distribution and transmission networks. In this paper we are increasing the levels of inverter. If we increase the level then the efficiency will be improved and also accuracy will be improved. One good solution is, combining the fault current limiting technologies with DC breaking topologies. The application of resistive Superconducting Fault Current Limiter (SFCL) on various types of HVDCCB and can estimate the effects of combining fault current limiters on conventional DC breakers. the simulation work done for resistive SFCL and added to the DC breakers and verify its interruption characteristics and distributed energy across HVDC CB. The major advantage is that the output waveform is more close to sinusoidal and harmonics can be reduced if higher the number of the level, approximately sin wave. From the results of simulation work, maximum fault current, interruption time and dissipated energy stress on the HVDC CB could be decreased by applying SFCL. By using the simulation results we can analyze the proposed method.

Keywords : DC Fault current Interruption, HVDC Fault, HVDC Circuit Breaker, 5-level inverter, MTDC, Resistive Superconducting Fault Current Limiter.

I. INTRODUCTION

The utilization of SFCL in power system provide most effective way to limit the fault current and results in considerable saving from not having to utilize high capacity circuit breakers. With Superconducting fault current limiters (SFCLs) utilize superconducting materials to limit the current directly or to supply a DC bias current that affects the level of magnetization of a saturable iron core. Recently we can achieve commercial application of the advance Multi Terminal HVDC (MTDC) networks, typically considered an optimum solution for renewable energy transmission and power grid inter-connection, the reliability of HVDC systems are more [1], [2]. Four types of DC breakers and SFCL were modelled, and fault current interruption characteristics were compared to determine the HVDC CBs type most suitable for the application of SFCL considering the current interruption capability and reduction of total dissipated energy during DC fault.

Conventional HVDC systems can be sufficiently protected by mechanical circuit breakers located on the AC side [3]; however, a selective coordination protection scheme that isolates faulted lines in MTDC to prevent the blackout of the entire grid system [4]. HVDC circuit breakers (HVDC CB) are widely considered a key technology in the implementation of the MTDC system [5].

The common three topologies for multilevel inverters are as follows:

1) Diode clamped (neutral clamped),
2) Capacitor clamped
3) Cascaded H-bridge inverter.

A multilevel inverter is power conversion device that produces an output voltage in the needed levels by using DC voltage sources applied to input [3]. It employs the capacitors connected in series to separate the DC bus voltage in different levels. This structure is

similar to the structure of the diode-clamped multilevel inverter, but it uses the capacitors instead of the diodes to clamp the voltage levels. The 5- level diode clamped multilevel inverter uses switches, diodes; a single capacitor is used, so output voltage is half of the input DC.

This paper focuses on a factor for resistive type SFCL, which is useful to improve the reliability of the system, with the transient stability study based on the equal area criterion, the performances of the proposed SFCL to reduce the level of fault currents. Some advantages can be obtained using multilevel inverter as follows: the output voltages and input currents with low THD, the reduced switching losses due to lower switching frequency, good electromagnetic compatibility owing to lower, high voltage capability due to lower voltage stress on switches.

The fault current interruption can be easily achieved by zero-current crossing. Where in AC circuit breakers can interrupt a fault current in natural zero current, artificial current zero should be implemented for DC breakers to enable fault current interruption. To achieve the zero-crossing condition of DC fault current, a forced current reduction method should be used. Various types of HVDC CB are summarized in [6], some of which have revealed prototypes and successful test results. Existing DC current breaking topologies focusing solely on methods to achieve artificial current zero should be somewhat achieved [7]. One feasible solution is fault current limiting technologies with DC breaking topologies.

The Resistive SFCL acknowledged as an effective solution to effectively limit fault current levels by absorbing electrical and thermal energy stresses during fault [8]. So, the combined application of SFCL and HVDC CB could be an alternative solution capable of decreasing the dissipated fault energy and improving the performance of HVDC CBs. In order to estimate the performance of combined-application of SFCL on HVDC CBs, simulation studies were performed

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Applications of multilevel inverter

- Static var compensation
- Variable speed motor drives
- High voltage system interconnections
- High voltage DC and AC transmission lines

MODELLING OF TEST-BED:

We are analyze the impact of SFCL on various types of HVDC CBs, a test-bed model was designed as shown in Fig. 1. The simple, symmetrical, monopole, point-to-point, 2-level, half-bridge HVDC system was utilized to get the interruption performance of the DC fault current in detail.

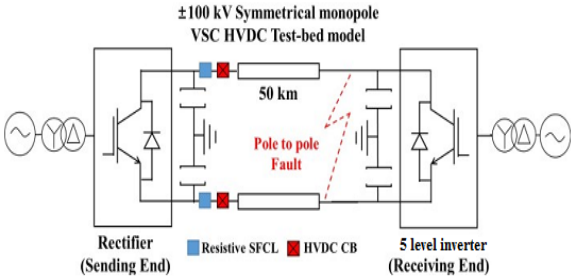


Figure 1. 2-level point-to-point HVDC test-bed model

TABLE -1. SPECIFICATIONS OF THE HVDC LINK AND SFCL

PARAMETER	VALUE
HVDC LINK	
Rated Voltage	+/- 100 KV
Nominal current	1 KA
Nominal power flow	100 MW
Transmission line length	50 KM
SFCL	
Rating	100 KV DC, 2KA
Max quenching Resistance (R_m)	10Ω
Transition time (t)	2ms

Resistive Superconducting Fault Current Limiter

According to the resistive SFCL, which is depend upon the quenching phenomena of superconductors have been developed and installed in medium- and high-voltage systems [10].

Therefore the theoretical analysis of a resistive SFCL [8], the quenching phenomena of SFCL can be expressed as:

$$\begin{Bmatrix} R_{max} = 0 & (t < t_{quenching}) \\ R_m\left(1 - exp\left(-t/T_{SC}\right)\right) & (t_{quenching} < t) \end{Bmatrix} \quad (1)$$

Where, R_m is the maximum quenching resistance and T_{sc} is the time constant for the transition to the quenching state.

The maximum quenching resistance R_m is 10 Ω. Until now, there is no practical application of DC SFCL. Therefore, to determine the transition time, time from zero resistance to maximum quench resistance of resistive SFCL, the transition time of AC SFCL was referred. It should be determined within 1/2 cycle, and therefore the transition time of designed SFCL was assumed to 2 ms. Therefore, in order to get nearly 10 ohms of R_q (quenching resistance) within 2 ms, the value of T_{sc} was find to 0.25 ms. The quenching characteristics of the designed SFCL based on (1) are shown in Fig. 2.

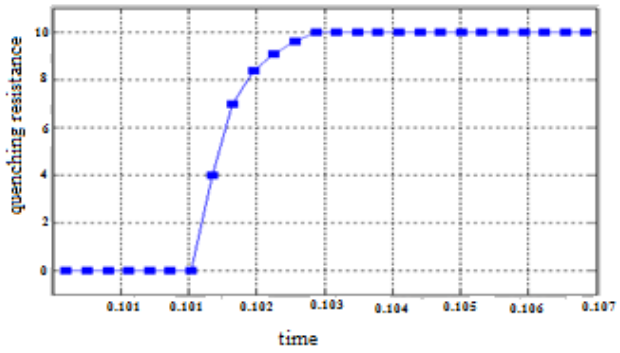


Figure 2. Resistive SFCL characteristics

Arc Modeling

According to the HVDC CB topologies which are classified as mechanical CB (MCB), passive resonance CB (PRCB), inverse current injection CB (I-CB) and Hybrid DC CB (HDCCB) [7]. In which the arc type such as mechanical, passive resonance DC CB, the implementation of arc dynamics is a major concern in the design for an accurate simulation model. The black-box arc model, which represents the arc dynamics by calculating the differential equation of the arc conductance, was designed.

In our simulation model, the modified Mayr black-box arc model was used for MCB, which assumes arc conductance, g, arc cooling power, $P_c(g)$, and arc time constant, τ, as shown.

$$\frac{1}{g}\frac{dg}{dt} = \frac{dlng}{dt} = \frac{1}{\tau(g)}\left(\frac{ui}{P_c(g)} - 1\right) \qquad (2)$$

The advantage of the modified Mayr arc model is able to determine the breaking capability of MCB by controlling $P_c(g)$. The following equations and parameters in Table I were used to determine the $P_c(g)$ and τ:

$$P_c(g) = P.P_0.g^a \qquad (3)$$

$$\tau(g) = \tau_0.g^b \qquad (4)$$

While various black-box arc models already exist, they only consider the continuous model environment. Due to the complicated nature of the system, a discrete model is required to accomplish an efficient simulation. To implement the continuous black-box arc model into in discrete model, (2) was transformed into integral form as (5) and the simulation model was designed as shown in Fig. 3.

$$g = \int_0^t \frac{1}{\tau}\left(\frac{i^2}{P_c(g)} - g\right) dt \qquad (5)$$

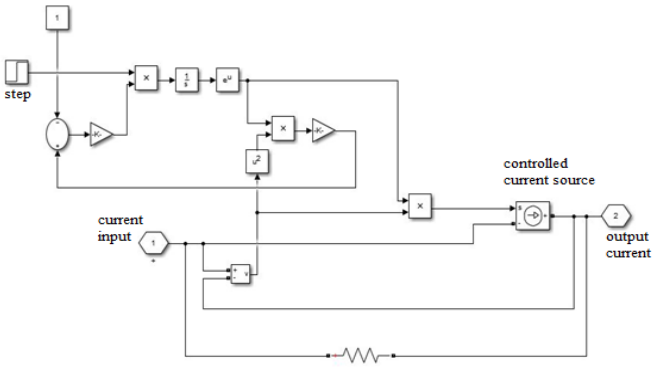


Figure 3. The modified Mayr black-box arc model designed using Matlab/ Simulink for discrete simulation environment

Table 2. Parameters of Black-Box Arc Model

Parameter	value
Cooling power P_0	0.393MW
Blow pressure P	70bar
a	0.25
T_0	15µsec
b	0.5

Modelling Of HVDC CBs

The concepts of HVDC CB are classified in CIGRE WG. B4.52 according to the method to achieve artificial current zero to interrupt fault current [15]. The simulation models of HVDC CBs in our simulation were designed as follows;

Mechanical CB (MCB): In MCB the DC current is reduced by increasing the arc voltage to higher value than the system voltage. By utilizing the black-box arc model, the simulation model of MCB was designed as shown in Fig. 4(a). Here assumed the delay time as 10ms for practical approach of simulation.

MCB

Figure 4. HVDC CB models: the (a) Mechanical CB (MCB)

Passive resonance CB (PRCB):

To dissipate the energy stress across MCB, the secondary path with a series L-C circuit is added as shown in Fig. 5(b).

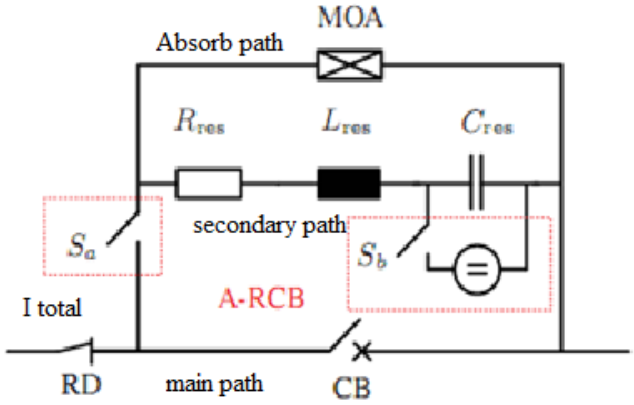


Figure 5. HVDC CB models: (b) Passive resonance CB (PRCB),

When the fault occurred at 0.1 sec, MCB opens with 10 ms of delay considering opening delay, and then an arc forms across the contacts with increasing arc impedance. The DC current begins to commutate and resonate in the secondary path after the arc impedance exceeds the L-C impedance. When a DC current of the primary path meets zero crossing, a current through the MCB can be interrupted by the extinction of the arc. An additional parallel surge arrester (SA) circuit is supplemented to prevent voltage stress across the PRCB during arc extinction.

Inverse Current Injection CB (I-CB):

However, the pre-charged capacitor via an additional DC power source injects an inverse current into the primary path after the current commutates to secondary path as shown in Fig. 4(c). This can reduce the interruption and oscillation time when compared to that of PRCB. Before a fault, a charging switch (ACB1) and an auxiliary switch (ACB2) maintains closed state. Thereby capacitor can be charged by DC source. When a fault occurs, after an 10 ms delay, MCB and ACB1 contacts open simultaneously. Then the high discharging inverse current from capacitor is supplied to main path. The fault current is rapidly decreased and transient recovery voltage appears between the terminals of I-CB. When the voltage exceeds to the knee voltage of SA, it is triggered to restrain the voltage rise, and it absorbs the fault energy. Therefore, remaining fault energy is exclusively absorbed by SA. If the current reaches to zero, a residual circuit breaker (RCB) opens and the current interruption is complete.

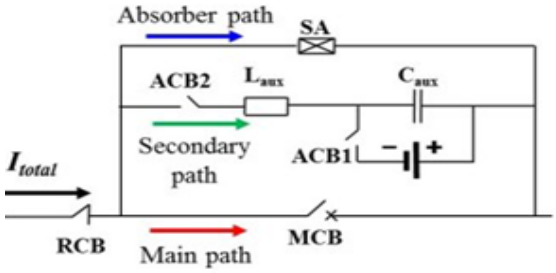


Figure 6. HVDC CB models: (c) Inverse current injection CB (I-CB)

Hybrid DC CB (HDCCB):

According to the scheme which is widely used as the optimal concept for interrupting DC fault current, was designed as illustrated in Fig. 4(d). The delay times of IGBT was assumed as Δt IGBT = 6 μs in simulation.

When a DC fault occurs, the auxiliary DC breakers (ADCB) and fast disconnector are opened sequentially, then the current starts to commutate from the main path to secondary path. After commutation, main DC circuit breakers (MDCB) in secondary path are opened, and total current is reduced because the current flows to the snubber circuit of MDCB until the parallel-connected SA trips. When the voltage across the HDCCB terminals exceed to knee voltage, the SA ignites and forces the DC fault current to zero by absorbing remaining fault energy. Finally, a RCB opens and isolates the DC fault.

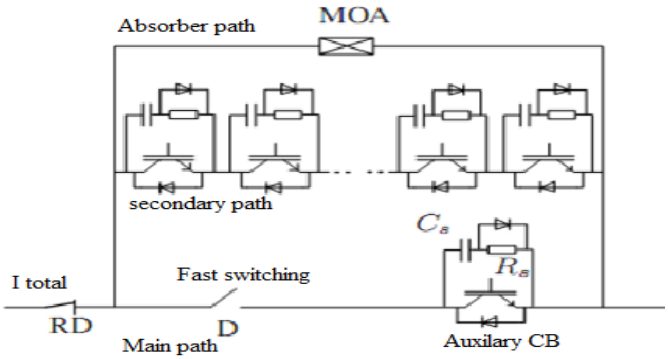


Figure 7. HVDC CB models: (d) Hybrid DC CB.

Modeling of 5 – Inverter

The single phase 5-level Cascaded Multilevel Inverter consists of simple two H-bridge modules, whose AC terminals are connected in series to obtain the output waveforms Fig.2. shows the power circuit for a five level inverter with two cascaded cells. Through different combinations of the four switches of each cell, the inverter can generate FIVE different voltage outputs, +2Vdc, +Vdc, 0, -Vdc, -2Vdc. The number of voltage

levels in a CHB inverter can be found from z = (2H+1) where H= is the number of H-Bridge cells per phase leg. The voltage level m is always an odd number for the CHB inverter. The total number of active switches (IGBT's) used in the CHB inverters can be calculated by Nsw = 3*2(z-1) =6(4) =24 switches (for three phase).where Nsw=number of switch [3],[6]. The resulting AC output voltage is synthesized by the addition of the voltages generated by different H-bridge cells. Each single phase H-bridge generates three voltage levels as +Vdc, 0, - Vdc by connecting the DC source to the AC output by different combinations of four switches, S11, S12, S13, and S14 as seen in Fig 1(c). The CHB-MLI that is shown in Fig. 2 utilizes two separate DC sources per phase and generates an output voltage with five levels. To obtain +Vdc, S11 and S14 switches are turned on, whereas -Vdc level can be obtained by turning on the S12 and S13. The output voltage will be zero by turning on S11 and S12 switches or S13 and S14 switches. If n is assumed as the number of modules connected in series, m is the number of output levels in each phase as given by z=2n+1. The switching states of a CHB-MLI (sw) can be determined by using Eq. sw= 3z [3],[7]. Considering the simplicity of the circuit and advantages, Cascaded H-bridge topology is chosen for the presented work. Table I shows the switching strategies used for single phase five level CHB-MLI

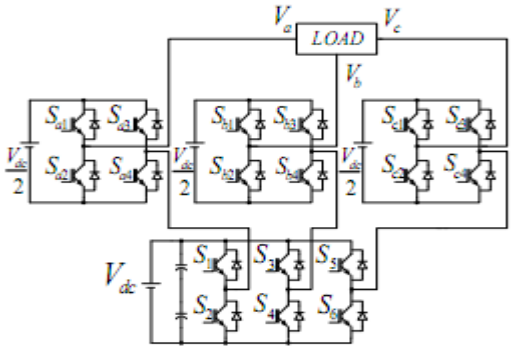


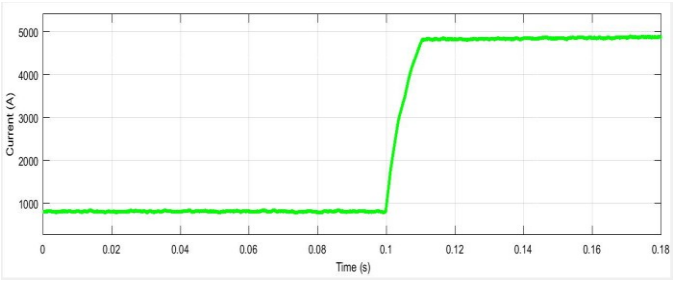
Figure 8. Topology of a 5-level three-phase cascaded hybrid multilevel inverter.

SIMULATION ANALYSIS AND DISCUSSION

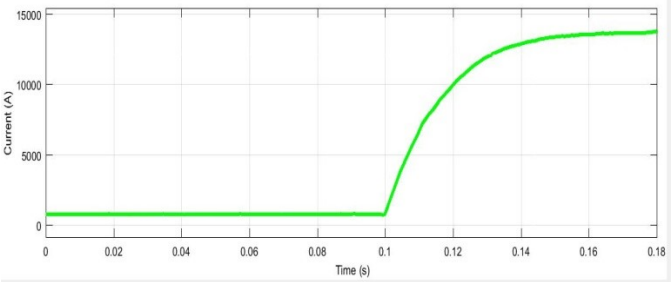
Transient fault simulations had done to analyze the effects of SFCL on various HVDC CB types. Each type of HVDC CB, both with and without SFCLs, was applied at the sending end of the test-bed. A pole-to-pole fault, which considered a severe fault in HVDC systems, was generated on the receiving end at 0.1 sec. The prospective maximum fault current without any protection devices was 14.75 kA in the designed test-bed. The rising rate of the fault current di/dt during early 10 ms was measured as 589 A/ms. Therefore, considering high rising rate of the fault current, fast interruption should be achieved.

Case 1: Mechanical CB (MCB)

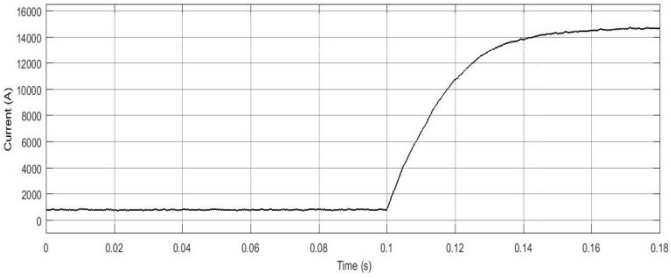
As per fig.5 shows the DC fault interruption performance of the MCB. A maximum prospective fault current was measured as 14.7 kA. Without SFCL, fault current was reduced from 14.75 kA to 13.75 kA. Arc extinction could not be achieved due to low cooling power, Pc(g), and a small current reduction was measured due to the generation of arc resistance. In the case of 'with SFCL', a 67 % current reduction from 14.75 kA to 4.8 kA was observed, but fault interruption was still not achieved.



(a) With MCB and SFCL



(b) With MCB and without SFCL



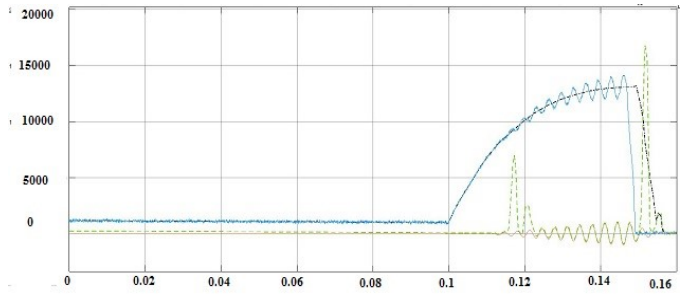
(c) Without MCB and without SFCL

Figure 9. Interruption characteristics of MCB when SFCL was applied

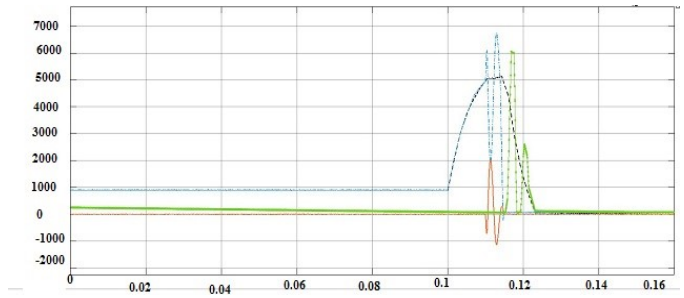
To interrupt the DC fault current utilizing the MCB only, the arc cooling power, Pc(g), should be increased; however, it is difficult to fulfill the insulation requirement, particularly in high-voltage application. In addition, DC fault interruption was not achieved in spite of the application of SFCL. Therefore, it was deduced that DC fault interruption via the MCB was not an appropriate solution to clear DC fault.

Case 2: Passive Resonance CB (PRCB)

According to the fig. 6 shows the DC fault interruption performance of the PRCB. Without SFCL, the maximum fault current intensity (Itotal) was measured at 13.2 kA, and the maximum current in the main path reached 27.5 kA owing to resonant oscillation. The total interruption time was 57 ms. In this regard, considering the fast di/dt of the DC fault current, using PRCB alone was not an appropriate solution to clear fault within a short time span.



(a) Without SFCL



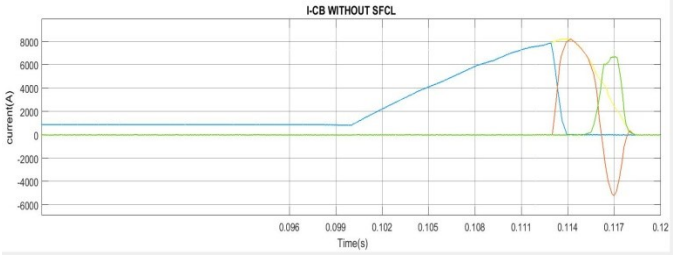
(b) With SFCL

Figure 10. Interruption characteristics of PRCB when SFCL was applied

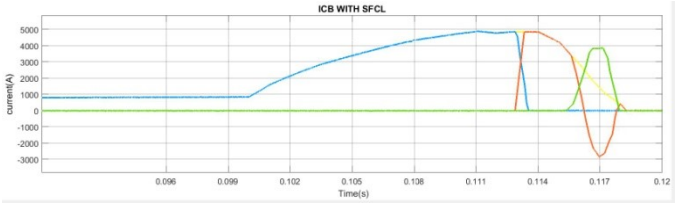
After applying SFCL, the maximum Itotal was 5 kA; 60 % of the fault current was decreased. As the impedance of the main path increased via SFCL quenching, the time constant L/R of the test-bed declined, enabling the reduction of total oscillation time. Thus, fast interruption was achieved within 24ms with less oscillation, and if faster interruption time is required, increasing the quench resistance could be a solution by reducing the time constant of the secondary path.

Case 3: Inverse current injection CB (I-CB)

According to the fig. 7 which is presents the interruption characteristics of the inverse current injection CB (I-CB). Without SFCL, the maximum Itotal was 8.2 kA, which is lower than that of the PRCB. Unlike the interruption characteristics of the PRCB, no oscillation was observed in the I-CB, because discharge of the pre-charged capacitor supplies large inverse current over a short duration.



(a) Without SFCL



(b) With SFCL

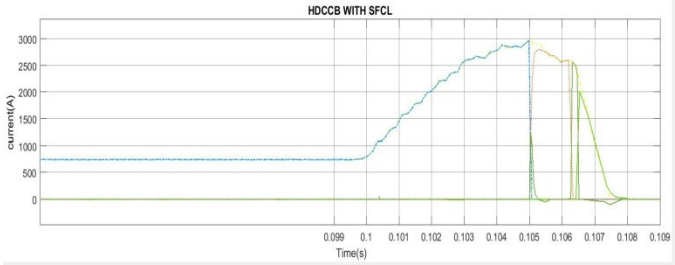
Figure 11. Interruption characteristics of the I-CB when SFCL was applied.

Therefore, a fast I-CB interruption time, measured at 18 ms, was achieved as compared to that of PRCB. In the case of 'with SFCL', the maximum Itotal was 4.9 kA. Interruption time was equal to the case without SFCL. There was no passive oscillation with the inverse current injection over a short duration; therefore, unlike PRCB, the L/R time constant on the secondary path did not influence on the interruption characteristics of the I-CB.

Case 4: Hybrid DC CB (HDCCB)

The primary characteristic of the HDCCB is that it achieves fast interruption due to the response time of a semi-conductor. The maximum I_{total} found was 3.5 kA, and the interruption time was 7.8 ms, which is the lowest value depicted in Fig. 8. By applying SFCL, the maximum I_{total} = 2.9 kA, which is the lowest value with a 16.40 % reduction ratio and estimated interruption time of 7.55ms. Regarding the fast response of HDCCB, the circuit interruption has been progressed within the transition time of SFCL. Therefore, we determined that the effect of SFCL on a HDCCB exhibits insufficient performance as compared to other concepts.

(a) Without SFCL



(b) With SFCL

Figure 12. Interruption characteristics of the HDCCB when SFCL was applied.

Analysis of Energy Dissipation

Energy dissipation is the primary design parameter used to determine the breaking capability of CB. In this study, dissipated energies on SFCL and HVDC CBs were calculated. From (6), the measured current, voltage and total interruption time determine the dissipated energy across the HVDC CB:

$$E_{dissipated} = \int_{t.fault}^{t.interruption} Pdt = \int_{t.fault}^{t.interruption} V_{cb} I dt \quad (6)$$

where the Vcb is the voltage across HVDC CB during a fault interruption.

The dissipated energy across the CB both with and without application of the SFCL have shown in figure. 9. Without the SFCL, the highest energy dissipation was observed in the MCB due to interruption failure, and the lowest energy dissipation was observed in the HDCCB. By applying the SFCL, energy reduction was observed from all types of HVDC CB. Among these, PRCB with SFCL showed the best performance with an 83.4 % energy reduction; however, the SFCL shows less effect on the HDCCB, which is considered the best concept among the HVDC CBs.

TABLE 3

Dissipated energy across HVDC CB in MJ

	Without SFCL	With SFCL
MCB	12.5	4.9
P-RCB	11.8	1.97
I-CB	4	1.8
HDCCB	0.48	0.36

Figure 13. Comparison of dissipated energy across the HVDC CB during a fault

To determine the optimum topology for HVDC CBs with SFCL, comparative analyses were conducted considering the interruption performance and cost, as shown in Table II. The best performance improvement was achieved via the PRCB. I-CB also resulted in improvement, though still less than that of the PRCB.

Maintenance of the I-CB is complicated due to the external power source needed to charge the auxiliary capacitor. The HDCCB, which showed the highest performance of all, has a disadvantage in its high development cost. In addition, a few HDCCB performance improvements were observed if the SFCL was applied. Exclusive use of the HDCCB was the optimum solution to achieve DC current interruption through the HDCCB, considering cost effectiveness. PRCB, which is considered the least efficient HVDC CB concept, has shown the noticeable enhancement by applying SFCL considering the fault interruption capability and development cost.

Table 4 Impact Of Resistive SFCL On Four Types Of HVDC CB

	MCB	PRCB	I-CB	HDCCB
Current reduction	67%	60%	40%	16.4%
Interruption time	NO interruption	33ms	0.1ms	0.25ms
Reduced $E_{fault\,(\%)}$	60.5	83.4	61.2	37.4

THD Analysis

Total harmonic distortion, or THD, is the summation of all harmonic components of the voltage or current waveform compared against the fundamental component of the voltage or current wave. THD calculations can be obtained from the SIMULINK. The switching pattern that is used in this project for all of the multilevel inverters is Sinusoidal PWM technique. In this method the switching angles for switches should be calculated in such a way that the dominant harmonics are eliminated (minimized). For a 5-level inverter the 5th harmonic will be eliminated.

$$\%THD=((V2^2+V3^2+V4^2+.....+Vn^2)^{1/2})V1$$

Where, V1= Fundamental Voltage magnitude

V2 = Magnitude of 2nd Harmonic

V3 = Magnitude of 3rd Harmonic .

Vn = Magnitude of nth Harmonic

The formula above shows the calculation for THD on a voltage signal. The end result is a percentage comparing the harmonic components to the fundamental component of a signal. The higher the percentage, the

more distortion that is present on the mains signal.from simulation analysis the voltage THD vary from 52.04% to26.6%.

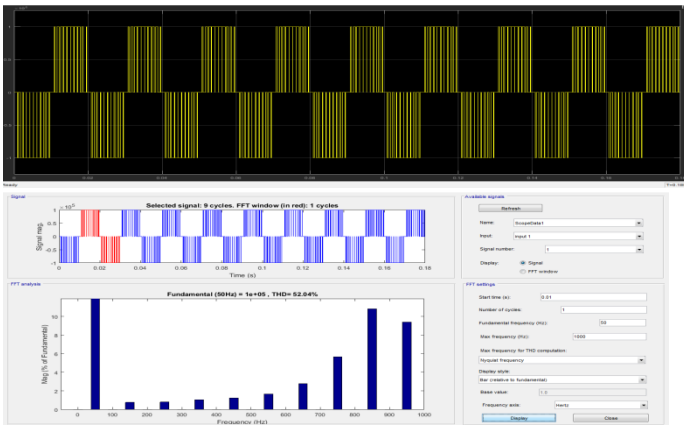


Fig.14.Voltage waveform and % THD for the conventional 3-Level Inverter

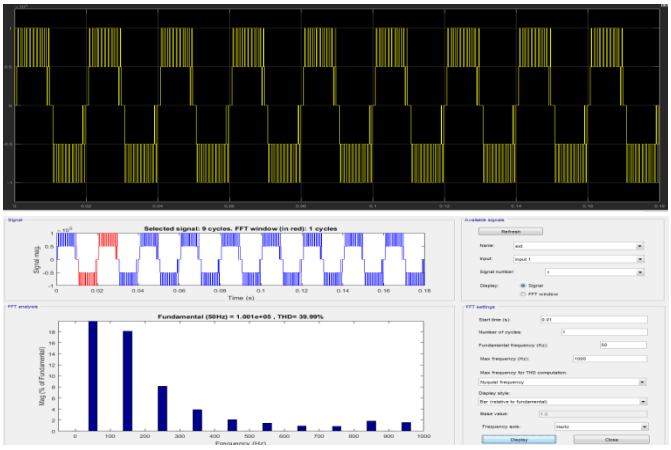


Fig.15. Voltage waveform and % THD for the 5 level Inverter

II. CONCLUSION

This paper deals with the impact of SFCL on various types of HVDC CB. The resistive SFCL considers quenching characteristics and concepts of HVDC CB models including the black-box arc model, and a simple HVDC were designed. A severe DC pole-to-pole fault was imposed to analyze the interruption performance. If we increase the levels then the output waveform is more close to sinusoidal. Higher the number of the levels, more approximate is the waveform to sin wave. From the simulation results, the maximum fault current, interruption time, and dissipated energy stress on an HVDC CB could be decreased by applying an SFCL. Noticeable enhancement of the fault interruption capability was exhibited by PRCB, which showed the longest interruption time and highest maximum fault current without SFCL. When the SFCL was applied, the L/R time constant of the secondary path was decreased, and therefore fast interruption with less oscillation was observed. Consequently, SFCL installation with PRCB could be a viable, reliable, and cost-effective option to enhance DC fault current interruption capability. Simulating the 5 level inverter the THD value of voltage decreases from 52.04% to 26.6% results good sinusoidal wave form.

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