FPGA Based Multilevel Inverter with Reduce Number of Switches for Photovoltaic System

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ABSTRACT

This work proposes a FPGA Based Multilevel Inverter with Reduce Number of Switches for Photovoltaic System. Three sorts of reference flags that are indistinguishable to each other with a counterbalance that is equal to the amplitude of the triangular transporter were utilized to create the PWM signals. The inverter can deliver seven levels of yield voltage levels (Vdc, 2Vdc/3, Vdc/3, 0, - Vdc, - 2Vdc/3, - Vdc/3) from the dc supply voltage. An advanced PI current control calculation was executed in a Xilinx XC3S250E FPGA to keep the current infused into the framework as sinusoidal. The proposed framework was composed and checked through recreation and executed in a model.

Keywords : Grid Connected, Modulation index, Multi level inverter, Photo Voltaic (PV) system, Pulse Width modulation (PWM), Total harmonic distortion (THD).

I. INTRODUCTION

The regularly expanding vitality utilization, petroleum derivatives, taking off expenses and modest nature, and intensifying condition have made a blasting enthusiasm for sustainable power source age frameworks, one of which is photovoltaic. Such a framework produces power by changing over the sun's vitality straightforwardly into power. Vitality created by photovoltaic framework and can be conveyed to control framework arranges through network associated inverters.

A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10 kW [1]. Types of single-phase grid-connected inverters have been investigated [2]. A common topology of this inverter is full bridge three-level. The three level inverter should the satisfy specifications through its very high switching, but it may be unfortunately increase switching losses, acoustic noise, and level of interference to other equipment. By improving its output waveform reduces its harmonic content and hence, also the size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter's switching operation [3].

Multilevel inverters are guaranteed that they have nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact [3], [4].

Various topologies for multilevel inverters have been pro- posed over the years. Common ones are diode-clamped [5]– [7], flying capacitor or multi cell, cascaded H-bridge, and modified H-bridge multilevel.

This paper recounts the development of a novel modified H-bridge single-phase multilevel inverter that has two diode embedded bidirectional switches and a novel pulse width- modulated (PWM) technique. The designed topology was applied to a grid-connected photovoltaic system with considerations for a maximum-power-point tracker (MPPT) and a current-control algorithm.

A multilevel power converter structure has been introduced as an alternative in high power and medium power situations. A multilevel converter not only assures high power ratings, but also enables the ease of

usage for renewable energy sources such as photovoltaic, fuel cells and wind, can be easily interfaced to a multilevel converter system for a high power application.

Figure 1. Proposed single phase seven level grid connected PV inverter

The term multilevel begun with the three level, subsequently, several multilevel converter topologies has been developed over the years. However, the elementary concept of a multilevel converter to achieve higher power is to use a series power semiconductor switches with several lower voltage DC sources to perform the power conversion by synthesizing a staircase voltage waveform. Batteries, Capacitors, and renewable energy voltage sources can be used as the multiple DC sources in order to achieve high voltage at the output; however, the calculated rated voltage of the power semiconductor switches depends only upon the rating of the DC voltage sources to which they are connected.

A multilevel converter gives more advantages over a conventional three level inverter that uses high switching frequency pulse width modulation (PWM).

II. PROPOSED INVERTER

The circuit diagram for PV connected single phase seven level grid connected inverter shown in fig. 3.2. Photovoltaic arrays were connected to the inverter via a dc-dc boost converter. The power generated by the inverter is to be delivered to the power network, so the utility to grid, rather than a load, was used. The dc-dc boost converter was required because the PV arrays had a voltage that is lower than the grid voltage. High dc bus voltages make more importance to ensure that power flows from the PV arrays to the grid. A filtering inductance Lf was used to filter the current injected into the grid. Proper switching of the inverter can produce seven output-voltage lev- els (Vdc , 2Vdc /3, Vdc /3, 0, −Vdc , −2Vdc /3, −Vdc /3) from the dc supply voltage.

The proposed inverter's operation can be divided into seven switching states, they are shown in Fig. 2(a)to 2(g). Fig. 2(a), (d), and (g) shows a conventional inverter's operational states in sequence, while Fig. 2(b), (c), (e), and (f) shows additional states in the proposed inverter synthesizing one- and two-third levels of the dc-bus voltage. The required seven levels of output voltage were generated as follows.

1) Maximum positive output (Vdc): When S1 is ON state, connecting the load positive terminal to Vdc , and S4 is ON, con- necting the load negative terminal to ground. Remaining controlled switches are OFF; the voltage applied to the load terminals is Vdc . Fig. 2(a) shows the current paths that are active at this stage.

2) Two-third positive output (2Vdc /3): The bidirectional switch S5 is ON state, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. Remaining controlled switches are OFF; the voltage applied to the load terminals is 2Vdc /3. Fig. 2(b) shows the current paths that are active at this stage.

3) One-third positive output (Vdc /3): The bidirectional switch S6 is ON state, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. Remaining controlled switches are OFF; the voltage applied to the load terminals is Vdc /3. Fig. 2(c) shows the current paths that are active at this stage.

4) Zero output: This level can be produced by two switching combinations; switches S3 and S4 are ON, or S1 and S2 are ON state, and remaining controlled switches are OFF; terminal ab is a short circuit level and the voltage applied to the load terminals is zero. Fig. 2(d) shows the current paths that are active at this stage.

5) One-third negative output (−Vdc /3): The bidirectional switch S5 is ON state, connecting the load positive terminal, and S2 is ON, connecting the load negative terminal to Vdc . Remaining switches are OFF; the voltage applied to the load terminals is −Vdc /3. Fig. 2(e) shows the current paths that are active at this stage.

6) Two-third negative output (−2Vdc /3): The

bidirectional switch S6 is ON, connecting the load in positive terminal, and S2 is ON, connecting the load negative terminal to ground. Remaining controlled switches are OFF; the voltage applied to the load terminals is −2Vdc /3. Fig. 2(f) shows the current paths that are active at this stage.
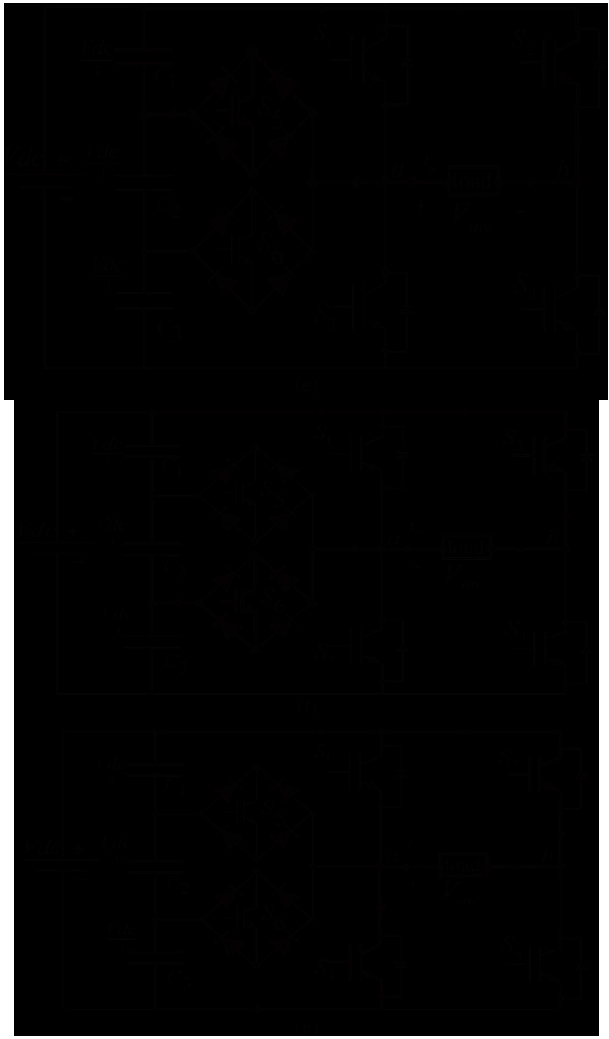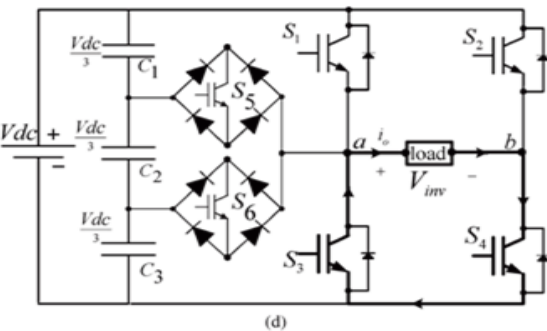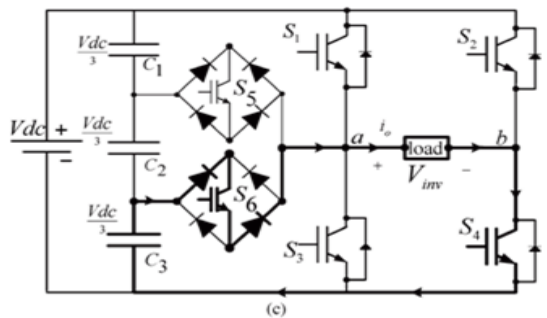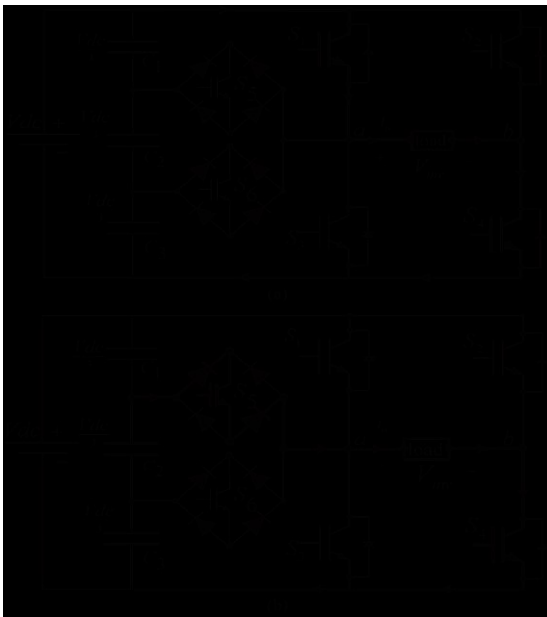
7) Maximum negative output (−Vdc): When S2 is ON state, connecting the load negative terminal to Vdc , and S3 is ON, connecting the load positive terminal to ground. Remaining controlled switches are OFF; the voltage applied to the load terminals is – Vdc. Fig. 2(g) shows the current paths that are active at this stage.

Table I shows the switching combinations that gen- erated the seven output-voltage levels (0, −Vdc , −2Vdc /3,−Vdc /3, Vdc , 2Vdc /3, Vdc /3).

TABLE I. OUTPUT VOLTAGE ACCORDING TO T HE SWITCHES' ON–OFF CONDITION

III. PWM TECHNIQUES

A novel PWM modulation technique was introduced to generate the PWM switching signals. Three reference signals (Vref1, Vref2, and Vref3) were compared with a carrier signal (Vcarrier). The corresponding reference signals had the same frequency, amplitude and were in phase with an offset value that was equivalent to the

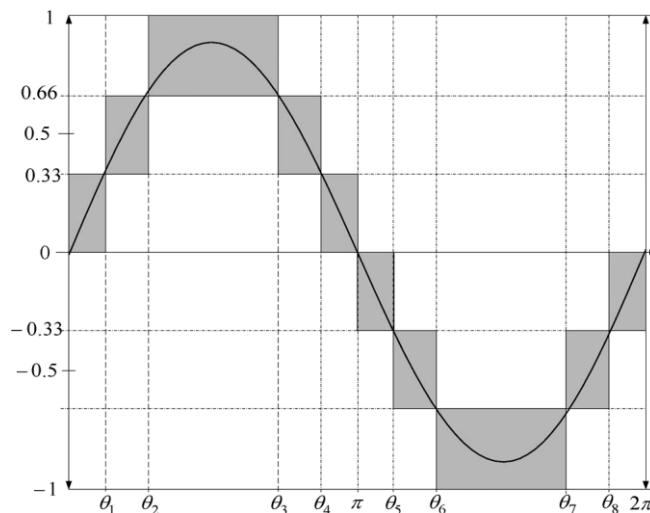amplitude of the carrier signal. The reference signals were each compared with the carrier signal. When the value of Vref1 had exceeded the peak amplitude of Vcarrier, Vref2 is made the comparison with Vcarrier until it had exceeded the peak amplitude of Vcarrier. Then, onward, Vref3 would take charge and would be compared with Vcarrier until it makes the value which is reached to zero. Once Vref3 had reached zero, the value of Vref2 would be compared until it reached zero. After that moment Vref1 would be compared with Vcarrier. Fig. 3 shows the result of switching pattern. The switches S1, S3, S5, and S6 would be switching at the rate of the carrier signal frequency, whereas S2 and S4 would operate at a frequency that was equivalent to the fundamental frequency.

For one cycle of the fundamental frequency, the proposed inverter operated through six modes. Fig. 4 shows the per- unit output-voltage signal for one cycle. The six modes are described as follows:

> Mode 1 : $0 < \omega t < \theta 1$ and $\theta 4 < \omega t < \pi$
> Mode 2 : $\theta 1 < \omega t < \theta 2$ and $\theta 3 < \omega t < \theta 4$
> Mode 3 : $\theta 2 < \omega t < \theta 3$
> Mode 4 : $\pi < \omega t < \theta 5$ and $\theta 8 < \omega t < 2\pi$
> Mode 5 : $\theta 5 < \omega t < \theta 6$ and $\theta 7 < \omega t < \theta 8$
> Mode 6 : $\theta 6 < \omega t < \theta 7$.--------------------(1)
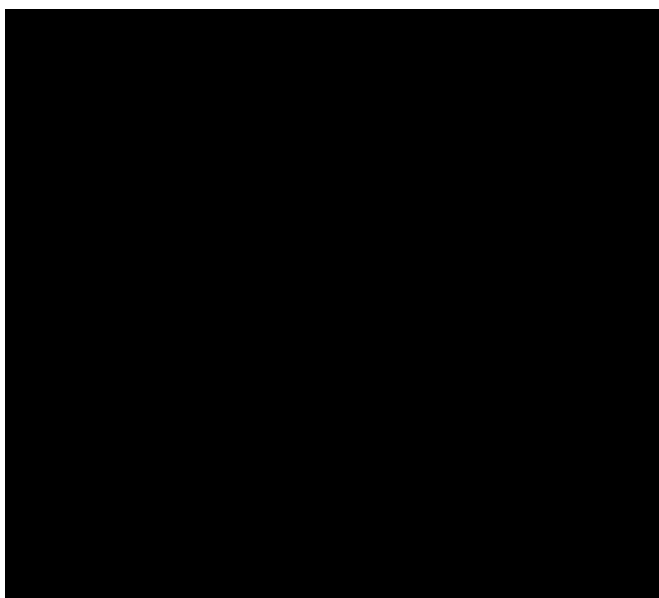
Figure 3. Switching pattern for the single-phase seven-level inverter.

Figure 4. Seven-level output voltage (Vab) and switching angles.

The phase angle of the device depends on the modulation index Ma. Theoretically the modulation index is

$$M_a = \frac{A_m}{A_C}$$ ------------- (2)

For single reference signal and dual carrier signal the modulation signal defined to be [6]

$$M_a = \frac{A_m}{2A_c}$$ ------------- (3)

The proposed inverter uses the three carrier signal so the modulation index is defined as

$$M_a = \frac{A_m}{3A_c}$$ -------------- (4)

Where Ac is the peak to peak value of the carrier signal and Am is the peak to peak value of the voltage reference signal Vref.

When the modulation intex more than 0.33 and less than 0.66. The phase angle displacement is given by

IV. IV. CONTROL SYSTEM

FPGA is Programmable Logic Device developed by one of the vital vendor of VLSI that is Xilinx, Inc. It comprises of millions of logic gates. From that some of them combined together to form a Configurable Logic Block (CLB). CLB simplifies higher-level circuit design. Netlist of gates that means Gates interconnections using software are defined through SRAM or ROM. Thus it makes the flexibility modification in the designed circuit

without altering the hardware part. When considering the Concurrent operation, it requires less hardware, easy and fast circuit modification, especially low cost for a complex circuitry and rapid prototyping make it as the most favorable choice for prototyping an ASIC.

The carrier wave is compared with the multiplied modulating signal which is derived from the look-up table. The corresponding data of the look up table are stored in the internal ROM unit. The external multiplicands and already stored data will determine the modulation index of the PWM. The data stored in the look-up table (ROM) consists of 60 data from the Red phase and another 60 data from the Blue phase. Most Part of Yellow phase is derived through addition of Red and Blue phases. Selector Unit and Multiplexer are used in the selection of required signal to the appropriate channel as to form a proper PWM output pattern at the output terminals.

The shifting of signal waveform is essential in order to vary the power factor of the system. The process is carried out by delay or advance the reset signal. The reset signal is fully connected to the entire module. A signal of positive triggering edge during positive and negative cycle is used as a reference by the reset signal. By producing the advancement and delay through reset signal by the external command will force the current in the main circuit to lead or lag the voltage supply.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

MATLAB SIMULINK simulated the proposed configuration before it was physically implemented in a prototype. The PWM switching patterns were generated by comparing three reference signals (Vref1 , Vref2 , and Vref3) against a triangu- lar carrier signal (see Fig. 6). Subsequently, the comparing process produced PWM switching signals for switches S1 –S6 , as Fig.5 and the output voltage of seven level inverter shown in fig.6

One leg of the inverter operated at a high switching rate that was equivalent to the frequency of the carrier signal, while the other leg operated at the rate of the fundamental frequency (i.e., 50 Hz). Switches S5   and S6   also operated at the rate of the carrier signal.
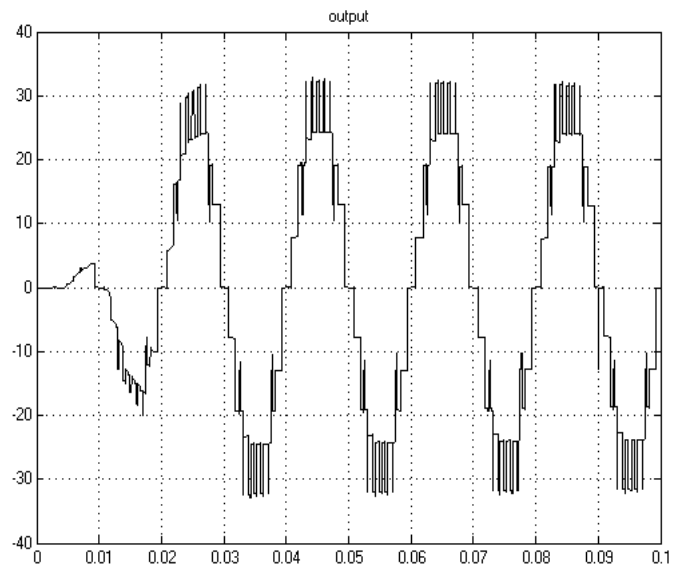

Figure 5. Simulation Output voltage of seven level inverter

B. EXPERIMENTAL RESULTS

The hardware output voltage for single phase seven level inverter shown in fig.7 and hardware photocopy shown in fig.8.
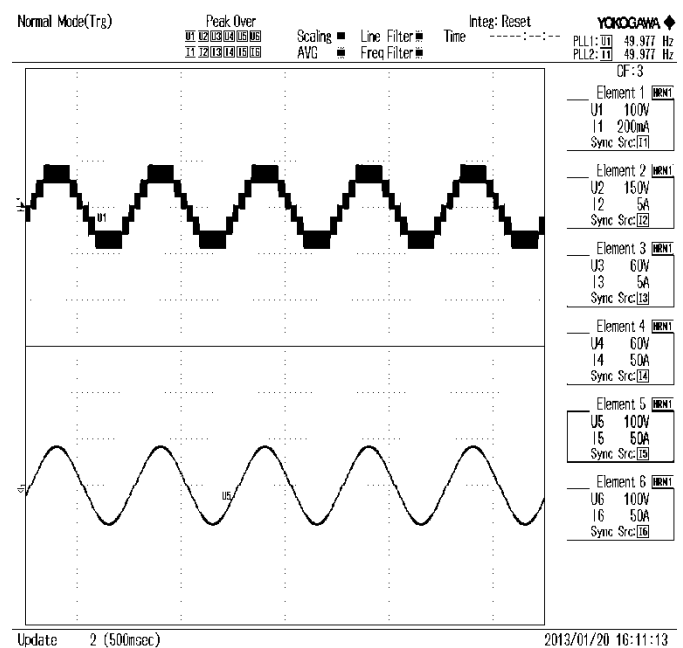

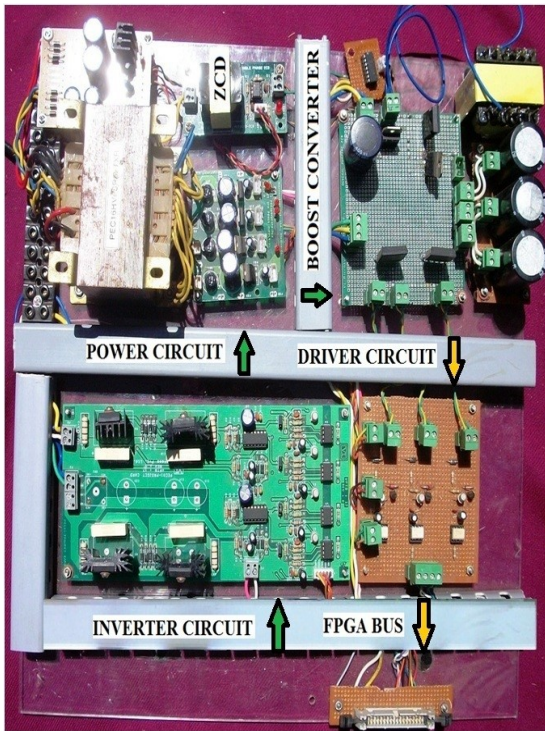**Figure 6.** Output voltage for single phase seven level inverter

Figure 7. Hardware Photocopy of proposed system.
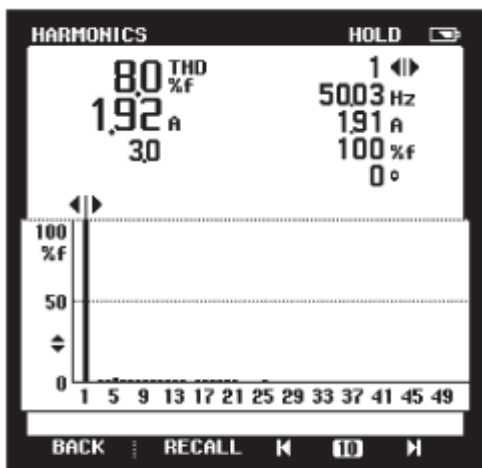
C. THD RESULT FOR MULTILEVEL INVERTER

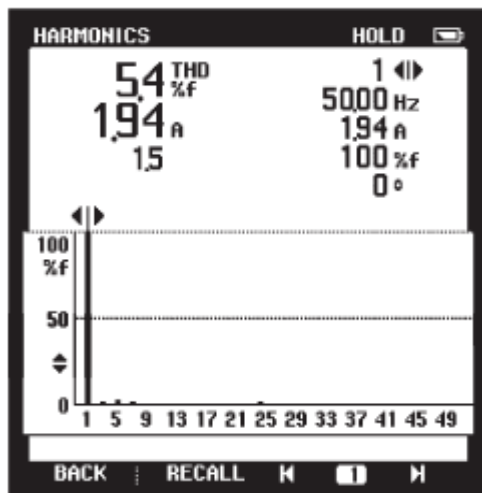**Figure 8.** THD results for 3-level inverter

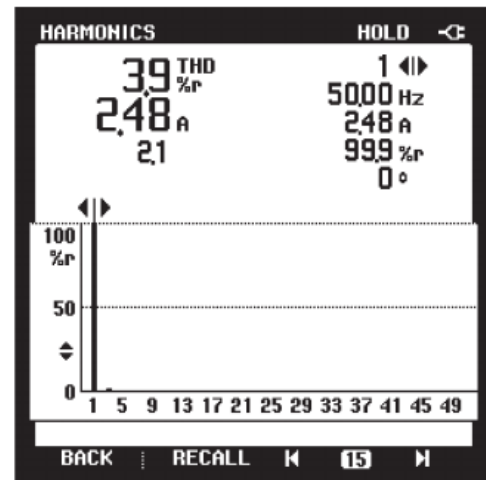**Figure 9.** THD results for 5-level inverter

Figure 10. THD results for proposed system

VI. VI.CONCLUSION

Using Xilinx FPGA to generate the PWM provides flexibility to modify the designed circuit without altering the hardware part. When Concurrent operation is used, it requires less hardware, easy and fast circuit modification, especially low cost for a complex circuitry and rapid prototyping make it as the most favorable choice for the PWM generation. From the analysis of simulation and experimental results it is confirmed that the harmonic distortion of the output current waveform of the inverter fed to the grid is within the stipulated limits laid down by the utility companies, the THD is less than five and three level inverter. All the above advantages have made the inverter configuration highly suitable for grid connected photovoltaic application (5kW).

VII. REFERENCES

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