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Decoupling of Fluctuating Power using Fuzzy Logic Controller for Single Phase Systems

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ABSTRACT

Single-phaseac/dc or dc/ac systems are innately subject to the symphonious aggravation that is caused by the well known doubled line frequency swell power. This issue can be facilitated through the establishment of bulky electrolytic capacitors in the dc link. An option approach is to utilize active power decoupling with the goal that the swell power can be redirected into other energystorage gadgets to pick up an enhanced framework execution..In perspective of this, this paper introduces a fuzzy logic controller to symmetrical half-connect circuit which uses the dc-interface capacitors to ingest the swell power, and the just extra segments are a couple of switches and a little filtering inductor. A plan case is displayed and the fuzzy logic controller circuit idea is likewise confirmed with recreation and trial comes about. It demonstrates that no less than ten times capacitance lessening can be accomplished with the proposed fuzzy logic controller active power decoupling technique, also, both the info current and output voltage of the converter can be all around directed notwithstanding when little dc-interface capacitors are utilized.

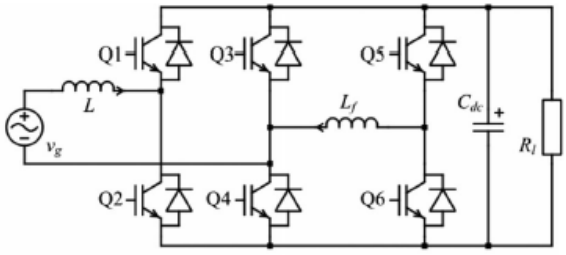
Keywords: Active Power Decoupling, Capacitance Reduction, Harmonic Compensation, Single-Phase Systems.

I. INTRODUCTION

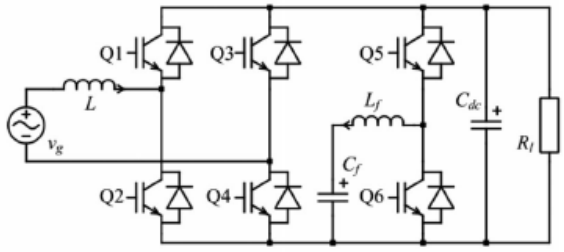
SINGLE-PHASE ac/dc or dc/ac power hardware frameworks have to great degree wide applications in private and mechanical control supplies or transformation frameworks. Case applications are front-end power factor correction (PFC) converters in buyer control supplies [1], on-board chargers for module crossover electric vehicles and 5-kW (or less) grid connected photovoltaic (PV) inverters for disseminated control age.A well-known issue with such frameworks is that their ac side immediate power contains a fluctuating segment that progressions at double the basic recurrence [2]. This fluctuating force is antagonistic to the framework execution since it might possibly cause mutilated information current of PFCs, overheating of batteries, and diminished most extreme power point following (MPPT) effectiveness of PV frameworks [3]. An extremely clear approach to alleviate its negative effect is to utilize cumbersome electrolytic capacitors in the dc connect with the goal that they can go about as cushions to the air conditioner side swell power. Nonetheless, those electrolytic capacitors are known to have high equivalent series resistance (ESR) and low swell current capacity, and their lifetime is likewise moderately short (a few thousand hours) when worried with the ostensible voltage and the swell current. Along these lines, they may cause inconveniences in a few applications where 20-or 25-year guarantee period is required, e.g., LED drivers and sun based inverters [3].

As of late, some active power decoupling strategies have been proposed to adapt to this issue, and the basic standard behind them is to present an additional dynamic circuit in the framework, with the goal that the swell power can be moved far from the dc connect and put away by different parts with extended lifetime, e.g., inductors and film capacitors, in a more proficient and powerful way. Fig. 1(a) demonstrates a dynamic technique which utilizes an inductor for swell energystorage [4], and the inductor current is controlled to be sinusoidal which is expert through the legitimate tweak of the additional third exchanging leg.

Despite the fact that inductors are dependable and powerful, they are by and large of low power thickness and high power misfortunes when utilized as energystorage components for principal parts, and along these lines, the execution change could be exceptionally constrained. In [3], the inductor is supplanted by a film capacitor and the swell power would then be able to be remunerated by controlling the voltage of the



(a)



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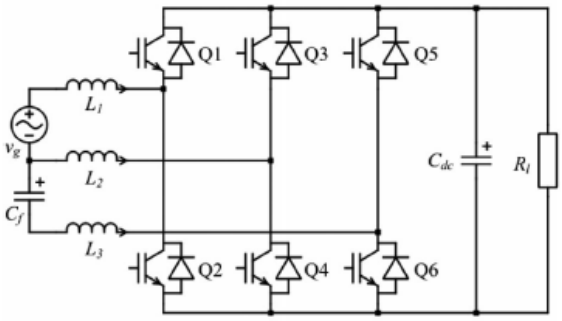


(c)

Figure 1. Typical circuit topologies for active power decoupling in a single-phase System.

Film capacitor to be amended sinusoidal as appeared in Figure 1(b). Be that as it may, such waveforms may contain high-arrange music which will be hard to track and control for an exceptionally underdamped second-arrange framework. Utilizing the very same circuit design, Wang et al. [5] propose to infuse a dc counterbalance in the capacitor reference voltage with the goal that the symphonious substance may turn out to be little and it might encourage the shut circle controller plan.All things considered, since the capacitor voltage does not go down to zero, it won't be completely released, which implies that the film capacitor isn't completely used. The comparable pay idea in light of capacitive swell power decoupling has likewise been talked about in. An all the more as of late proposed dynamic power decoupling strategy is talked about in and its circuit chart is appeared in Fig. 1(c). The presented half-connect, together with one leg of the full-connect rectifier, basically shapes another full-connect circuit, and for this situation, the voltage of the film capacitor can be controlled to be sinusoidal and it settle all the troubles said beforehand. Despite the fact that being powerful in swell power pay, this topology isn't relevant in a few conditions, e.g., PFCs and unfurling span based inverters, in light of the fact that the power stream is unidirectional. It might likewise end up noticeably tricky in H5 inverters, where the full-connect circuit will be irregularly confined from the dc interface to dispose of the spillage current. In a stacked exchanged capacitor idea is proposed as the energy support for single phase frameworks. Nonetheless, the circuit

may include a huge number of capacitors and switches if high energy buffering proportion is sought after. In addition, this circuit hypothetically can't accomplish culminate dynamic power decoupling and little voltage vacillation may dependably exist in the dc interface. Rather than utilizing paralleled circuit setups talked about beforehand, Wang et al. [6] propose an arrangement pay approach where a controlled voltage source is embedded in between the dc-interface capacitor and the heap and through along these lines, low-voltage semiconductors can be utilized to develop the dynamic control decoupling circuit and to pick up an enhanced framework execution. Despite the fact that the dc-connect capacitance can be decreased paying little mind to the designs of remuneration circuits, a typical issue for the current dynamic power decoupling strategies is that, the framework swell power must be ingested by extra energystorage components, either inductors or film capacitors, and this infers the capacitance lessening isn't advanced [7].With a specific end goal to accomplish a basic and reduced plan, and furthermore to break the impediment forced by the front-end topology in, this paper proposes another topology to acknowledge dynamic power decoupling, and its circuit outline is appeared in Fig. 2. As anyone might imagine seen, two indistinguishable film capacitors are utilized and associated in arrangement in the dc interface, whose midpoint is then associated with another stage leg through a little sifting inductor.

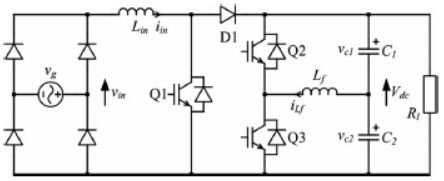


Figure 2. Proposed symmetrical half-bridge circuit for single-phase active power decoupling.

Along these lines, the dc-interface capacitors may not just give a high-voltage dc transport to help ac/dc or dc/ac transformation, however can likewise ingest the framework swell power. The additional symmetrical half-connect circuit is additionally simple to control, on the grounds that the voltages of the two film capacitors will both be sinusoidal. In addition, the capacitors can be then again released to zero in the event that that high swell control remuneration is required, and the power decoupling can be refined without utilizing extra energystorage inductors or, on the other hand capacitors. The power stream engaged with this circuit and the important controller configuration are nitty gritty in this paper. Both reproduction and test comes about are exhibited to demonstrate the viability of this idea.

II. CIRCUIT ANALYSIS AND OPERATING PRINCIPLES

The proposed symmetrical half-connect circuit is appeared in Figure 2, which is connected to a solitary stage PFC converter as a case here. It ought to be noticed that and furthermore as specified beforehand, the proposed dynamic power decoupling technique will not be obliged by its front-end topologies, and it can be essentially utilized as a part of any single-stage ac/dc or dc/ac frameworks, as long as there is a high-voltage dc transport accessible. For this situation, two indistinguishable film capacitors, having C1 = C2 = Cfareassociated in arrangement to develop the dc-interface voltage Vdc, and vc1 (t) and vc2 (t) are utilized to mean the voltages of the upper and lower capacitors, individually. Keeping in mind the end goal to give the twofold line recurrence swell control, their voltages are then controlled to be sinusoidal with a counterbalance esteem that equivalents to a large portion of the dc-connect voltage Vdc/2, what's more, they can be composed as

$$\begin{cases} v_{c1}(t) = \frac{V_{dc}}{2} + V_C \sin(\omega t + \theta) \\ v_{c2}(t) = \frac{V_{dc}}{2} - V_C \sin(\omega t + \theta) \end{cases} \quad (1)$$

Where θ is the stage edge between the capacitor voltage vc1 (t) also, the information voltage vin (t), and ω is the essential precise recurrence. Vc is the sufficiency of the film capacitor voltage having Vc ≤ Vdc/2. The capacitor current ic1 (t) and ic2 (t) can at that point be effortlessly inferred as

$$\begin{cases} i_{c1}(t) = I_c \cos(\omega t + \theta) = \omega C_f V_c \cos(\omega t + \theta) \\ i_{c1}(t) = -I_c \cos(\omega t + \theta) = -\omega C_f V_c \cos(\omega t + \theta) \end{cases} \quad (2)$$

Where *Ic*is the amplitude of the filtered capacitor current. The instantaneous power *pc* (*t*) provided by these two capacitors will be

$$p_{c(t)} = v_{c1}(t) i_{C1}(t) + v_{c2} i_{C2}(t)$$
$$= 2V_c \sin(\omega t + \theta) \omega C_f V_c \cos(\omega t + \theta) \quad (3)$$
$$= \omega C_f {V_c}^2 \sin(2\omega t + \theta)$$

In order to achieve accurate power compensation, the instantaneous power *pLf*(*t*) of the filter inductor *Lf* must also be taken into consideration

$$i_{Lf(t)} = i_{c1}(t) - i_{c2}(t)$$

$$= 2I_c \cos(\omega t + \theta) = 2\omega C_f V_c \cos(\omega t + \theta) (4)$$

$$P_{Lf}(t) = L_f \frac{di_{Lf}(t)}{dt} i_{Lf}(t)$$

$$= -\omega L_f \left(2\omega C_f V_c\right)^2 \sin(\omega t + \theta) \cos(\omega t + \theta) =$$

$$-2\omega L_f \left(\omega C_f V_c\right)^2 \sin(2\omega t + 2\theta) \quad (5)$$

Therefore, the total instantaneous power *phb*(*t*) provided by the symmetrical half-bridge circuit will be

$$phb(t) = p_c(t) + pLf(t)$$

$$= \left[\omega C_f {V_c}^2 - 2\omega L_f \left(\omega C_f V_c\right)^2\right] \sin(2\omega t + 2\theta) \quad (6)$$

Equation (6) shows that the filter inductor may reduce the compensation capacity of this circuit and its value should be minimized in the design.

The instantaneous power to the PFC stage *ppf c* (*t*) can be found in a similar manner by defining the input voltage *v*in(*t*) and current *i*in(*t*) to be

$$v_{in}(t) = V_{in} |sin(\omega t)| \quad \text{And} \quad i_{in}(t) = I_{in} |\sin(\omega t)| \quad (7)$$

$$pPFC(t) = p_{in}(t) + p_{Lin(t)}$$

$$= v_{in}(t) i_{in}(t) + L_{in} \frac{di_{in(t)}}{dt} i_{in}(t)$$

$$= \frac{V_{in} I_{in}}{2} - \frac{V_{in} I_{in}}{2} \cos(2\omega t) + \frac{\omega L_{in} {I_{in}}^2}{2} \sin(2\omega t) \quad (8)$$

Where sin (*ωt*) ≠ 0. By equating the time-varying terms of (8) to (6), it is possible to derive that

$$\theta = \frac{1}{2} arc \tan\left(-\frac{V_{in} I_{in}}{\omega L_{in} {I_{in}}^2}\right) = \frac{1}{2} arc \tan\left(-\frac{V_{in}}{\omega L_{in} I_{in}}\right) \quad (9)$$

For this situation, the voltage references of C1 and C2 can be dictated by (2), and through shut circle control, the framework swell power can be nearly crossed out by these two dc-connect capacitors and the dc-interface voltage will be genuinely consistent. It ought to be noticed that in handy usage, there may exist a few blunders because of parameter resilience of the segments furthermore, constrained remuneration pick up, and a shut circle alteration of the voltage references might be required to tweak the swell control pay as examined.

The glorified working waveforms of the proposed converter are introduced in Fig. 3, where the channel inductance, exchanging misfortune, and conduction misfortune in the circuit are altogether disregarded. It is clear that the two dc-connect capacitors can give the fluctuating control that can be utilized to cross out those proliferated from the air conditioner lattice side, and the voltage of the upper

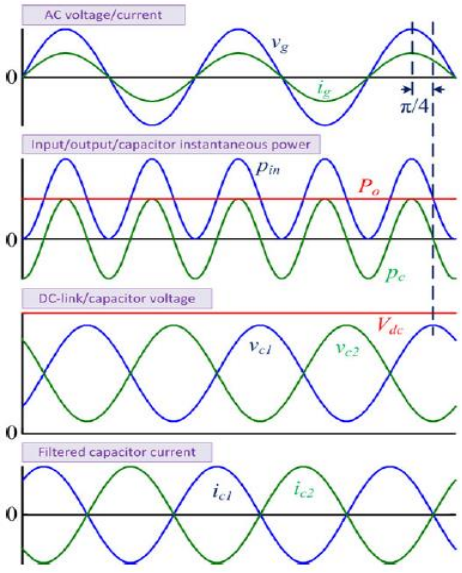


Figure 3. Idealized operating waveforms for the proposed active power decoupling circuit.

$$V_c = \sqrt{\frac{\sqrt{\left(\frac{V_{in}I_{in}}{2}\right)^2+\left(\frac{\omega L_{in}I_{in}^2}{2}\right)^2}}{\omega C_f - 2\omega L_f(\omega C_f)^2}} \quad (10)$$

capacitor has π/4 stage move with the framework voltage.

With a specific end goal to inspect the capacitance decrease accomplished by the proposed dynamic power decoupling technique, the swell power over the inductors Lin and Lf are dismissed on the grounds that they are nearly considerably littler than those capacitive ones. At that point, the symmetrical half-connect circuit can give the greatest swell power when Vc = Vdc/2 and as indicated by (2)

$$\omega C_f V_c^2 = \frac{V_{in}I_{in}}{2} \text{And} \frac{\omega C_f V_{dc}^2}{4} = P_{in} \quad (11)$$

$$C_{eq} = \frac{C_f}{2} = \frac{2P_{in}}{\omega V_{dc}^2} (12)$$

Where *P*in is the amplitude of the input ripple power and *C*eqis the equivalent dc-link capacitance. For a typical 60-Hz power system with a dc-link voltage of 380 V, the required capacitance is only 36.7 μF/kW according to (3).

In contrast, if there is no active power decoupling and it is desired that the dc-link voltage ripple should be less than 1% of the nominal voltage, the dc-link capacitance would be [5]

$$0.01V_{dc} = \frac{P_{in}}{2\omega C_{dc}V_{dc}} \text{And } C_{dc} = \frac{50P_{in}}{\omega V_{dc}^2} \quad (13)$$

Condition (4) plainly demonstrates that the dc-interface capacitance can hypothetically be decreased by 25 times when contrasted with that of a customary aloof approach. Be that as it may, by and by, the change may not be so huge in light of the fact that the capacitor voltage Vc is ordinarily controlled to be marginally not as much as Vdc/2 in request to counteract over modulation of the symmetrical half-connect. Fig. 4 demonstrates the dc-interface capacitance prerequisite with deference to the power rating of the converter and the adjustment record of the symmetrical half-connect circuit. The adjustment file is standardized to solidarity when Vc = Vdc/2.

In specific applications, e.g., PFC converters for PC control supplies, there is another necessity for the yield capacitors, which is to keep up the yield voltage for a short period regardless of whether its ac side information voltage is lost. The required capacitance would then be able to be computed as

$$C_{dc} \geq \frac{2.P_{out}.t_{holdup}}{V_{dc}^2 - V_{dc\_}min^2} \quad (14)$$

Where the regular detail for this robbery time told up is 20 ms. On the off chance that the base dc-interface voltage vdc min is characterized to be 250 V and the power misfortunes of the PFC converter are ignored, the required capacitance is observed to be 488.4 μF/kW, which is adequate to give swell power remuneration even just 0.5 adjustment record is connected to the converter as per Figure 4.

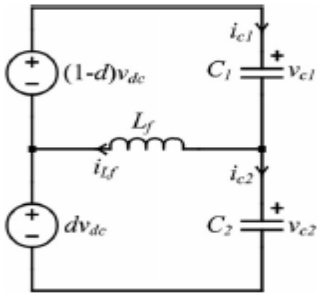


Figure 4. Averaged equivalent circuit of the proposed symmetrical half-bridge.

III. SYSTEM MODELING AND THE CONTROLLER DESIGN

The displaying and controller outline of the PFC converter has been widely talked about in the writing and consequently will not be tended to in this paper. For the presented symmetrical half-connect, it essentially has two exchanging states and its comparing time-found the middle value of model can be determined by averaging the state conditions over an exchanging cycle. The resultant comparable circuit demonstrates is appeared in Figure 5 and in light of

this model, it is simple to infer the accompanying differential conditions:

$$\begin{cases} L_f \frac{di_{Lf}(t)}{dt} = -v_{c1}(t) + [1 - d(t)].v_{dc}(t) \\ C_f \frac{dv_{c1}(t)}{dt} = i_{c1}(t) \end{cases} \quad (15a)$$

$$\begin{cases} L_f \frac{di_{Lf}(t)}{dt} = v_{c2}(t) - d(t).v_{dc}(t) \\ C_f \frac{dv_{c2}(t)}{dt} = i_{c2}(t) \end{cases} \quad (15b)$$

Where $d(t)$ is the duty cycle applied to the upper switch Q2 shown in Figure 2. Ideally, the compensation network can cancel the ac side ripple power and the dynamics of the dc-link voltage and its ripple component can be neglected. In this case, by substituting (2) and (4) into (15.b)

$$\begin{cases} L_f \frac{di_{Lf(t)}}{dt} = v_{c2}(t) - d(t).V_{dc} \\ C_f \frac{dv_{c2}(t)}{dt} = -\frac{i_{Lf}(t)}{2} \end{cases} \quad (16)$$

Taking the Laplace transform of (16) and also considering the damping effect of a practical circuit, the control-to-capacitor voltage transfer function *Ghb*can finally be derived as

$$G_{hb} = \frac{v_{c2}(s)}{d(s)} = \frac{V_{dc}}{2L_f C_f s^2 + K_d C_f s + 1}$$

And

$$\omega_{res} = \frac{1}{\sqrt{2L_f C_f}} \quad (17)$$

Where Kd is a parameter that speaks to the damping impact gave by the ESR of latent segments and ωresis the LC full recurrence. The ESRs of the capacitors are overlooked here on the grounds that they are of film sort and have to a great degree low esteem.

It ought to be noticed that by and by, there dependably exists some control mistakes and part resilience, and in this manner, the dc-link voltage swell may not be zero and present the basic mode current in the two decoupling capacitors. For this situation, ic1 (t) = –ic2 (t) = iLf (t)/2 is never again legitimate and with a specific end goal to dispose of the unsettling influence from the dc interface, the deliberate capacitor voltage vc2 (t) ought to be preprocessed before being sent into the voltage controller as takes after

$$v_c(t) = \frac{v_{c2}(t) - v_{c1}(t)}{2} = \frac{2v_{c2}(t) - v_{dc}(t)}{2} \quad (18)$$

The above equation in effect indicates that the control variable should be changed to *vc*2 (*t*) – *vc*1 (*t*) rather than *vc*2 (*t*). Combining (15) and (18)

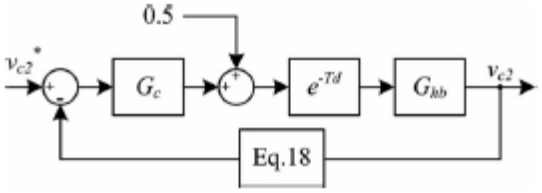
$$\begin{cases} 2L_f \frac{di_{Lf}(t)}{dt} = v_{c2}(t) - v_{c1}(t) + [1 - 2d(t)].v_{dc}(t) \\ = 2v_c(t) + [1 - 2d(t)].v_{dc}(t) \\ C_f \frac{d[v_{c2}(t) - v_{c1}(t)]}{dt} \\ = 2C_f \frac{dv_c(t)}{dt} = i_{c2}(t) - i_{c1}(t) = \_i_L(t) \end{cases} \quad (19)$$

By introducing perturbation in the state variables

$$\begin{cases} L_f \frac{d[I_{Lf} + \hat{\imath}_{Lf}(t)]}{dt} = [V_c + \hat{v}_c(t)] + \left[\frac{1}{2} - D - \hat{d}(t)\right] \\ .[V_{dc} + \hat{v}_{dc}(t)] \\ C_f \frac{d[V_c + \hat{v}_c(t)]}{dt} = -\frac{I_{Lf} + \hat{\imath}_{Lf(t)}}{2} \end{cases} \quad (20)$$

By equating ac and dc quantities and then proceed only with ac equations (neglect second-order ac quantities)

$$\begin{cases} L_f \frac{\widehat{di}_{Lf}(t)}{dt} = \hat{v}_c(t) - \hat{d}(t).V_{dc} + \left(\frac{1}{2} - D\right).\hat{v}_{dc}(t) \\ C_f \frac{d\widehat{v_c}(t)}{dt} = -\frac{\hat{\imath}_{Lf}(t)}{2} \end{cases} \quad (21)$$



Figuer 6. Control block diagram for the proposed active power decoupling circuit.

At the point when worked around the quiet point, the impact of the swell voltage can be ignored in light of the fact that 1/2 – D is similarly significantly littler than Vdc. For this situation, the unsettling influence from the dc connection can be dispensed with and is

streamlined to be the same as and subsequently, the plant move work appeared in still remains constant. Utilizing the parameters recorded in Table I, the open loop pick up of this framework is plotted as the strong line in Fig. 6, where plainly its stage reaction is about –180° after the LC thunderous recurrence. This paper proposes an altered sort III compensator to balance out this framework and it is inserted with a thunderous controller, which guarantees zero unfaltering state following mistake of the voltage control circle, and its exchange work can be composed as

$$G_c = K_p \frac{\left(\frac{s}{\omega_{z1}}+1\right)\left(\frac{s}{\omega_{z2}}+1\right)}{\left(\frac{s}{\omega_p}+1\right)} \frac{s}{s^2+\omega^2} \qquad (22)$$

Where ωz1 and ωz2 are the two zeroes to give stage help ability and ought to be set around the LC reverberation recurrence. ωp is the post to lessen the framework high-arrange music what's more, is ordinarily been not as much as half of the framework exchanging frequency. Kp is the relative pick up that modifies the framework hybrid recurrence. Since the ESR of film capacitors is low, there is no compelling reason to add another post to scratch off the ESR zero of capacitors, which for this situation is well over the framework control recurrence. The Bode graph of the outlined controller is then plotted as the dashed line in Fig. 6 and it demonstrates that this controller can give most extreme stage increase in 67.3° at 1040 Hz, and it additionally has high pick up at principal recurrence to complete the voltage following mistake to be zero. The control square graph is appeared in Fig. 6 and it is connected to control the voltage of the lower capacitor in the dc connect, andthe voltage of the upper capacitor will be naturally determined because the total dc bus voltage is already regulated by the PFC controller, which is usually a very slow control loop.

IV. FUZZY LOGIC CONTROLLER

Fuzzy logic is a complex mathematical method that allows solving difficult simulated problems with many inputs and output variables. Fuzzy logic is able to give results in the form of recommendation for a specific interval of output state, so it is essential that this mathematical method is strictly distinguished from the more familiar logics, such as Boolean algebra.

In order to operate fuzzy logic needs to be represented by numbers or descriptions. For example, speed can be represented by value 5 m/s or by description “slow”. Term “slow” can have different meaning if used by different persons and must be interpreted with respect to the observed environment. Some values are easy to classify, while others can be difficult to determine because of human understanding of different situations. One can say “slow”, while other can say “not fast” when describing the same speed. These differences can be distinguished with help of so-called fuzzy sets.

Usually fuzzy logic control system is created from four major elements presented on Figure.7: fuzzification interface, fuzzy inference engine, fuzzy rule matrix and defuzzification interface. Each part along with basic fuzzy logic operations will be described in more detail below.

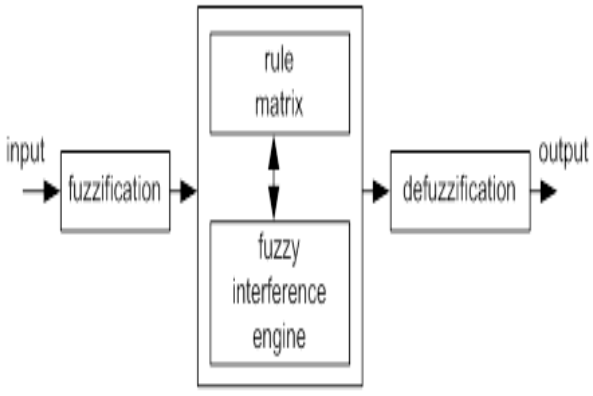
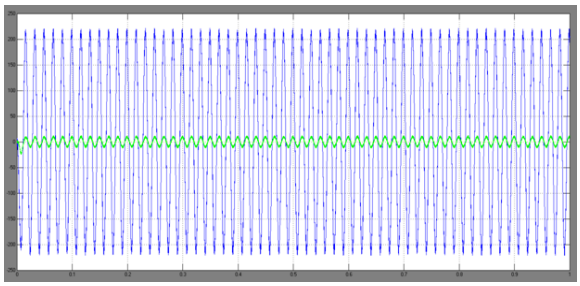
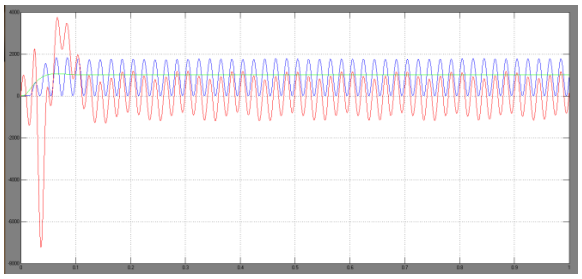


Figure 7. Fuzzy logic controller

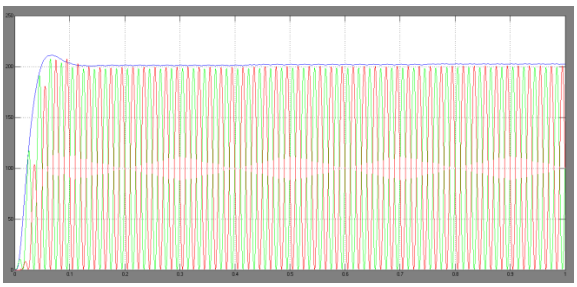
V. SIMULATION RESULTS



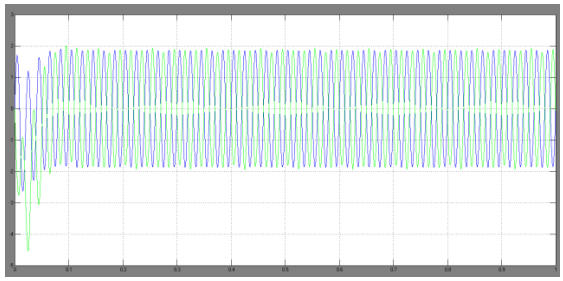
(a) Ac voltage and Current(Vg,Ig)



(b) Input output capacitor instantaneous power (Pin, Po ,Pc)

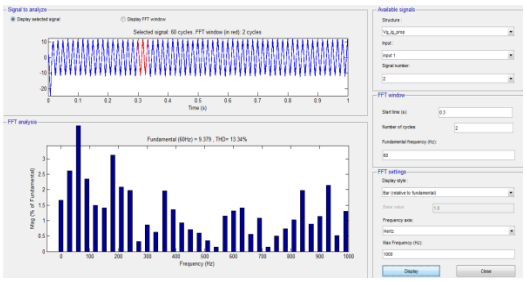


(c) DC link capacitor voltage (Vdc,Vc1,Vc2)



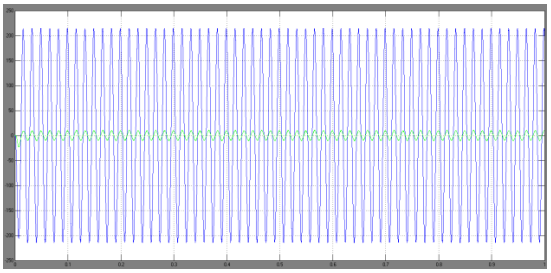
(d) Filtered capacitor currents (Ic1,Ic2)

(e) THD values of Vg

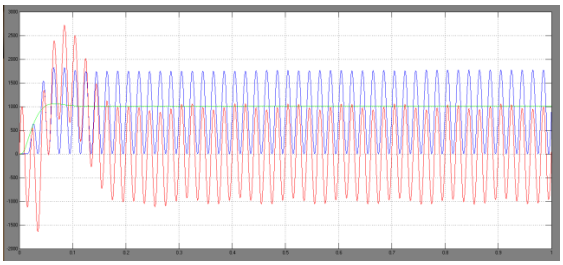


(f) THD values of Ig

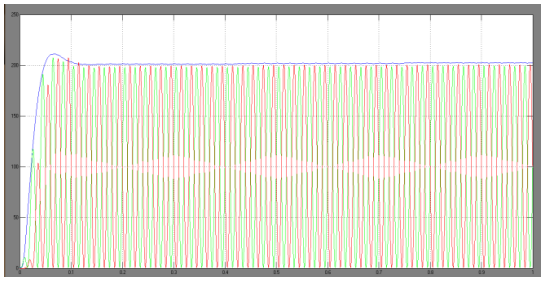
Figure 8. Simulation results showing the key operating waveforms of the proposed active power decoupling circuit.



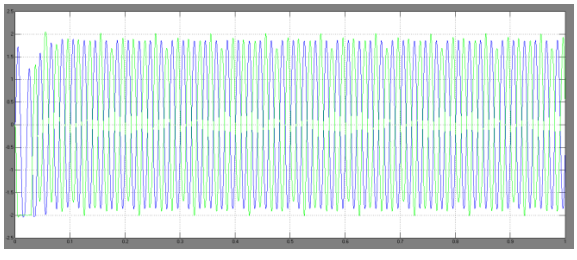
(a) Ac voltage and Current (Vg, Ig)



(b) Input output capacitor instantaneous power (Pin, Po ,Pc)



(c) DC link capacitor voltage (Vdc,Vc1,Vc2)



(d) Filtered capacitor currents (Ic1,Ic2)

(e) THD values of Vg

(f) THD values of Ig

Figure 9. Simulation results showing the key operating waveforms of the active power decoupling circuit by using fuzzy logic controller.

Table 1. Comparison of THD values for proposed controller and FLC controller

Signals	Active power controller	Fuzzy logic controller
Grid Voltage(Vg)	1.91%	0.24 %
Grid Current(Ig)	13.34%	3.30%

VI. CONCLUSION

This paper has introduced a fuzzy logic controller to symmetrical half-connect circuit to decouple the fluctuating power in single-phaseac/dc and dc/acsystems. The dc-connect capacitors in the proposed framework may not just give a high-voltage dc transport to help control change, yet additionally ingest the framework swell power started from the air conditioner side. The subsequent framework is more practical as looked at to other existing dynamic power decoupling strategies since it does not require extra detached parts to store the framework swell energy. The swell voltage in the dc interface and the THD of the brace current can be fundamentally diminished, which demonstrates the viability of the proposed arrangement. The proposed symmetrical half-scaffold can likewise be viewed as a non specific converter cell furthermore, may be a promising answer for disposal of the fluctuating control and the lessening of dc-connect capacitance in other propelled topologies, e.g., NPCs and MMCs. By using fuzzy logic controller for decoupling the fluctuating power gives a reliable operation and dynamic responses in results than compared to proposed active power controller.

VII. REFERENCES

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