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PLL Structures System for Distributed Generation Systems Under Grid Fault Conditions

Mallela Naresh[1], P. Chinnaiah[2], V. Sunil Kumar Reddy[3]

[1]M. Tech, Department of Electrical and Electronics Engineering (EPS), MJR college of engineering and technology, Piler, Andhra Pradesh, India

[2]Assistant professor, Department of Electrical and Electronics Engineering, MJR College of engineering and technology, Piler, Andhra Pradesh, India

[3]HOD, Department of Electrical and Electronics Engineering, MJR College of engineering and technology, Piler, Andhra Pradesh, India

ABSTRACT

This project presents a fuzzy logic controller based PLL's for dissects the synchronization ability of the power system. The fuzzy logic controller incorporated with the decoupled double synchronous reference (PLL), the dual second order generalized integrator PLL, and the three-phase enhanced PLL, intended to work under grid fault conditions. In grid fault conditions we used existing methods without fuzzy logic controller PLL's by using these methods we improve the ability of the grid systems. By using these controllers we synchronized the system voltage magnitude and angles. In proposed method we use the fuzzy logic controller based PLL's for synchronized the voltage magnitude and angles. Compared to existing method in proposed method we achieve fast speed response for different grid faults.

Keywords : PLL, Fuzzy Logic Controller, TSO, LVRT, GCR, FRT, DSOGI

I. INTRODUCTION

The expanded infiltration of these advances in the electrical system has strengthened the effectively existing worry among the transmission system administrators (TSOs) about their impact in the network security; as a result, the systemconnection models are turning out to be increasingly prohibitive for distributiongeneration systems in all nations.

In the actual grid code necessities (GCRs), uncommon imperatives for the operation of such plants under grid voltage Deficiencyconditions have picked up an awesome significance. These necessities decide the fault limits among those through which a system to the networkshould stay connected with the system, offering ascend to particular voltage profiles that indicate the profundity and leeway time of the voltage hangs that they should withstand. Such prerequisites are known as low voltage ride through (LVRT) and are depicted by a voltage versus time characteristic.

In spite of the fact that the LVRT prerequisites in the distinctive gauges are altogether different,the principal issue that generationsystems must bear the cost of when a voltage droop happens is the confinement of their transient reaction, keeping in mind the end goal to maintain a strategic distance from its defensive detachment from the system. This is the situation, for occasion, of altered speed wind turbines in view of squirrel enclosure instigation generators, where the voltage drop in the stator

windings can lead the generator to an overspeed stumbling.

Arrangements in view of the improvement of assistant systems, for example, STATCOMs and element voltage controllers (DVRs), have assumed a definitive part in upgrading the issue ride through (FRT) capacity of distributed generation systems. Similarly, propelled control functionalities for the force converters have additionally been proposed.

In specific nations, the TSOs additionally give the active/reactive power example to be infused into the system amid a voltage droop; this is the situation for the German E-on and the Spanish Red Electrical Española(REE). This pattern has been taken after by whatever is left of the TSOs; additionally, it is trusted that this operation prerequisite will be broadened, and particular requests for adjusted and unequal lists will emerge in the accompanying variants of the lattice codes around the world.

With respect to operation of the distributed generation systems under adjusted and unequal issue conditions, applicable commitments, for example, can be found in the writing. These arrangements depend on cutting edge control systems that need exact data of the matrix voltage variables keeping in mind the end goal to work legitimately, something that has provoked the significanceof system synchronization calculations. In force systems, the synchronous reference outline PLL (SRF PLL) is the most expanded strategy for synchronizing with three-phase systems. In any case, regardless of the way that the execution of SRF PLL is acceptable under adjusted conditions, its reaction can be deficient under unequal, defective, or mutilated conditions.

Three enhanced and propelled grid synchronization systems are concentrated on and assessed: the decoupled doublesynchronous reference outline PLL (DDSRF PLL), the double second request summed up integrator PLL (DSOGI PLL), also, the three-phase enhanced PLL (3phEPLL). Their execution, computational expense, and dependability of the adequacy what's more, phase discovery of the positive arrangement of the voltage, under uneven and misshaped circumstances, have been assessed as per test lattice, which have been replicated in a real scaled electrical system.

II. GRID SYNCHRONIZATION SPECIFICATIONSBASED ON GCR

Despite the fact that few works are distributed inside of the field of grid synchronization, every one of them are focused on breaking down the individual element execution of every proposition, without first deciding a period reaction window inside of the dynamic conduct of the grid under test, which would be thought to be agreeable.

In spite of the way that the identification of the issue can be conveyed out with more straightforward calculations, the significance of cutting edge matrix synchronization systems lies in the need of having precise data about the size what's more, period of the matrix voltage amid the flaw, keeping in mind the end goal to infuse the reactive force required by the TSO. In the German standard, it is expressed that voltage control must happen inside of 20 ms after the flaw acknowledgment, by giving a reactive current on the low voltage side of thegenerator transformer to no less than 2%of the appraised current for each percent of the voltage dip, as appeared in Figure 1. 100% responsive power conveyance must be conceivable, if fundamental.

III. DESCRIPTION OF THE THREESYNCHRONIZATION SYSTEMS

A large portion of the positive-sequence location calculations are taking into account SRF PLLs. In spite of having a decent reaction under adjusted conditions, their execution gets to be deficient in unequal flawed lattices (95% of cases), and their great operation is exceedingly adapted to the frequency steadiness, which is contradictory with a strong synchronization

system. Numerous creators have talked about various propelled models, whichcan beat the issues of the traditional PLL, utilizing frequency and abundance versatile structures which can manage uneven, broken, and consonant dirtied networks. In the system of these topologies, three PLL structures will be examined and assessed in this paper.

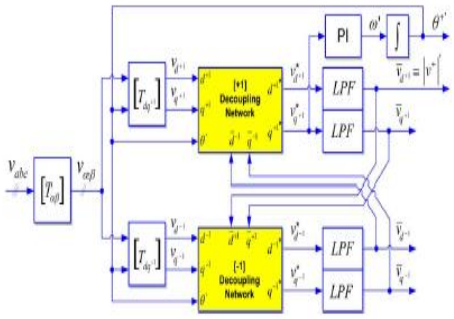


Figure 1. DDSRF-PLL block diagram.

A. Ddsrf Pll

The DDSRF PLL was produced for enhancing the ordinary SRF PLL. This synchronizationsystem abuses two synchronous reference outlines pivoting at the essential utility frequency, one counterclockwise and another clockwise, keeping in mind the end goal to accomplish an exact location of the positive-and negative-succession segments of the lattice voltage vector when it is influenced by unequal lattice issues. The graph of the DDSRF PLL is appeared in Figure 1.

At the point when the three-phase grid voltage is unequal, the crucial positive-arrangement voltage vector shows up as a dc voltage on the dq+1 tomahawks of the positive-arrangement SRF and as air conditioning voltages at double the major utility frequency on the dq–1 axes of the negative-arrangement SRF. Conversely, the negativesequence voltage vector will bring about a dc segment on the negative-succession SRF and an air conditioner wavering on the positivesequence SRF. Since the plentifulness of the wavering on the positive-grouping SRF matches the dc level on the negativesequence SRF and the other way around, a decoupling system is connected to signals on the dq positive/negative SRF axes with a specific end goal to counteract such air conditioning motions. Low-pass filters (LPFs) in Figure 1 are in charge of separating the dc part from the sign on the decoupled SRF axes. These dc parts gather data about the adequacy and phase point of the positive-and negative-arrangement segments of the matrix voltage vector.

At last, the PI controller of the DDSRF PLL deals with the decoupled q-pivot sign of the positive-grouping SRF (v∗ q+1) what's more, performs the same capacity as in a SRF PLL, adjusting the positive-arrangement voltage with the d-hub. This sign is free of ac segments because of the impact of the decoupling systems; the transfer speed of the circle controller can be hence expanded.

B. Dsogi Pll

The working standard of the DSOGI PLL for assessing the positive-and negative-grouping segments of the network voltage vectors depends on utilizing the quick symmetrical part (ISC) technique on the αβ stationary reference outline,

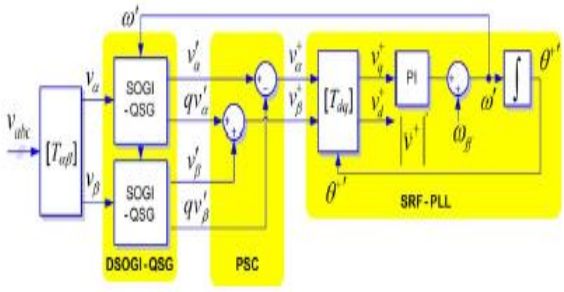


Figure 2. DSOGI-PLL block diagram.

as clarified in. The graph of the DSOGI PLL is appeared in Figure 2. As it can be seen, the ISC strategy is executed by the positive-grouping estimation square.

To apply the ISC strategy, it is important to have an arrangement of signs, vα–vβ, speaking to the information voltage vector on the αβ stationary reference outline together with another arrangement of signs, qvα–qvβ, which are in quadrature and slacked concerning vα–vβ. In the DSOGI PLL, the signs to be supplied to the ISC strategy are gotten by utilizing a double second request summed up

integrator (DSOGI), which is a versatile bandpassfilter in view of the summed up integrator concept.At its output, the DSOGI gives four signs, in particular, vα what's more, vβ, which are sifted variants of vα and vβ, separately, furthermore, qvα and qvβ, which are the in-quadrature versionsof vα and vβ.

A traditional SRF PLL is connected on the assessed positive-arrangement voltage vector, v+αβ, to make this synchronization systemfrequency versatile. Specifically, the v+αβ voltage vector is meant the pivoting SRF and the sign on the q-hub, v+q , is connected at the info of the circle controller.As a result, the basic network frequency (ω) and the phase edge of the positive-succession voltage vector (θ+) are evaluated by this circle. The evaluated frequencyfor the major lattice part is encouraged back to adjust the middle frequency ω of the DSOGI.

C. 3phepll

The improved phase bolted circle (EPLL) is a synchronization system that has demonstrated to give great results in singlephase synchronization systems. An EPLL is basically a versatile bandpass filter, which can alter the cutoff frequency as an element of the information signal. Its structure was later adjusted for the three-phase case, with a specific end goal to distinguish the positive-succession vector of three-phase signals, getting the 3phEPLL that is spoken to in Figure 3.

For this situation, every phase voltage is prepared freely by an EPLL. This square filters the information signal and generatestwo sinusoidal outputs of the same adequacy and frequency,vn and jvn, the second one being 90◦ as for vn.The comings about signs constitute the data for the computational unit. Inferable from these in-quadrature flags, the quick positive-grouping voltage part, v+abc, can be evaluated by method for utilizing the ISC strategy.

IV. DISCRETE IMPLEMENTATION

The execution of the diverse structures under test is truly reliant on their last advanced usage, especially on the discretization approach made to their continuous equations.

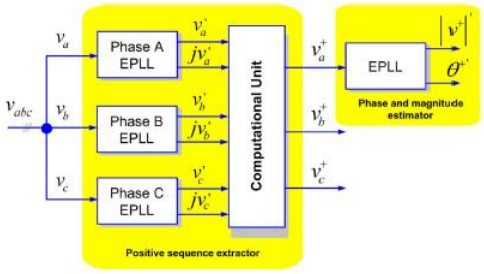


Figure 3. 3phEPLL block diagram.

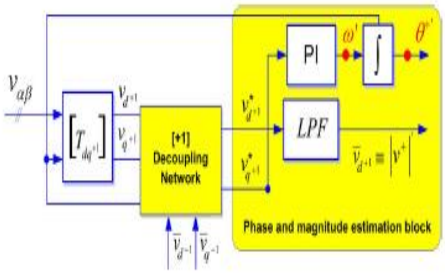


Figure 4. Phase and magnitude estimation loop of the DDSRF PLL.

This usage is basic and ought to be concentrated on in subtle element as a direct usage can offer ascent to extra delays on top of it that thwart the great execution of the PLL. A few strategies, for example, the forward Euler, the regressive Euler, and the Tustin (trapezoidal) numerical combination, offer a decent execution when utilized for discretizing other synchronization systems. In any case, Euler techniques can be insufficient under specific conditions, because of the need of presenting extra example delays. Consequently, as indicated by the particular needs of the displayed topologies, this segment will depict the discrete representation of each PLL independently. Keeping in mind the end goal to encourage the perception of theprocess, the diverse building hinders that show up at Figs. 1–3 will be referenced.

A. Ddsrf-Pll Discretization

The discrete model of this PLL can be effectively acquired subsequent to the consistent representation of a few sections does not change in the discrete space. This is the situation for the change pieces Tαβ, Tdq+1, and Tdq–1, whose depiction can be found as rule scope writing.

1) Positive-and Negative-Sequence Decoupling Networks:The decoupling system constitutes a standout amongst the most vital commitments of this synchronization technique. The discrete equations of these squares are appeared in (1), being practically the same as in the nonstop area. It is only important to think of one as test deferral of θ, ¯vd–1 , ¯vq–1 , ¯vd+1, and ¯vq+1 in request to stay away from logarithmic circles.

2) Phase and Magnitude Estimator Discretization: In the DDSRF PLL, the decoupling system seems inserted in the established SRF-PLL circle (see Figure

3) Be that as it may, this doesn'tinfluence the discretization of the phase and greatness estimator since v∗d+1 and v∗q+1 go about as the info of this square.

$$\begin{bmatrix} v^*_{d^{+1}}[n+1] \\ v^*_{q^{+1}}[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d^{+1}}[n+1] \\ v_{q^{+1}}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(2\theta'[n]) & -\sin(2\theta'[n]) \\ \sin(2\theta'[n]) & -\cos(2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d^{-1}}[n] \\ \bar{v}_{q^{-1}}[n] \end{bmatrix} \times \begin{bmatrix} v^*_{d^{-1}}[n+1] \\ v^*_{q^{-1}}[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d^{-1}}[n+1] \\ v_{q^{-1}}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(-2\theta'[n]) & -\sin(-2\theta'[n]) \\ \sin(-2\theta'[n]) & -\cos(-2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d^{+1}}[n] \\ \bar{v}_{q^{+1}}[n] \end{bmatrix}. \quad (1)$$

The discrete controller and the integrator can be assembled utilizing a in reverse numerical estimation. The frequency and phase can then be spoken to in the z-area (2), considering v∗q+1 as the blunder to be minimized. In this comparison, a feed forward of the ostensible frequency is given by method for ωff

$$W'(z) = \frac{(k_p + k_i \cdot T_s)z - k_p}{z-1} \cdot V^*_{q^{+1}}(z) + \omega_{ff}$$
$$\theta^{+'} = \frac{T_s \cdot z}{z-1} \cdot W'(z). \quad (2)$$

At long last, specimen based representation offers ascend to (3), which are the expressions to be actualized

$$\omega'[n+1] = \omega'[n] - k_p \cdot v^*_{q^{+1}}[n] + (k_p + k_i \cdot T_s) \cdot v^*_{q^{+1}}[n+1]$$
$$\theta^{+'}[n+1] = \theta^{+'}[n] + T_s \cdot \omega'[n+1]. \quad (3)$$

In these mathematical statements, a frequency feed forward has been presented
as an underlying condition to ω.

4) LPF Block Discretization: The amplitudes of the dq positive-and negative-grouping parts are the outputs of the decoupling systems. Be that as it may, four unending motivation reaction (IIR) LPFs remove the swell from every succession estimation keeping in mind the end goal to fortify the execution of the PLL if there should be an occurrence of symphonious contamination. A first-arrange filter with a cutoff frequencyωf, equivalent to half of the systemfrequency, was initially proposed; thus, the same exchange capacity has been actualized in this paper for assessment purposes in

$$y[n] = \frac{1}{T_s \cdot \omega_f + 1} \cdot x[n] + \frac{T_s \cdot \omega_f}{T_s \cdot \omega_f + 1} \cdot u[n]$$
$$x[n+1] = y[n]. \quad (4)$$

B. Dsogi-Pll Discretization

1) DSOGI-QSG Block Discretization: As was already said in Section II, the DSOGI-based quadrature signal generator (QSG) of Figure 1 comprises of two autonomous what's more, decoupled second-arrange summed up integrators (SOGIs). Along these lines, each SOGI-based quadrature signal generator can be discretized exclusively, in this manner encouraging its numerical portrayal. In Figure 5, the square graph of the actualized SOGI is appeared.

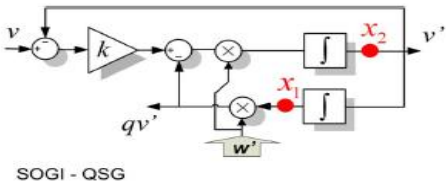


Figure 5. Quadrature signal generator based on a second order generalizedintegrator (SOGI QSG).

This quadrature signal generator (QSG) is a straight system itself; consequently, a discrete representation can be efficiently acquired if the ceaseless state space

is already deducted. The mathematical statements of the SOGI state space seem point by point in (5). Where v constitutes the information while v and qv are the two inquadrature output signals.

$$\left.\begin{aligned}\dot{x}_n &= A\cdot x_n + B\cdot v\\ y_n &= C\cdot x_n\end{aligned}\right\};\quad x_n=\begin{bmatrix}x_1\\x_2\end{bmatrix}\quad y_n=\begin{bmatrix}v'\\qv'\end{bmatrix}$$
$$A=\begin{bmatrix}0 & 1\\ -\omega'^2 & -k\cdot\omega'\end{bmatrix}\quad B=\begin{bmatrix}0\\k\cdot\omega'\end{bmatrix}\quad C=\begin{bmatrix}0 & 1\\ \omega' & 0\end{bmatrix}. \quad (5)$$

$$A'=\gamma\begin{bmatrix}4+2T_s\cdot k\cdot\omega'[n]-T_s^2\cdot\omega'[n]^2 & 4T_s\\ -4T_s\cdot\omega'[n]^2 & 4-2T_s\cdot k\cdot\omega'[n]-T_s^2\cdot\omega'[n]^2\end{bmatrix},\ B'=\gamma\begin{bmatrix}2T_s\cdot k\cdot\omega'[n]\\ 4k\cdot\omega'[n]\end{bmatrix}$$
$$C'=\gamma\begin{bmatrix}-2T_s^2\cdot\omega'[n]^2 & 4T_s\\ 2T_s\cdot\omega'[n]\cdot(2+T_s\cdot k\cdot\omega'[n]) & 2T_s^2\cdot\omega'[n]\end{bmatrix},\ D'=\gamma\begin{bmatrix}2T_s\cdot k\cdot\omega'[n]\\ k\cdot T_s^2\cdot\omega'[n]^2\end{bmatrix}$$
$$\gamma=\frac{1}{4+2\cdot T_s\cdot k\cdot\omega'[n]+T_s^2\cdot\omega'[n]^2} \quad (6)$$

The discretization of this system has been performed utilizing trapezoidal integrators, as they offer a superior discovery of the phase, which is imperative when managing sinusoidal signs. The typical estimations of every lattice of (7) are point by point in (6), appeared at the base of the page. In these networks, Ts is the inspecting time of the discrete system, ω[n] is the assessed frequency greatness, which originates from the estimation made at the SRF-PLL obstruct at every calculation step, and k is the SOGI pick up.

$$\begin{aligned}x[n+1] &= A'\cdot x[n]+B'\cdot v[n]\\ y[n] &= C'\cdot x[n]+D'\cdot v[n].\end{aligned} \quad (7)$$

The discrete state space of (6) is acquired from the ceaseless representation by method for the scientific technique exhibited in (8)

$$\begin{aligned}A' &= \left(I+\frac{A\cdot T_s}{2}\right)\left(I-\frac{A\cdot T_s}{2}\right)^{-1}\\ B' &= \left(I-\frac{A\cdot T_s}{2}\right)^{-1}\cdot B\\ C' &= T_s\cdot C\cdot\left(I-\frac{A\cdot T_s}{2}\right)^{-1}\\ D' &= C\cdot\left(I-\frac{A\cdot T_s}{2}\right)^{-1}\cdot\frac{B\cdot T_s}{2}\end{aligned} \quad (8)$$

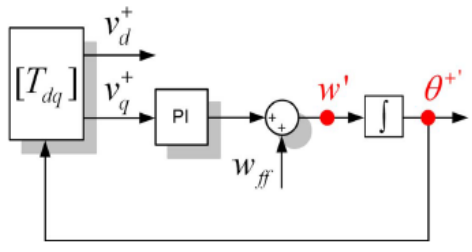


Figure 6. State variables of the SRF-PLL block.

Where Ts is thesamplingtime.

The subsequent discrete system is the best alternative as it decreases the need of utilizing extra postpones for breaking mathematical circles that show up utilizing different strategies which don't consider the SOGI QSG all in all.

2) SRF PLL Discretization: The frequency and phase identification is gotten by method for the SRF PLL appeared in Figure 6. The discretization of the controller and the integrator is performed utilizing the regressive numerical estimate. The frequency and phase can then be spoken to in the z-area, as appeared in (9), where v+ q constitutes the mistake to be minimized.

$$W'(z)=\frac{(k_p+k_i\cdot T_s)z-k_p}{z-1}\cdot V_{q+1}^*(z)+\omega_{ff}$$
$$\theta^{+'}=\frac{T_s\cdot z}{z-1}\cdot W'(z). \quad (9)$$

It can be seen that the past mathematical statements in (9) are equivalent to (2), as, in both cases, a SRF PLL is actualized. In like manner, the specimen based representation of (9) can be composed as appeared in

$$\omega'[n+1]=\omega'[n]-k_p\cdot v_{q+1}^*[n]+(k_p+k_i\cdot T_s)\cdot v_{q+1}^*[n+1]$$
$$\theta^{+'}[n+1]=\theta^{+'}[n]+T_s\cdot\omega'[n+1]. \quad (10)$$

C. 3phEPLL Discretization

This three-phase lattice synchronization system misuses the EPLL as a quadrature signal generator. A free EPLL is utilized for preparing every one of the three-phase voltages. The same EPLL structure is connected again to identify the greatness furthermore, period of the positive-succession voltage segment.

1) QSG Block—EPLL Discretization: The square graph of the EPLL executed in this paper is displayed in Figure 7.

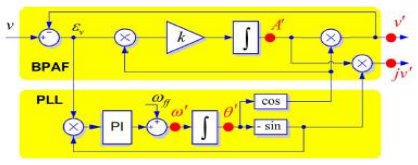


Figure 7. Quadrature signal generator based on an EPLL structure.

As indicated by this graph, the state space representation of the EPLL in the nonstop area can be composed as appeared in

$$\dot{A}'(t) = k \cdot e(t) \cdot \cos\theta'(t)$$
$$\dot{\omega}'(t) = -k_i \cdot e(t) \cdot \sin\theta'(t)$$
$$\dot{\theta}(t) = \omega'(t) + \frac{k_p}{k_i} \cdot \dot{\omega}'(t). \quad (11)$$

The discrete state space variable representation was depicted a forward Euler estimate to reach agreeable results; in this way, the same strategy has been executed here

$$e[n+1] = u[n+1] - v'[n]$$
$$A'[n+1] = A'[n] + T_s \cdot k \cdot e[n] \cdot \cos(\theta'[n])$$
$$\omega'[n+1] = \omega'[n] - T_s \cdot k_i \cdot e[n] \cdot \sin(\theta'[n])$$
$$\theta'[n+1] = \theta'[n] + T_s \cdot \omega'[n] - T_s \cdot k_p \cdot e[n] \cdot \sin(\theta'[n]). \quad (12)$$

At last, after the state variables are ascertained, the EPLL output can be gotten by (13), producing the two quadrature signals

$$v'[n+1] = A'[n+1] \cdot \cos(\theta'[n+1])$$
$$qv'[n+1] = -A'[n+1] \cdot \sin(\theta'[n+1]). \quad (13)$$

This kind of discretization strategy needs a more exact tuning, because of the way that the steady areas of the s-plane furthermore, z-plane are distinctive. Nonetheless, its significant straightforwardness, contrasted with the Tustin or in reverse reconciliation, profits by the computational pace of this piece.

2) Computational Block Unit: The portrayal for this square is the same in both discrete and consistent areas. By the by, particular comparisons are utilized as a part of this paper, as appeared in (14).

3) Phase and Magnitude Detection Block: This component is in view of another EPLL, which is in charge of evaluating the phase and the extent of the positive-arrangement key segment. Its discretization is equivalent to that appeared in (12)

$$v_a^+[n] = \frac{1}{3}v'_a[n] - \frac{1}{6}(v'_b[n] + v'_c[n]) + \frac{1}{2\sqrt{3}}(jv'[n]_b - jv'_c[n])$$
$$v_c^+[n] = \frac{1}{3}v'[n]_c - \frac{1}{6}(v'_a[n] - v'_b[n]) + \frac{1}{2\sqrt{3}}(jv'_a[n] - jv'_b[n])$$
$$v_b^+[n] = -(v_a^+[n] + v_c^+[n]). \quad (14)$$

V. Three synchronization systems under test

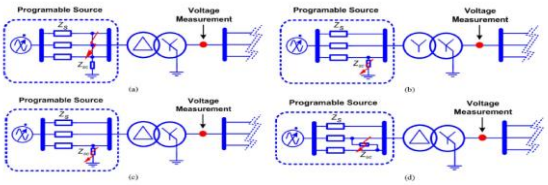
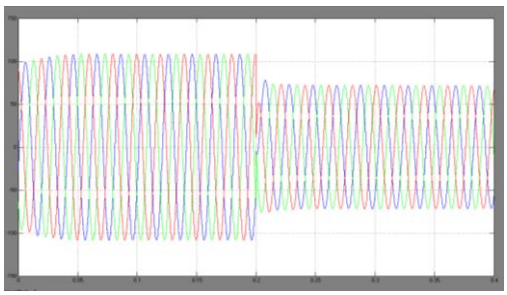


Figure 8. Generation of grid voltage sags in the experimental setup. (a) Generation of a Type "A" voltage sag. (b) Generation of a Type "B" voltage sag.(c) Generation of a Type "C" voltage sag. (d) Generation of aType "D" voltage sag.

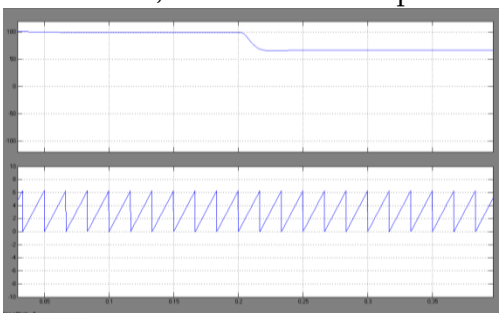
Three of the proposed droops give ascend to lopsided voltages, what's more, thus, to positive-and negative-succession parts. The nearness of the negative arrangement amid the shortcoming permits a more thorough investigation of the synchronization ability of the diverse calculations under test. In addition, uneven issues constitute 95% of the voltage droops that influence appropriated era systems. Keeping in mind the end goal to get the previously stated plunges, distinctive shortcomings have been copied with the programmable air conditioning source at the essential twisting of the transformer, as showed in Figure 8.

Harmonic-dirtied voltage (8% THD): According to the EN50160 standard, the THD of the voltage waveforms at the output of an era office can't be higher than 8%. Considering this prerequisite, the execution of the system synchronization systems under test when the system voltages get to be contorted.

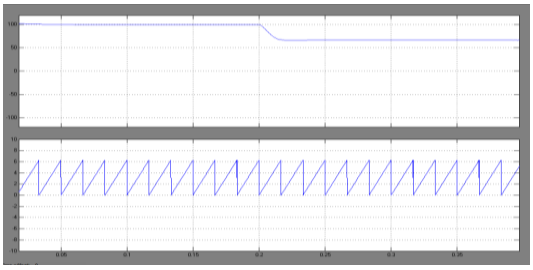
VI. SIMMULATION RESULTS



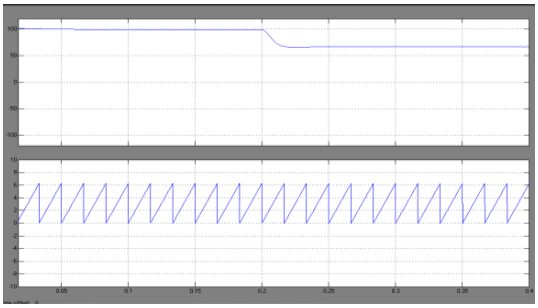
System Voltage under Three Phase Fault (LLLG) for DSOGI-PLL, DDSRF-PLL and 3phEPLL



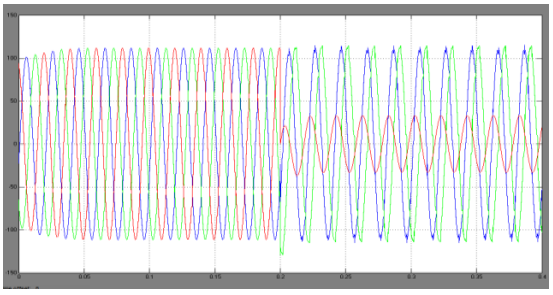
Voltage magnitude and Theta of the system by using DSOGI-PLL under three phase fault



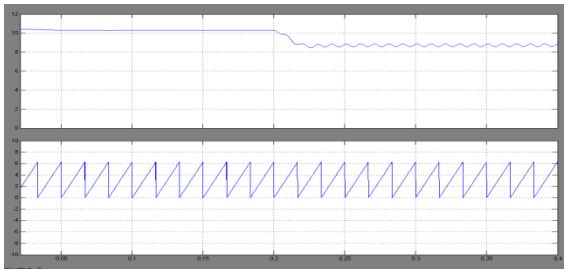
Voltage magnitude and Theta of the system by using DDSRF-PLL under three fault



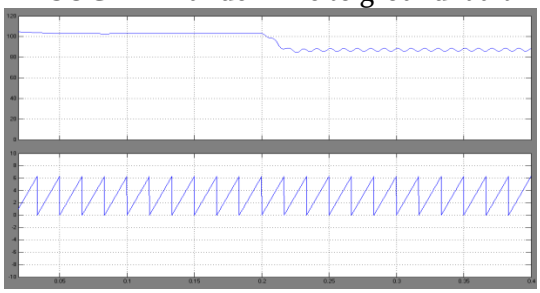
Voltage magnitude and Theta of the system by using 3phEPLL under three fault



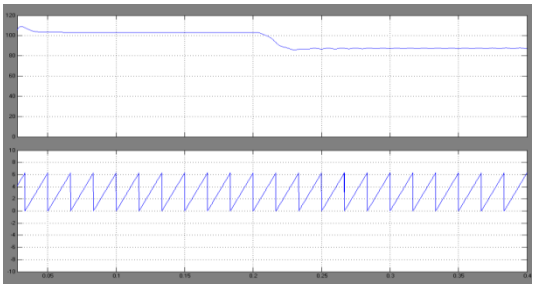
System voltage under Lineto Ground Fault for DSOGI-PLL, DDSRF-PLL and 3phEPLL (case1)



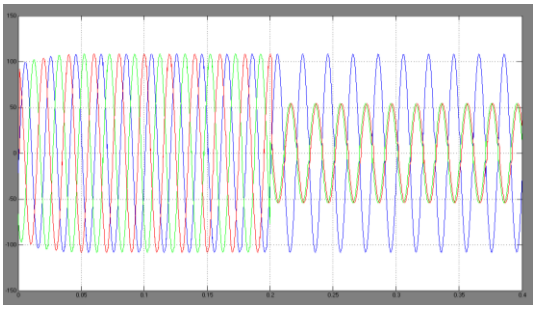
Voltage magnitude and Theta of the system by using DSOGI-PLL under Line to ground fault



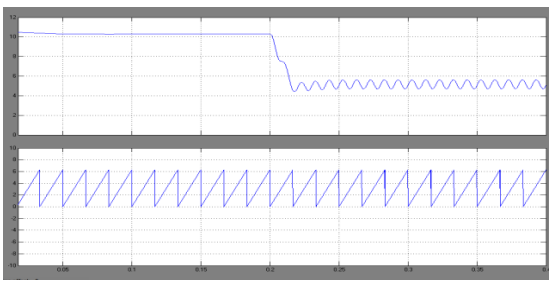
Voltage magnitude and Theta of the system by using DDSRF-PLL under Line to ground fault



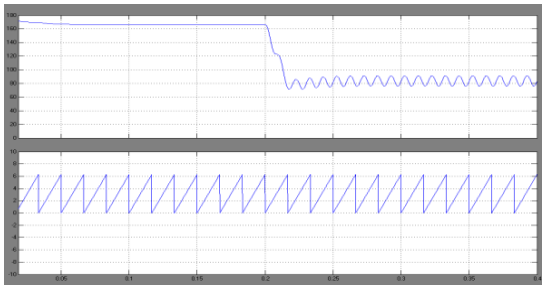
Voltage magnitude and Theta of the system by using 3phEPLL under Line to ground fault



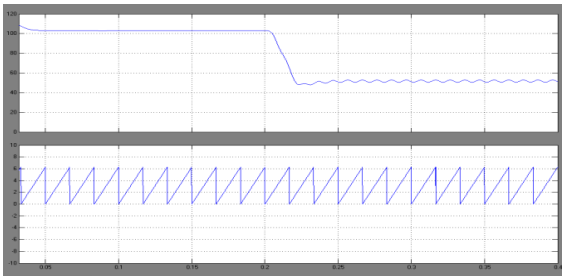
System voltage under Line to Line faultfor DSOGI-PLL, DDSRF-PLL and 3phEPLL



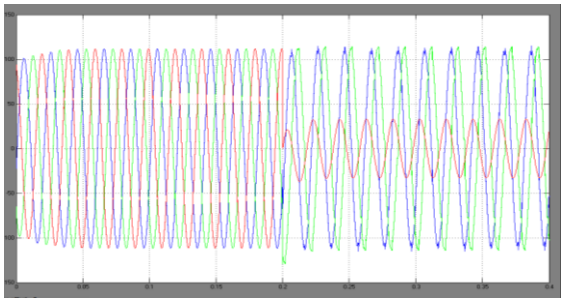
Voltage magnitude and Theta of the system by using DSOGI-PLL under Line to Line fault



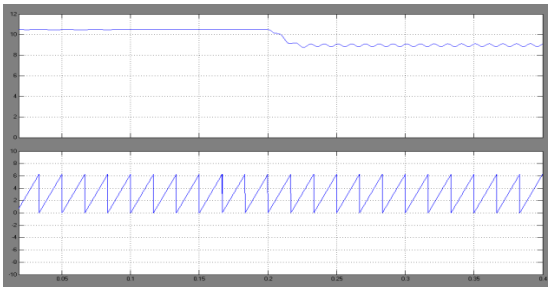
Voltage magnitude and Theta of the system by using DDSRF-PLL under Line to Line fault



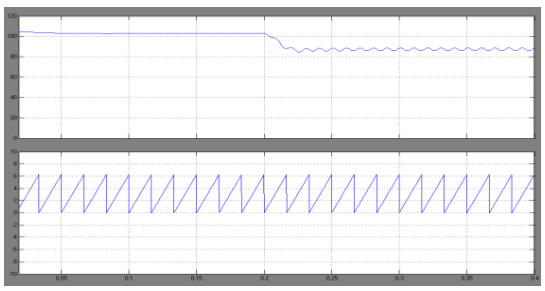
Voltage magnitude and Theta of the system by using 3phEPLL under Line to Line fault



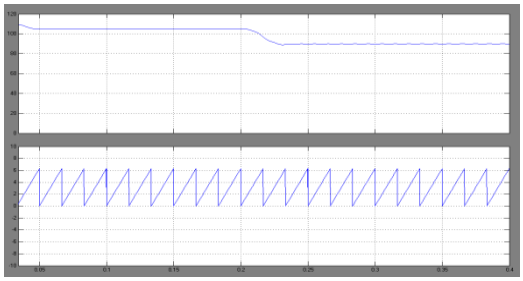
System Voltage under Phase to Ground Fault for DSOGI-PLL, DDSRF-PLL and 3phEPLL (case2)



Voltage magnitude and Theta of the system by using DSOGI-PLL under Line to ground fault

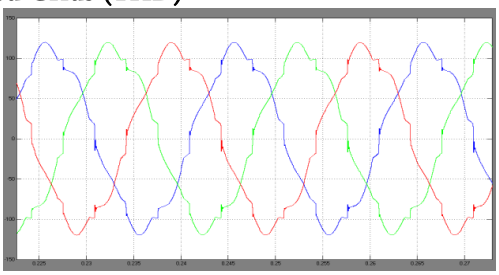


Voltage magnitude and Theta of the system by using DDSRF-PLL under Line to ground fault

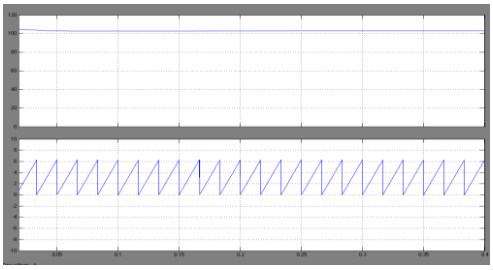


Voltage magnitude and Theta of the system by using 3phEPLL under Line to ground fault

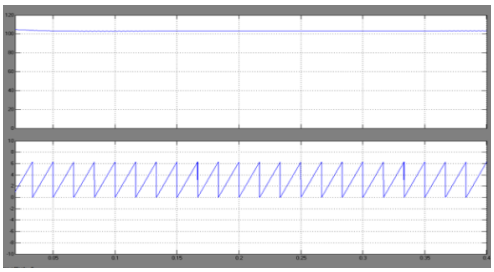
Polluted Grids (THD)



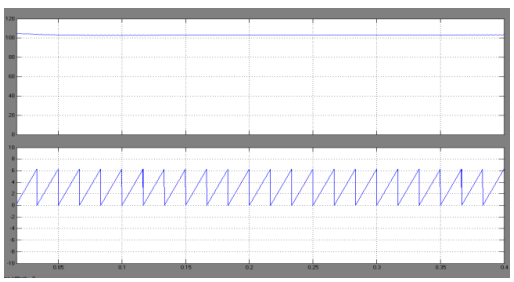
System voltage under polluted grid condition for DSOGI-PLL, DDSRF-PLL and 3phEPLL



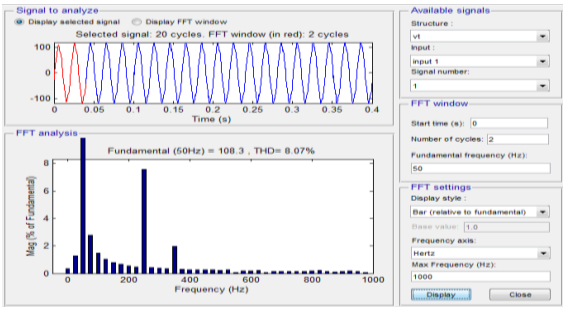
Voltage magnitude and Theta of the system by using DSOGI-PLL under Polluted Grid



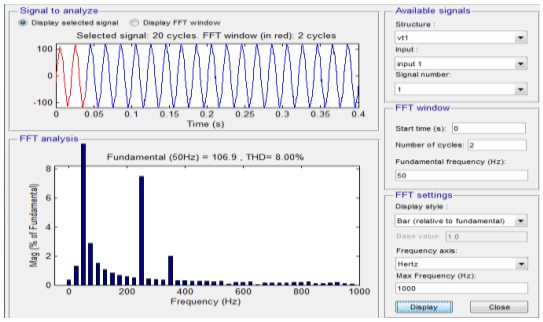
Voltage magnitude and Theta of the system by using DDSRF-PLL under Polluted Grid



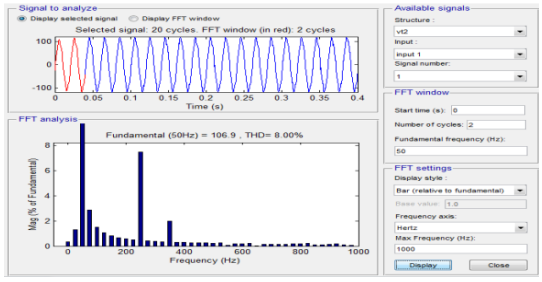
Voltage magnitude and Theta of the system by using 3phEPLL under Polluted Grid



Total Harmonic Distraction (THD) of polluted grid in DSOGI-PLL

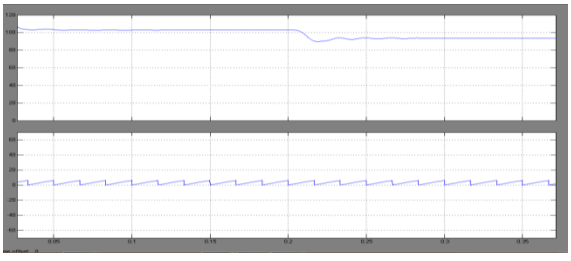


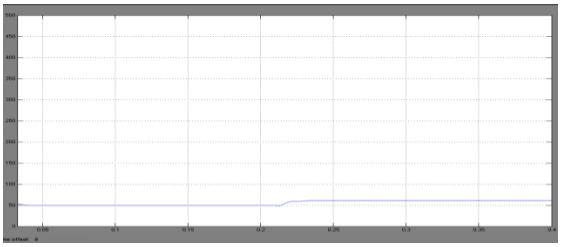
Total Harmonic Distraction (THD) of polluted grid in DDSRF-PLL



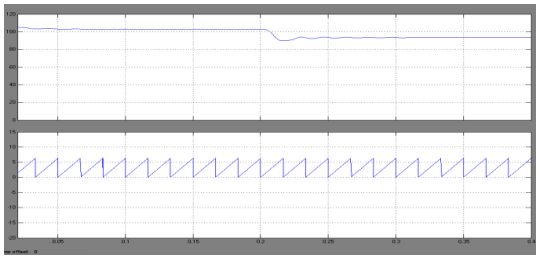
Total Harmonic Distraction (THD) of polluted grid in 3phEPLL

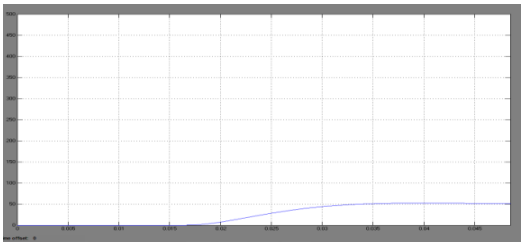
Frequency Changes (50–60 Hz)



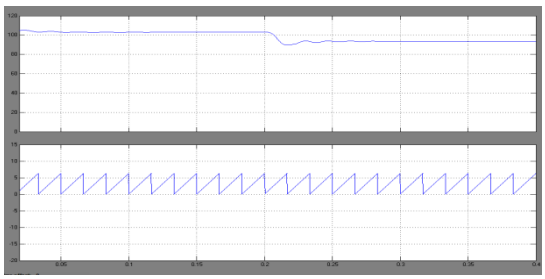


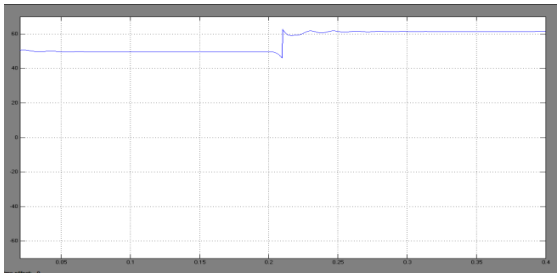
Amplitude, phase (rad), and frequency detection for the DSOGI PLL





Amplitude, phase (rad), and frequency detection for the DDSRF PLL





Amplitude, phase (rad), and frequency detection for the 3phEPLL

VII. CONCLUSION

This paper concentrated on grid fault conditions and synchronized the voltage magnitudes and angles by using fuzzy logic controller based PLL's. In existing method we have DDSRF PLL, DSOGI PLL and 3phEPLL by using these PLL's we achieve the synchronized voltage magnitudes and angles. But using these PLL's we get some harmonics in voltage of the grid so to limit and increase the speed of the system response we go for fuzzy logic controller based PLL's. By incorporated these PLL's with fuzzy logic controller we get low total harmonic distortion and

Speed of the system is fast compared to existing method.

VIII. REFERENCES

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