© 2018 IJSRSET | Volume 4 | Issue 1 | Print ISSN: 2395-1990 | Online ISSN : 2394-4099
Themed Section : Engineering and Technology

Implementation of an Efficient Reverse Compressor Multiplier and Adder Based MAC Architecture

K. Sreenath[1], H. Chandrasekhar[2]
[1]Mtech Student, Department of ECE, VemuInstitute of Technical Education,Tirupathi, India
[2]Associate Professor, Department of ECE, Vemu Institute of Technical Education,Tirupathi, India

ABSTRACT

Power dissipation is recognized as a critical parameter in modern VLSI design field. To satisfy MOORE'S law and to produce consumer electronics goods with more backup and less weight, low power VLSI design is necessary. High speed and low power Multiplier-Accumulator (MAC) units are required for applications of digital signal processing like Fast Fourier Transform, Finite Impulse Response filters, convolution etc.The proposed MAC uses multiplier with reverse compressor design multiplier and adders as primitive building blocks for efficient application. Further, the Verilog-HDL coding of MAC architecture and their implementation by Xilinx ISE 14.3 SynthesisTool. The proposed reverse compressor multiplier and adder based architecture used to be applied to MAC unit and in comparison to the previous design MAC unit and verified that the proposed architecture have reduce interms of delay.

Keywords –Multiply Accumulate Compressor, Reversible Gates, Adder.

I. INTRODUCTION

The increasing demand for portable systems and the need to limit power consumption and heat dissipation in very-high density chips have led to rapid developments in low-power design during the recent times. The battery lifetime is also a concern on the overall power consumption of the portable system.

Hence, reducing the power dissipation of integrated circuits through design improvements is a major Challenge in portable systems design. The need for low-power design is also an issue in high-performance digital systems, like microprocessors, digital signal processors (DSPs) and other applications. In digital VLSI circuits, computation is the critical part and it decides the power consumption and operating speed of the designs. For computations arithmetic circuits involves adders and multipliers; which are the most copiously used components. Digital signal processors performing filtering, convolution and etc, relies on the efficient implementation of these adder, multiplier and MAC Arithmetic units. Low power compressor architecture is proposed in this brief to reduce the power consumption of the MAC architecture since the presence of more number of compressors. The impact of the circuit design level or the data path optimizations is addressed at the MAC level for DSP applications. In MAC, additionally the carry propagate addition involved in multiplier and accumulate stages are merged to exploit and increase the number of compressors in the MAC architectures. Designs were illustrated in ASIC and FPGA domains as per the standard design methodology.

II. CONVENTIONAL COMPRESSOR ALGORITHM

Multipliers require high amount of power and delay during the partial products addition. At this stage,

most of the multipliers are designed with different kind of adders that are capable to add two/three or at most 4 bits by using 4-2 compressors. For higher order multiplications, a huge number of adders or compressors are used to perform the partial product addition. We have minimized the number of adders by introducing different compressors.

The conventional 4-2 compressor structure actually compresses five partial product bits into three. The architecture can be implemented with two stages of full adder (FA) connected in series as shown in Figure 1. The outputs of 4-2 compressor consist of one bit in position j and two bits in position (j + 1). This straight forward approach has four XOR gate delays.

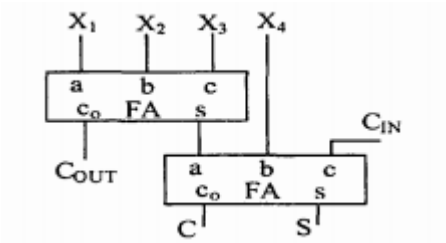


Figure 1. Conventional 4-2 compressor

This implementation is better and the delay is that of three XOR gates delays. With the similar logic 5-2 compressor.The problems of this kind of conventional compressor are:

(i)The uneven delay profile of the outputs arriving from different input paths tends to generate a lot of glitches.

(ii) Compressors do the simple operation of addition that adds more number of bits at a time. But the conventional 4-2 compressors require one more half adder of which two inputs are 'COUT' and 'C' (shown in Figure 2), to produce the final addition result. Example: if X1=X2=X3=X4=1 and CIN =0 (in Figure 1) then the addition result be four i.e 100 but the conventional architecture produces COUT=1, C=1 and S=0. Now if COUT and C fed to a half adder then it produces the final result in exact form as shown in Figure 2.

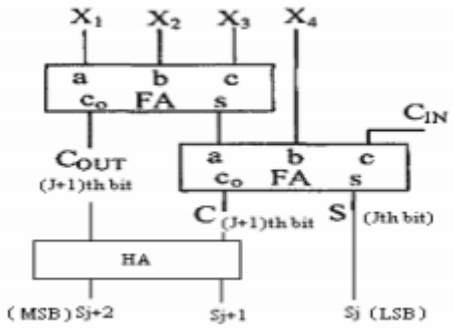


Figure 2. Modified 4-2 compressor

(iii) For 4-2 compressor, a half adder is required but for 5-2 compressor a full adder is required because a 5-2 compressor is implemented by series connection of three full adders, that generates three carry output bits in position 'j+1' and one sum bit in position 'j', shown in Figure 3. Thus this conventional logic not only increases the critical path delay but also increases the number of output bits.

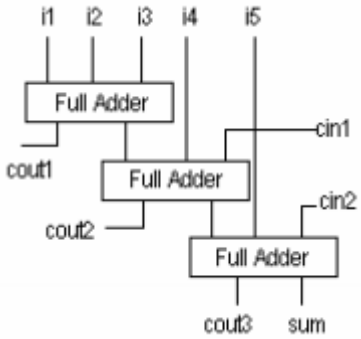


Figure 3. Conventional 5-2 compressor

As the weightage of sum bit is '1' and the weightage of carry bits is '2' of conventional compressors, so the results that produced by those compressors are correct but not in proper binary form. When these conventional compressors are used in multiplier to achieve high speed then one half adder/full adder is required per compressor to process those carry bits.

III. REVERSE LOGIC COMPRESSOR

Reversible Logic:

Reversible logic plays an important role in recentyears due to its ability to reduce the power dissipation Which is the main requirement in Low power VLSIdesign. It is based on the Quantum computingusing a physical mechanism that

isthermodynamically as well as logically reversible. According to Landauer's research the amount ofenergy dissipated for every irreversible bit operation is at least kTln2 joules, where k=1.3806505*$10^{-23}m^2kg$-2K-1(joule/Kelvin-1).A circuit is said to bereversible if the input vector can be uniquelyrecovered from the output vector and there exist oneto-one correspondence between its input and outputs. A basic 4x4 input TSG gateis taken and used as Full Adder and the same is used to build 4:2 compressors. Basic gatesused in this paper are Peres gates, TSG gates.

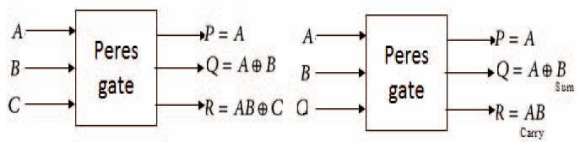


Figure 4. 3x3 Peres Gate as And gate/Half Adder

In Figure 4 Peres gate is used as AND gate togenerate Partial Products by making input c zero and
the same can be used as Half adder with Output Q as Sum and R as Carry output.

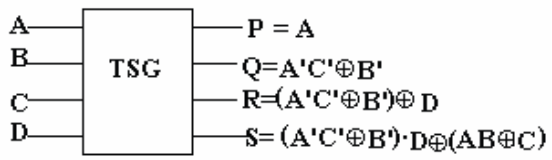


Figure 5a. Basic TSG gate

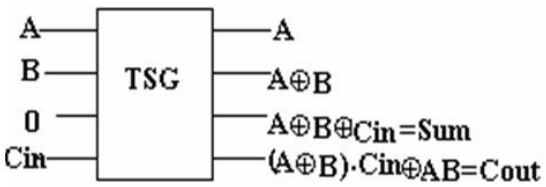


Figure 5b. TSG gate as Full Adder

Figure 5a describes an 4 input TSG reversible logic gate with 4 outputs as shown above and by making input C as '0' it acts as Full Adder.

Compressors:

Compressors are used to implement arithmetic and digital signal processing architectures for high performance applications. These are used especially in adder structures to reduce the complexity and time delay. These are also used in Multiplier architectures to add all partial products and for final addition. In multiplier architectures the main source of power, delay and area consumption are from how these partial products are accumulated. These compressors are used to reduce time delay and increase its speed for specific architecture. Generally compressors reduce N-input bits to a single sum bit of equal weight to that of the inputs and carry out bit. In usage we had 3:2, 4:2, 5:2, etc. In this paper we used only 4:2 compressors with four inputs (x1, x2, x3, x4) and two outputs sum and carry. The 4:2 compressors receive an input Cin from the preceding module of one binary bit order lower in significance, and produce an output Cout to the next compressor module of higher significance as shown in figure 6. Besides, to accelerate the carry save summation of the partial products, it is imperative that the output, Cout be independent of the input Cin.

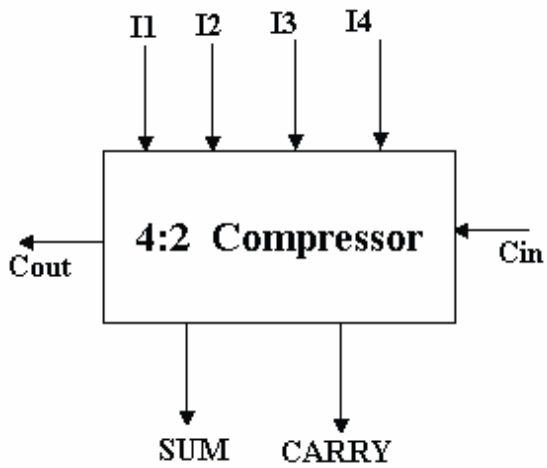


Figure 6. 4:2 Compressors

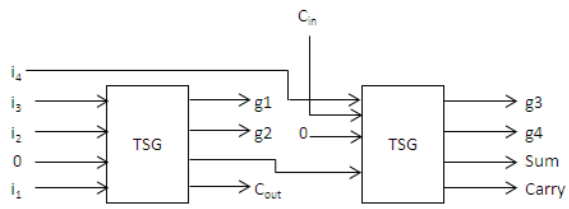


Figure 7. Reversible 4:2 Compressor using TSG gates

IV. THE PROPOSED MAC UNIT

The multiply-accumulate unit computes the product of two numbers and adds that product to an accumulator. The MAC unit, consisting of a multiplier followed by an adder and an accumulator register which stores the result when clocked. The output of the register is fed back to one input of the adder, so that on each clock the output of the multiplier is added to the register. Combinational multipliers require a large amount of logic, but can compute a product much more quickly than the method of shifting and adding typical of earlier computers. The MAC circuit must check for overflow, which might happen when the number of MAC operations is large. Overflow in a signed adder occurs when two operands with the same sign produce a result with a different sign.

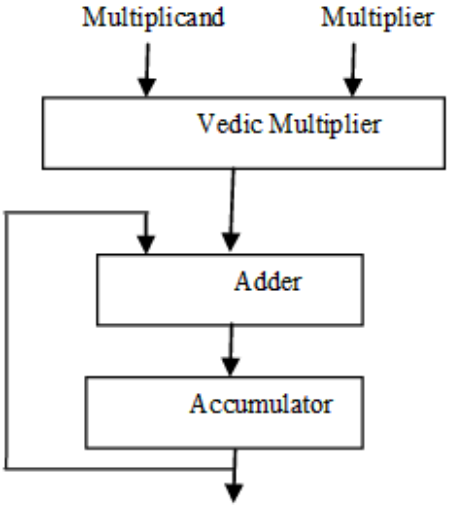


Figure 8. Architecture of MAC unit.

Figure 8 shows the architecture of the proposed MAC unit. The two input 8 bit operand to the MAC unit are X[7:0] and Y[7:0]. The 32 bit output from MAC unit is Q[16:0]. The proposed design uses one 8x8 Vedic multiplier using „Urdhva Tiryagbhyam" algorithm 16 bit accumulator using carry save adder, and one 16 bit register. Vedic multiplier can increase the MAC unit design speed. Carry save adder is used as anaccumulator in this design. The Vedic multiplier and carry save adder in the MAC unit design enhance the MAC unit speed so as to gain better system performance. The product of Xi X Yi is fed back into the 16-bit Carry Save Adder and then added again with the next product Xi x Yi. This MAC unit is capable ofmultiplying and adding with previous product consecutively (Output = Σ Xi Yi).

A. Proposed Multiplier

Basically Multiplier consists of 3 stages
1. Partial Product Generation, 2.Partial Product Addition 3. Final Product Addition.

Multiplier essentially consists of 2 operands a multiplicand "Y" and Multiplier "X" and produces a product. In stage 1 each bit is multiplied to produce Partial products. Stage 2 is an important stage where all partial products gets added using various adder structures in a tree like fashion. Stage 3 is used to generate the Final Product. Our proposed multiplier uses Peres gates to generate partial products, 4:2 TSG based compressors to add partial products and the same is compared with conventional Multipliers.

Partial Product Generation:

To generate Partial Products we used peres gates because quantum cost per gate is less when compared to other reversible gates.Inliteratureto generate partial products they used Fredkin gates or Peres gates[5]. Quantum Cost for Fredkin gate is 5 but for Peres gate it is 4.

Partial Product Addition:

This paper combines two different technologies like Compressor logics and Reversible Logics for adding Partial Products on Vedic Multiplier and it was observed that number of stages and number of gates used reduces when compared to other existing structures.

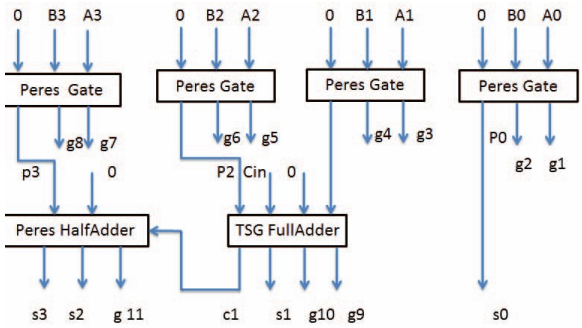


Figure 9. 2x2 bit Reversible Vedic Multiplier

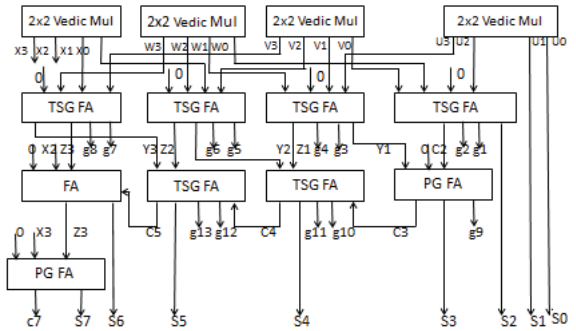


Figure 10. 4x4 bit Reversible Vedic Multiplier using 2x2 bit Vedic Multipliers

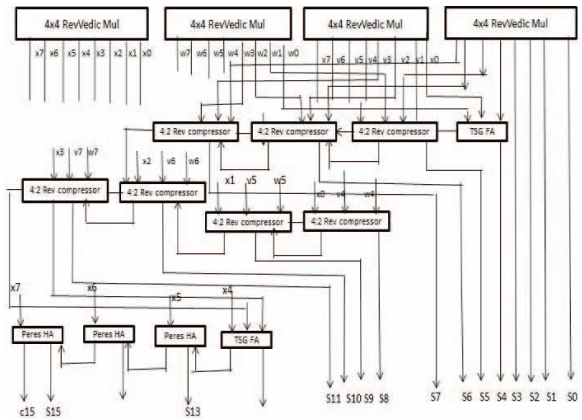


Figure 11. 8x8 bit multiplier using 4x4 bit Multipliers

Final Product Summation:

In the proposed method final adders are not requiredthe output of the compressors itself gives FinalProduct. Hence we can say that complexity of thecircuit reduces when compare to conventional Multipliers.

B. Proposed adder

The Carry Save Adder (CSA) is a type of DigitalAdder, used to compute the sum of three or morenumber of bits in binary form. CSA gives lesspropagation delay and the Glitching problem in RCAis also avoided. Since, the Representation of 8 bitCSA is shown in Figure 12.

Here, we compute the sum of two 8 bit binary numbers so 8 half adders at the first stage is required instead of 8 full adders. Since, we add bits of two binary numbers only. If, P and Q are two 8 bit numbers then it produces the partial products and carry Si and Ci respectively. Where,

Si = Pi Qi

Ci = Pi .Qi

However, a CSA Produces all the output values inparallel. So that, the computation time isReducedcompared to RCA. Also, Parallel in Parallel out(PIPO) is used in Accumulator Stage.

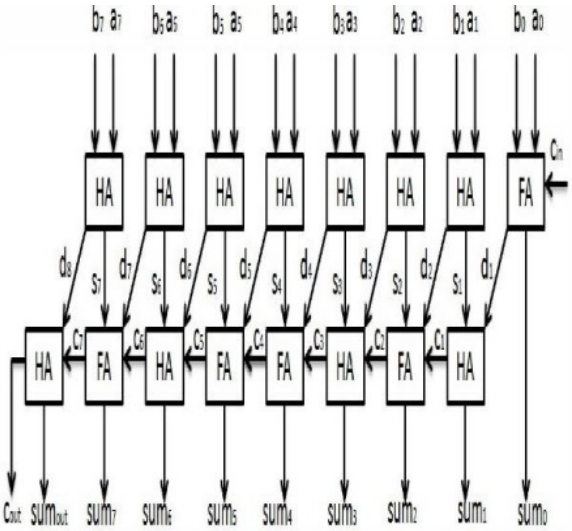


Figure 12: A Typical 8 bit Carry Save Adder

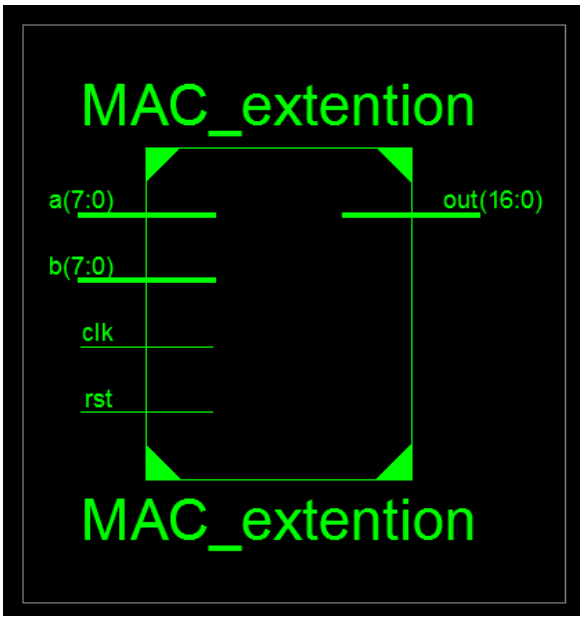
V. RESULTS

The MAC is designed using verilog HDL, Simulation and synthesis results are carried out using Xilinx ISE 14.3. Hence the proposed MAC architecture is found most efficient in terms of speed and delay.

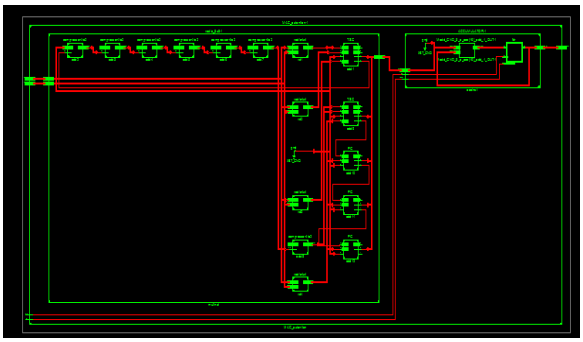
Table 1. comparison results of proposed and existing MAC architectures

parameter	MAC using Compressor based Wallace tree	MAC using Compressor based Vedic	MAC using Compressor based reverse Vedic
Number of slice LUT's	139	123	112
Number of bonded IOBs	35	35	35
Delay	7.756ns	7.079ns	6.669ns

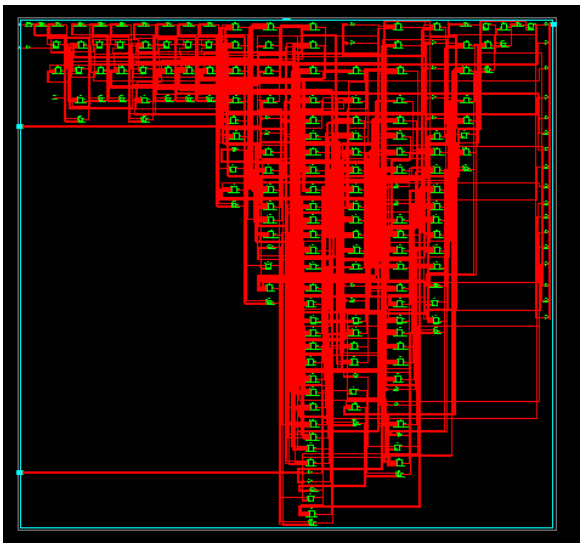
Block diagram



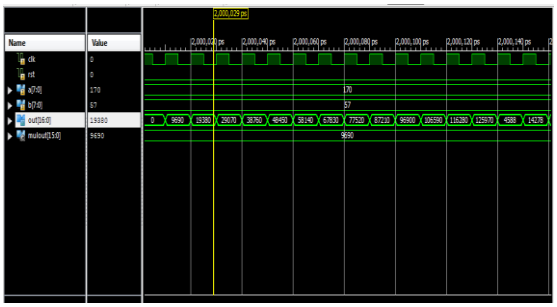
RTL schematic



Technology schematic



Simulation results



VI. CONCLUSION

A High Performance MAC Unit is designed and implemented using reversecompressor based Vedic Multiplier and Carry Save Adder. Thus we propose a new high speed, low power and area efficient MAC architectures which will be an improvement over the existing architecture by replacing conventional 4:2 compressor with proposed 4:2 compressor. The proposed architectures have yielded better efficient results in terms of delay, area and speed.

VII. REFERENCES

[1]. Chang, Chip-Hong, JiangminGu, and Mingyan Zhang."Ultra low-voltage low-power CMOS 4-2 and 5-2compressors for fast arithmetic circuits." Circuits and Systems I: Regular Papers, IEEE Transactions on 51.10 (2004): 1985-1997.

[2]. Tung Thanh Hoang; Sjalander, M.; Larsson-Edefors, P., "AHigh-Speed, Energy-Efficient Two-Cycle Multiply-Accumulate (MAC) Architecture and Its ApplicationtoaDouble-Throughput MAC Unit," Circuits and Systems I:Regular Papers, IEEE Transactions on , vol.57, no.12, pp.3073,3081, Dec. 2010.

[3]. Chen Ping-hua; Zhao Juan, "High-speed Parallel 32×32-b Multiplier Using a Radix-16 Booth Encoder," IntelligentInformation Technology Application Workshops, 2009.IITAW '09. Third International Symposium on , vol., no., pp.406,409, 21-22 Nov. 2009

[4]. Kiwon Choi; Minkyu Song, "Design of a high performance 32×32-bit multiplier with a novel sign select Booth encoder," Circuits and Systems, 2001. ISCAS 2001. The2001 IEEE International Symposium on , vol.2, no., pp.701,704 vol. 2, 6-9 May 2001.

[5]. Rajput, R.P.; Swamy, M.N.S., "High Speed Modified Booth Encoder Multiplier for Signed and Unsigned Numbers," Computer Modelling and Simulation (UKSim),2012 UKSim 14th International Conference on , vol., no., pp.649,654, 28-30 March 2012.

[6]. Yangbo Wu; Weijiang Zhang; Jianping Hu, "Adiabatic 4-2 compressors for low-power multiplier," Circuits andSystems, 2005. 48th Midwest Symposium on , vol., no., pp.1473,1476 Vol. 2, 7-10 Aug. 2005.

[7]. Jaina, D.; Sethi, K.; Panda, R., "Vedic Mathematics Based Multiply Accumulate Unit," Computational Intelligenceand Communication Networks (CICN), 2011 InternationalConference on, vol., no., pp.754,757, 7-9 Oct. 2011.

[8]. Aliparast, Peiman, Ziaadin D. Koozehkanani, and FarhadNazari. "An Ultra High Speed Digital 4-2 Compressor in 65-nm CMOS." International Journal of Computer Theory& Engineering 5.4 (2013).

[9]. N. Weste and David Harris, "CMOS VLSI Design- A Circuits & System Perspective", Pearson Education, 2008.

[10]. ChandraMohan U, "Low Power Area Efficient Digital Counters", Proceedings of the 7th VLSI Design and Test Workshops, VDAT, August 2003.

[11]. Narendra C P & Ravi K M Kumar, "Efficient Comparator based Sum of Absolute Differences Architecture for Digital Image Processing Applications", Foundation of Computer Science, New York, USA, International Journal ofComputer Applications, 96(4):17-24, June 2014.

[12]. D. Radhakrishnan A.P. PreethySingapore "Low Power CMOS Pass Logic 4-2 Compressor for High-SpeedMultiplication",circuits and systems, 2000, Proceedings of the 43rdIEEE Midwest Symposium, pages 1296-1298.

[13]. S. F. Hsiao, M.R. Jiang and J.S. Yeh, "Design of high-speedlow-power 3-2 counter and 4-2 compressor for fast multipliers,"Electronics Letters, vol. 34, no. 4, pp. 341-342, Feb. 1998

[14]. M.Margala and N.G. Durdle, "Low-Power Low-Voltage 4-2Compressors for VLSI Applications," Proc. Workshop on LowPower Design, 1999.

[15]. S.Veeramachanemi, K.Krishna, L.Avinash, S.R.Puppola,M.B.Srinivas, "Novel architectures for high speed and lowpower3-2, 4-2 and 5-2 compressors", IEEE Proc .Of VLSID'07,pp.324-329,2007.

[16]. HimanshuThapliyal and M.B Srinivas "Novel ReversibleMultiplier Architecture Using Reversible TSG Gate"ComputerSystems & Applications, 2006 IEEE International Conference,pages 100-103.