© 2018 IJSRSET | Volume 4 | Issue 1 | Print ISSN: 2395-1990 | Online ISSN : 2394-4099
Themed Section : Engineering and Technology

A Novel Design and Implementation of Dual Use of Power Lines For Design-For-Testability by using LOC and LOS Technique

Mahalakshmi[1] , R. Mallikarjuna Reddy[2]

[1]M. Tech Student, Department of ECE, Vemu Institute of Technical Education, Tirupathi, India
[2]Assistant Professor, Department of ECE, Vemu Institute of Technical Education, Tirupathi, India

ABSTRACT

The PLC is one in which the power pins and the power distribution networks of ICs are used for data communication as well as power delivery. PLC is used in order to reduce the number of input pins that an IC needs to couple the test data signals to each and every node. Hence to extract the test data signals from this power lines, so many receivers are in need at each and every nodes of the ICs or at places where we have to apply the test. For this purpose, PLC receivers are already designed. But all of them consume very high power. So, in this paper Launch On Capture (LOC) And Launch On Shift (LOS) a power efficient CMOS PLC receiver for the same purpose in 180 nm CMOS technology under a supply voltage of 1.8 V is designed with the help of Tanner tool. To achieve this much extreme low power, so many CMOS low power technics are successfully employed like the stacking method, resistor less approach
Keywords : Design-for-testability (DFT), PLC at ICs, PLC receiver, power line communications (PLCs), LOC and LOS.

I. INTRODUCTION

Today's VLSI technology is advancing in such a way that the designers can incorporate a large number of functions inside a chip. Microprocessors are one of the best examples for this. Day by day the size of ICs reduces and the operations it can perform are increasing. So many challenges still exist such as, the need of proper provision for the thermally generated heat removal, the number of the input output pins that an IC needs, proper power supply injection etc., due to which there exists limits on incorporating functions inside ICs. Also routing inside the IC too has a major role in it. There should also be the provisions in ICs like sensors to detect what is happening inside each and every point and if anything happens wrongly, the normal state have to be recovered. Even though the increase in system complexity is an advantage in the sense that the size of ICs can be reduced, with that there should be new inventions for proper data passage inside the same. The power line communication aspect presented in this paper is one of such methods.

In power line communication, it efficiently uses the power distribution networks inside ICs since they are the only components that reach each and every node. So if there have a provision to pass the test data, which are used for fault diagnosis, scan design etc. to whichever areas we need to apply the test that will be an attractive way of communication in ICs, So that the routing overhead inside the ICs to pass these testing data can be intelligently avoided. So in PLC, the power distribution networks are used for power delivery and also data communication. The test data are superimposed on the power signal and are transmitted through the power distribution networks of ICs rather than the separately allotted routing

paths. Also the number of power pins can be reduced since there is no need to carry the test data through the input pins. Of course, adopting such a power line communication always has to overcome the extreme noise level at the power lines. So there should be effective methods to overcome the same. Essentially there is the need of receivers at each and every node to extract these data signals efficiently from the power lines. Many variants of the same already exist, but a power efficient design is not yet met. Why the receiver should be power efficient is because, otherwise if each unit of receiver consumes such huge power, the overall power consumption of the entire chip will increase by a large value, which is hard to afford.

In this paper, such a power efficient CMOS PLC receiver is designed in 180nm CMOS technology under the supply voltage of 1.8 V. The methods that are incorporated to achieve the power reduction are very simple to understand and realize. With each new generation of deep submicrometer vlsi technologies, testing, debugging, and diagnosis of vlsi circuits become more difficult and expensive. In addition to higher circuit complexity for a deeper submicrometer technology, larger process variations, greater interconnection delays relative to transistor switching time, and larger leakage current also contribute to make the testing more challenging. It is a general consensus among test engineers That accessibility, i.e., controllability and observability, to internal nodes for both 2-d and 3-d ics is essential to address the testing problems. Conventional design-for-testability (dft) methods, such as scan design, provide dedicated or shared signal paths between i/o pins and internal nodes. As the circuit complexity increases, the number of internal nodes increases proportionally, and individual internal nodes are less accessible due to the limited Number of available i/o pins. One promising approach to provide ubiquitous accessibility to internal nodes is the dual use of power pins and power distribution networks (PDNs) for data communications as well as power delivery, which is essentially power line communications (PLCs) at the IC level. The PLC at the IC level would be useful for low data rate communications such as scan design, system debugging, and fault diagnosis. The approach also eliminates the need to route a data path from the node to an external data pin. To the best of our knowledge, PLC in an IC environment was exclusively reported in and . The conceptual PLC system in an IC environment considered for our research. A test instrument sends the data superimposed on the supply voltage of a system board. The signal travels through a power pin(s), the power planes of a package, and the PDN, and then it reaches at the intended node(s). The PLC receiver embedded inside a chip extracts the data from the power line. All the previous PLC receivers designed in report only the simulation results. This paper presents a PLC receiver, whose main design objective is robust operation under supply voltage variations and droops. The proposed PLC receiver was designed and fabricated in CMOS 0.18-μm technology with a supply voltage of 1.8 V.

II. PREVIOUS WORKS

PLC Receivers in Integrated Circuits

The proposed topic of the thesis research is to develop a PLC receiver in CMOS technology. A few of PLC receivers in CMOS were developed by Dr. Dong S. Ha's team. The PLC receivers demonstrate feasibility of power line communications in ICs. The PLC receiver proposed by Thirugnanam et al. in is composed of a sensing circuit, a differential amplifier with an offset cancellation, and a positive feedback latch. The offset cancellation, which removes the DC voltage of the signal, is based on a fixed bias voltage, and is sensitive to supply voltage fluctuations. The PLC receiver was designed in CMOS 0.18 um technology. The PLC receiver proposed by Chawla et al. in adopts a coherent detection for ultra wideband (UWB) data signals. It achieves a higher sensitivity than its predecessor owing to the coherent detection, but dissipates more power due to higher circuit complexity. Like its predecessor, the PLC receiver also relies on a fixed bias voltage to remove the DC

voltage from the signal and 4 hence suffers from the same shortcoming. The PLC receiver was designed in CMOS 0.18 μm technology initially, and was also developed in 0.13 μm CMOS technology later.

Thirugnanam PLC Receiver

The PLC receiver proposed by R. Thirugnanam in is shown in Figure . It consists of a sensing circuit, a differential amplifier, and a latch. The sensing circuit, which is simply a common source with diode connected load, detects the transmitted signal in the power line and shifts the DC level of the signal down. The output of the sensing circuit, which is single ended, is applied to a differential amplifier. One input of the differential amplifier is connected to a constant reference voltage, and the other input to the drains of M3 and M4 whose gates are connected to the clock signal. When the clock signal is low, the output of the sensing circuit is connected to the input of the differential amplifier, and the amplifier amplifies the sensed signal and compares it with the reference signal. When the clock is high, M3 is off and M4 is on. The amplifier is disconnected from the sensing circuit, and the M5 acts as diode with resistance 1/gm. The output of the differential amplifier is connected a latch, consisting of back-to back inverters. The latch converts the output of the differential amplifier to the supply rails, i.e., logic values. The transistor M9 enables the latch to sample at the falling edge.

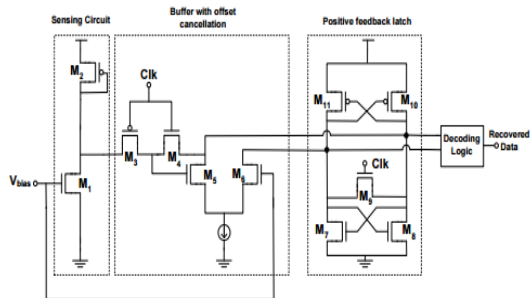


Figure 1: PLC receiver proposed by R. Thirugnanam

III. PROPOSED PLC RECEIVER

The proposed on-chip PLC receiver receives the data superimposed on power lines, and the data (such as scan test data) are sent from a test instrument. Therefore, the transmitter for the PLC receiver is an external instrument rather than the one on the same chip. The receiver was designed in CMOS 0.18-μm technology with a supply voltage of 1.8 V. It consists of three building blocks, and this section describes the design of each building block.

A. Block Diagram

A block diagram of the proposed PLC receiver is shown in Fig. The proposed PLC receiver consists of three blocks, each sharing the same supply voltage (VDD + $vdd(t)$). The first block is a level shifter, which lowers the dc level of the signal superimposed on the supply voltage. The level shifted signal is processed by the subsequent block, a signal extractor, which amplifies the signal and converts it to a differential signal. The logic restorer, which is a differential Schmitt trigger, recovers logic values from the differential signal. The design and operation of each block is explained below.

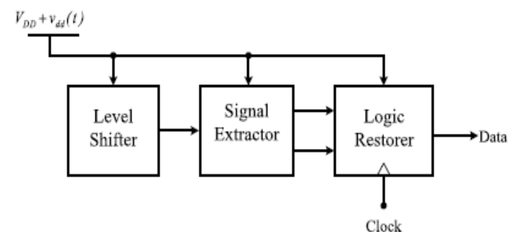


Figure 2: Block diagram of the proposed PLC receiver

B. Level Shifter

The level shifter shown in Fig. can be treated as a common source amplifier with diode-connected load as, in which the amplifier input is fixed to a bias voltage Vbias. The level shifter propagates the data signal $vdd(t)$ imposed on the supply voltage VDD to the output while lowering the dc voltage level of the signal to 0.5 VDD. To propagate the data signal superimposed on the supply voltage to the output, the output should be sensitive to supply voltage variations. In other words, contrary to a typical amplifier design, the power supply rejection ratio (PSRR) of the level shifter should be set to small.

The PSRR of the common source amplifier with the gate of M1 as the input is defined as the ratio of the voltage gain from the input to the voltage gain from the supply voltage

PSRR = Av/AVDD (1)

where Av is the small-signal voltage gain from the input (i.e., the gate of M1) to the output of the amplifier, and AVDD is the small-signal gain from the power supply to the output. Av is btained as

Av ≈ – gm1/gm2 (2)

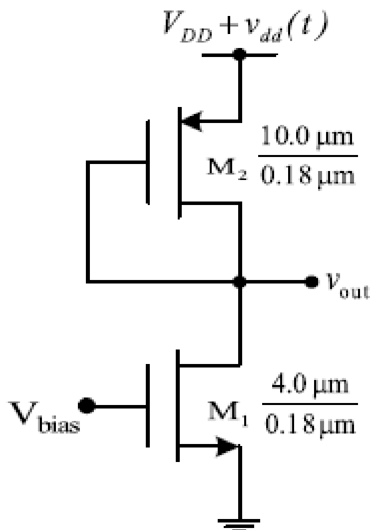


Figure 3: Level shifter.

where $gm1$ and $gm2$ are the transconductances of $M1$ and $M2$, respectively. $AVDD$ is obtained as in (3) and becomes 1 ignoring the channel length modulation.

$$A_{V_{DD}} = \frac{r_{o1}}{1/g_{m2} + r_{o1}} \approx 1. \quad (3)$$

Thus, the PSRR of a common source amplifier is expressed as

PSRR ≈ $-gm1/gm2$ (4)

The transconductance of a MOS transistor is

$$g_m = \mu C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{TH}). \quad (5)$$

By substituting (5) in (4), the PSRR becomes

$$\mathrm{PSRR} \approx \frac{\mu_n (W/L)_1 (V_{GS} - V_{TH})_1}{\mu_n (W/L)_2 (V_{GS} - V_{TH})_2}. \quad (6)$$

Equation (6) indicates that the PSRR can be lowered by setting $(W/L)1$ small, $(W/L)2$ large, the overdrive voltage of $M1$ small, and the overdrive voltage of $M2$ large. This means that the bias voltage and the W/L ratio of $M1$ should be set to small, while operating $M1$ in saturation. Since the desired dc voltage level at the output of the sensing circuit is 0.5 VDD, the condition sets the overdrive voltage of $M2$. A large W/L ratio for $M2$ increases the current ID, and so it is a compromise between low-power dissipation and low PSRR. The overdrive voltage ($VGS– VTH$) of $M1$ is set to a near minimal (= 0.08 V) for the proposed level shifter and that for $M2$ large (= 0.373 V). In addition, $(W/L)1$ is set relatively small (= 22.2), and $(W/L)2$ relatively large (= 55.6). The resultant PSRR for the level shifter is 1.3 (or 2.27 dB), which is small compared with a typical value of analog amplifiers ranging from 65 to 80 dB.

C. Signal Extractor

The input signal of the signal extractor is the data signal offset with 0.5 VDD, and the signal extractor amplifies the data signal while removing the dc offset voltage. The signal extractor shown in below, is a differential amplifier, in which one input is connected to an RC low-pass filter. The low-pass filter intends to extract the dc value of the signal. The differential amplifier rejects the common-mode signal of the two inputs or the dc value. It also converts a single-ended input into a differential output pair.

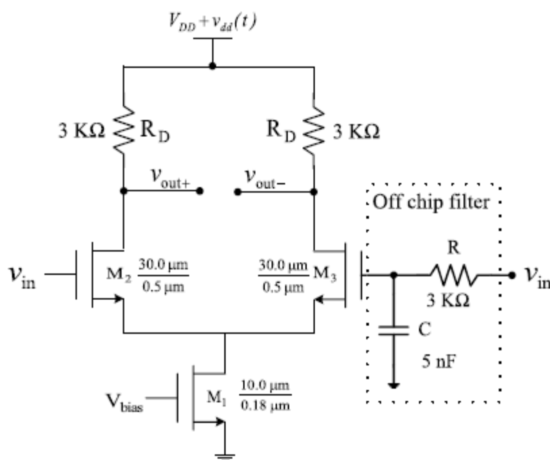


Figure 4: Signal extractor

The voltage gain of the differential amplifier is expressed as

$$Av = -gm2{,}3\ RD \qquad (7)$$

where gm2 and gm3 are equal to μCox(W/L)(VGS–VTH).

D. Logic Restorer

The logic restorer translates the data in the form of an analog differential signal into logic values. It is based on the differential Schmitt trigger presented in and is shown Fig. . A key aspect of the Schmitt trigger is the hysteresis generated through the regenerative feedback circuit, specifically a cross-coupled inverter pair. When a new data signal is applied to the logic restorer, the clock is turned from low to high and turns OFF *M*5 and *M*6. It reduces the current supplied to the differential amplifier, which results in a smaller gap between the high and the low threshold voltages. The cross-coupled inverter pair settles to a high or low state, and hence the output of the logic restorer. Then, the clock signal becomes low, and *M*5 and *M*6 are turned ON. The gap between the two threshold voltages becomes wider, which increases the immunity to noise and disturbances.

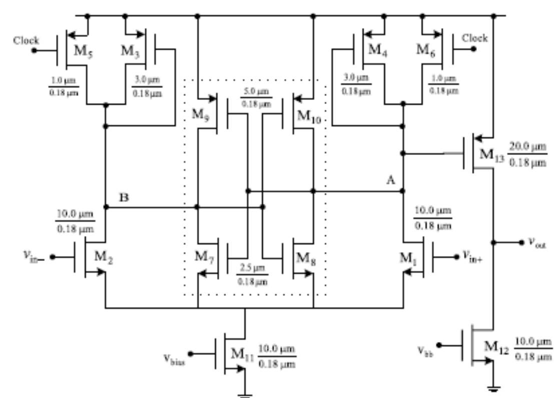


Figure 5: Differential Schmitt trigger

E. Scalability and Location of the PLC Receiver

The level shifter is a rather unique block and specific for our PLC receiver. The level shifter has two transistors in cascode, so it can be scaled to lower supply voltages easily. Consider that the resistive load for the signal extractor is replaced by a current source. Then, both the signal extractor and the Schmitt trigger have three transistors in cascode, which are common for analog circuits. Therefore, they would scale along with other analog circuits. It should be noted that the two blocks are commonly used building blocks for analog circuits, and have been migrated to the advanced processing technologies with lower supply voltages. When compared with digital circuits, analog circuits do not scale well in the supply voltage. Therefore, the proposed PLC receiver, or its variations, may not be applicable for extremely low supply voltages such as those for low-power digital circuits operating at very low supply voltages.

The physical location of a PLC receiver on the chip affects its performance. Obviously, a PLC receiver located closer to the source, i.e., the power pin through which the data signal is applied, performs better. The cost is possibly a long signal path from the receiver to the target logic block to which the data are applied. Impact on the signal quality at various locations inside a chip was investigated in , and simulation results for a ball grid array package are reported.

IV. Launch On Capture (LOC) And Launch On Shift (LOS)

Main transition fault ATPG methodologies are Launch on Capture and Launch on Shift (also known as broadside-load and skewed-load respectively). They both launch transition at the input of combinational block in different way for the same fault detection. As shown in figure-6, two vectors V1 and V2 are used to perform transition delay fault testing. Here figure-6(a) describes the LOC waveform. As illustrated, last shift of scan chain initialize the inputs of combinational block and first functional clock is used to launch transition in the combination block (here scan enable signal is de-asserted after V1).

Second functional clock would captures the propagated transition at the output. Then scan enable signal would asserted. Example, for scan chain having N scan-length, in LOC, first vector of N bit is loaded in to scan chain by N slow clock. Then two fast clock (functional clock) are used to launch and capture transition into and from the combinational block. Again scan chain unloads with N slow clocks. Here scan enable signal transit from high to low after last shift of loading process. So, launch clock always occur in function mode and launching of transition would be along function path.

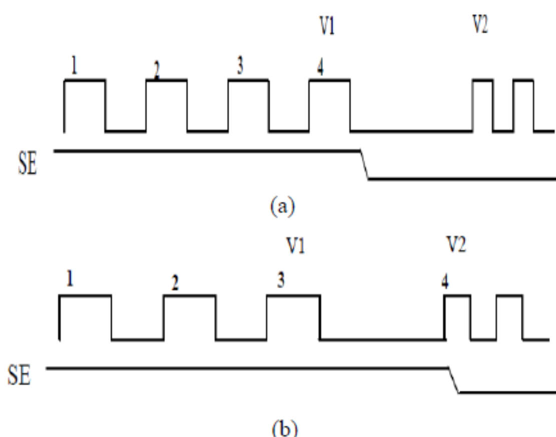


Figure-6 (a): LOC Waveform (b) LOS Waveform

A. Proposed architecture for LOC based logic restorer

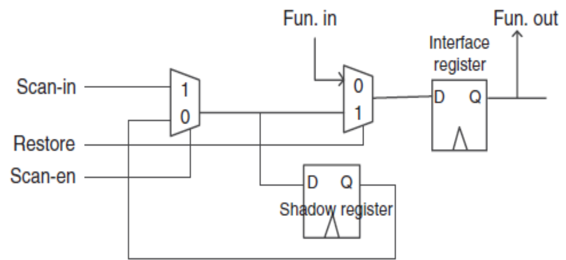


Figure 7: Architecture for LOC

B. Proposed architecture for LOS based logic restorer

As the LOS scheme launches transitions via a shift operation, a set of test patterns is valid as long as the final scan cell ordering in the chain perfectly matches that during test generation. Therefore, LOS pattern generation should be done subsequent to scan stitching in conventional LOS. The only additional constraint imposed on scan stitching by the proposed partitioning scheme is that the interface registers of each region should be placed in consecutive positions on the scan chain and that they must be stitched in a bidirectional manner. Such a special stitching and the associated DfT support are required only for the interface registers in order to enable a proper rewind operation; minimization of the number of interface registers helps to minimize the area cost incurred. Finally, restoring the value of the rightmost bit of a group of interface registers subsequent to the launch operation necessitates an extra flip-flop, which holds the value of the rightmost interface bit upon launch; a subsequent rewind operation restores the value of the rightmost interface register from the value in this extra flip-flop.

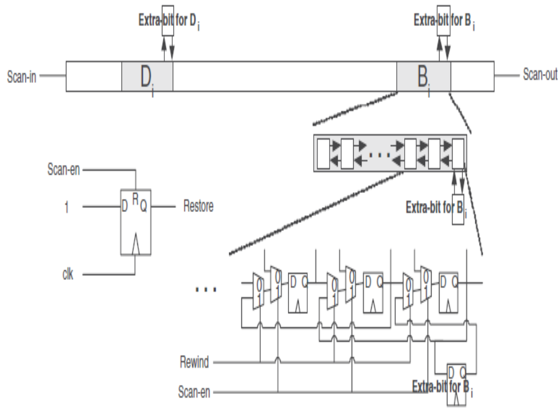


Figure 8: Block diagram for LOS

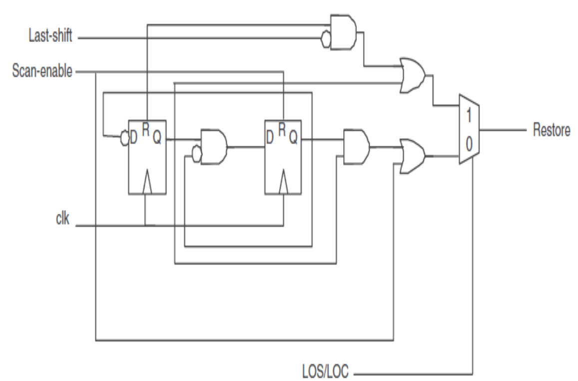


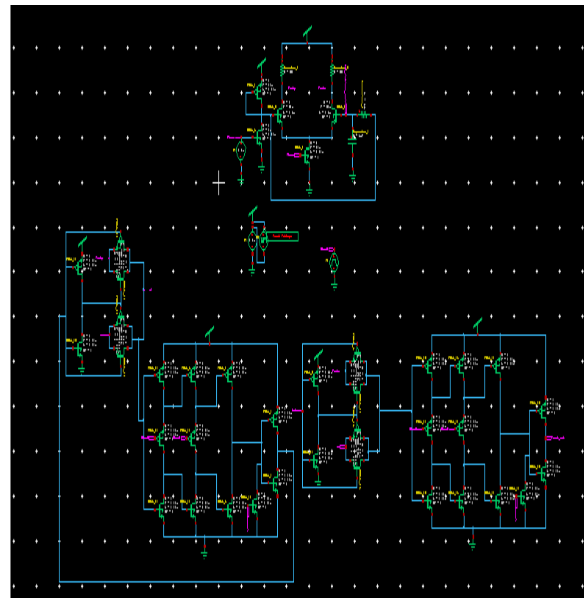
Figure 9: Architecture for Mixed tesing by LOC and LOS

C. Mixed testing

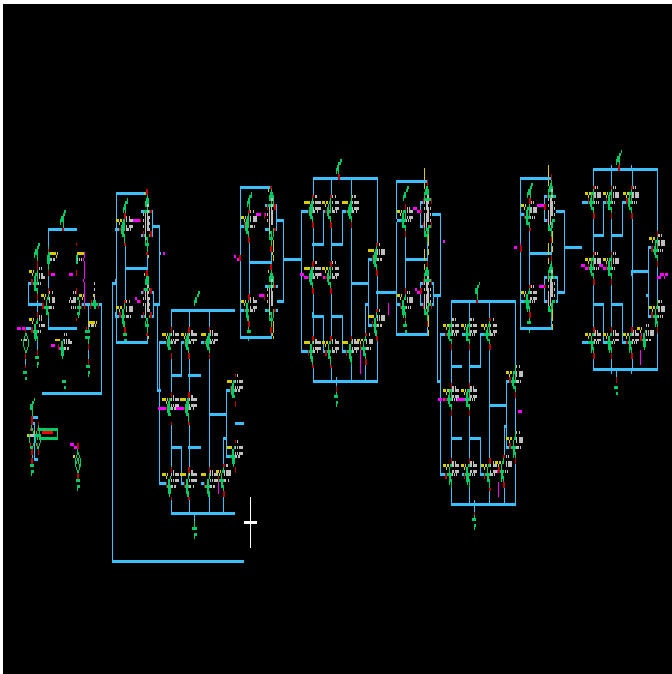
As the LOS and LOC testing may uniquely detect faults in a mutually exclusive manner, a mixed test with both LOS and LOC patterns typically yields a higher fault coverage level compared to either testing scheme applied alone. In this section, we outline the DfT support required to support lowpower mixed testing with both LOS and LOC patterns. While the bidirectional stitching of interface registers fails to enable the proposed low-power LOC testing, the shadow register support can be utilized to enable the proposed lowpower LOS testing; the shadow registers can replace the bidirectional stitching for the restoration of the load state in LOS testing. Therefore, to support both low-power LOS and LOC testing, the architecture in Fig. 3 can be utilized, but with a couple of changes; the shadow registers should be clocked only during the shift cycles, and a unified Restore signal should be generated to support both LOS and LOC operations. The simple circuitry that generates this unified Restore signal is provided in Fig. 5. The LOS/LOC signal, which denotes the type of test for the current pattern being applied and can be

V. RESULTS

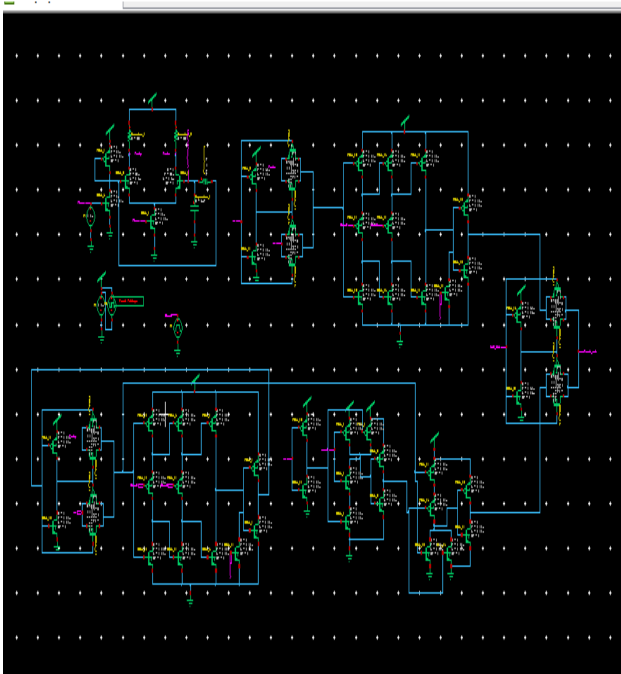
Architecture for LOC



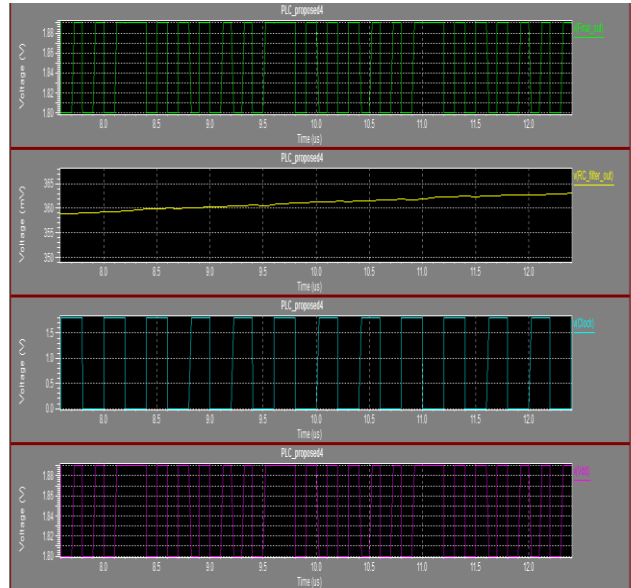
Architecture for LOS



Architecture: Mixed Testing



Mixing Testing Wave Forms



VI. CONCLUSION

A power efficient CMOS PLC receiver which can be incorporated in microprocessor like ICs to extract the test data signals from the power lines which are used for the low data rate communications such as scan design, system debugging, fault diagnosis etc. is designed and simulated in this work in CMOS 180 nm technology under the supply voltage of 1.8v. The proposed method paper Launch On Capture (LOC) And Launch On Shift (LOS) PLC system adopts a binary ASK modulation scheme, and the PLC receiver consists of three building blocks. The level shifter shifts the dc level of the data signal to a half of the supply voltage. The signal extractor, based on a differential amplifier, removes the dc voltage from the data signal with the aid of a low-pass filter, which mitigates supply voltage fluctuations and droops. The logic restorer, based on a differential Schmitt trigger, extracts logic values from the data signal while improving the noise immunity of the receiver. The PLC receiver was designed to demonstrate the feasibility of a robust receiver as a proof of concept and fabricated in CMOS 0.18-μm technology.

VII. REFERENCES

[1]. W. C. Chung and D. S. Ha, "A new approach for massive parallel scan design," in Proc. IEEE Int. Test Conf., Nov. 2005, pp. 1-10.

[2]. L. T. Wang, C. E. Stroud, and N. A. Touba, System-on-Chip Test Architectures: Nanometer Design for Testability. San Mateo, CA, USA: Morgan Kaufmann, 2010.

[3]. S. M. Saeed and O. Sinanoglu, "Design for testability support for launch and capture power reduction in launch-off-shift and launch-off-capture testing," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 22, no. 3, pp. 516-521, Mar. 2014.

[4]. J. Rajendran, O. Sinanoglu, and R. Karri, "Regaining trust in VLSI design: Design-for-trust techniques," Proc. IEEE, vol. 102, no. 8, pp. 1266-1282, Aug. 2014.

[5]. S.-J. Wang, Y.-S. Chen, and K. S.-M. Li, "Low-cost testing of TSVs in 3D stacks with pre-bond testable dies," in Proc. IEEE Int. Symp. VLSI Design, Autom., Test (VLSI-DAT), Apr. 2013, pp. 1-4.

[6]. H.-H. S. Lee and K. Chakrabarty, "Test challenges for 3D integrated circuits," IEEE Des. Test. Comput., vol. 26, no. 5, pp. 26-35, Sep./Oct. 2009.

[7]. M. Lee et al., "A novel DFT architecture for 3DIC test, diagnosis and repair," in Proc. Int. Symp. VLSI Design, Autom. Test (VLSI-DAT), Apr. 2014, pp. 1-4.

[8]. M. Richter and K. Chakrabarty, "Optimization of test pin-count, test scheduling, and test access for NoC-based multicore SoCs," IEEE Trans. Comput., vol. 63, no. 3, pp. 691-702, Mar. 2014.

[9]. T. Han, I. Choi, H. Oh, and S. Kang, "A scalable and parallel test access strategy for NoC-based multicore system," in Proc. IEEE 23rd Asian Test Symp. (ATS), Nov. 2014, pp. 81-86.

[10]. H. Kim, Y. Lee, and S. Kang, "A novel massively parallel testing method using multi-root for high reliability," IEEE Trans. Rel., vol. 64, no. 1, pp. 486-496, Mar. 2015.

[11]. Y. Fkih, P. Vivet, B. Rouzeyre, M.-L. Flottes, G. Di Natale, and J. Schloeffel, "2D to 3D test pattern retargeting using IEEE P1687 based 3D DFT architectures," in Proc. IEEE Comput. Soc. Annu. Symp. VLSI (ISVLSI), Jul. 2014, pp. 386-391.

[12]. Y. Fkih, P. Vivet, B. Rouzeyre, M.-L. Flottes, and G. Di Natale, "A JTAG based 3D DfT architecture using automatic die detection," in Proc. IEEE 9th Conf. Ph.D. Res. Microelectron. Electron. (PRIME), Jun. 2013, pp. 341-344.

[13]. A. Chandra, S. Chebiyam, and R. Kapur, "A case study on implementing compressed DFT architecture," in Proc. IEEE 23rd Asian Test Symp. (ATS), Nov. 2014, pp. 336-341.

[14]. E. Alpaslan, Y. Huang, X. Lin, W.-T. Cheng, and J. Dworak, "On reducing scan shift activity at RTL," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 29, no. 7, pp. 1110-1120, Jul. 2010.

[15]. S. Pei, H. Li, and X. Li, "Flip-flop selection for partial enhanced scan to reduce transition test data volume," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 12, pp. 2157-2169, Dec. 2012.

[16]. E. Alon, V. Stojanovi´c, and M. A. Horowitz, "Circuits and techniques for high-resolution measurement of on-chip power supply noise," IEEE J. Solid-State Circuits, vol. 40, no. 4, pp. 820-828, Apr. 2005.

[17]. N. H. Weste and D. M. Harris, CMOS VLSI Design: A Circuit and Systems Perspective, 4th ed. Reading, MA, USA: Addison-Wesley, 2011.

[18]. L.-C. Hsu and H.-M. Chen, "On optimizing scan testing power and routing cost in scan chain design," in Proc. Int. Symp. Quality Electron. Design, Mar. 2006, pp. 1-6.

[19]. X. Hu, "Analysis of microelectronic power distribution networks and exploration of 3D ICs," Ph.D. dissertation, Dept. Elect. Eng., Univ. California, San Diego, CA, USA, 2012.

[20]. J. Rius, "IR-drop in on-chip power distribution networks of ICs with nonuniform power consumption," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 21, no. 3, pp. 512-522, Mar. 2013.