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Anovel Approach to Solve Voltage Unbalance of the Dc Links In Multilevel H-Bridges Based Solid State Transformer Connected To Grid

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ABSTRACT

As the expansion of the dc distribution system and the augment of the penetration of distributed generations an intelligent transformer with the capability to actively supervise the power and allowing for the easy connection of the distribution resources is becoming essential. The cascaded H-bridge multilevel inverter (CHMI)-based solid state transformer (SST) has the features of immediate voltage regulation, voltage sag compensation, fault isolation, power factor correction, harmonic isolation and dc output. Acting very much like an energy router, each SST has bidirectional energy flow control potential allowing it to control active and reactive power flow and to handle the fault currents on both low- and high-voltage sides. Its large control bandwidth offers the plug-and-play feature for distributed resources to speedily recognize and respond to changes in the system. This paper proposes a 20-kVA cascaded H-Bridge multilevel converter-based SST to directly interface with 7.2-kV single-phase distribution voltage level. The SST consists of a cascaded multilevel ac/dc rectifier, dual active bridge (DAB) converters with high-frequency transformers. The DAB converter regulates the 400-V-low-voltage dc bus and added dc/ac inverters can be added to present a 60 Hz 120/240-V ac residential voltage.

Keywords: Cascaded H-Bridge converter,*dq*vector control, solid-state transformer (SST), voltage and power balance.

I. INTRODUCTION

Permanent mThe proliferation of distributed generation and renewable energy resources has motivated the researchers to investigate the feasibility of a new microgrid operation mode future renewable electric energy delivery and management (FREEDM) system. The FREEDM system is a new medium-voltage microgrid composed of several solid-state transformers (SST), high bandwidth digital communication, and distributed control. As the fundamental component of innovative smart microgrid system, SST is intended to replace the conventional line-frequency transformers and performs the power flow control. Conventional transformers possess many undesirable properties including bulky and power quality susceptibility. In contrast, the SST is an intelligent power electronics system with capabilities such as managing power flow, providing power quality improvement, and allowing easy connection of the distribution resources [1]–[5].

Figure 1 shows a typical FREEDM system which consists of three parts. The first part is the user-level interface that includes both a 400-V dc distribution bus and low-voltage 220-V ac bus. The second part is an intelligent energy management (IEM) device, which is connected to 10-kV ac distribution bus and supports the regulated buses. The IEM is actually formed by the SST that manages bidirectional power

flow control to all devices connected to the low-voltage (400 and 220 V ac) buses and loads. It also has many additional functions such as voltage regulation, voltage sag compensation, fault isolation, and harmonic isolation. The third part is called the distributed grid intelligence operating system, which is embedded into the IEM device and utilizes the communication network to coordinate the system power management with other energy routers. Furthermore, an intelligent fault management device is used to prevent potential faults in the 10-kV ac circuit and reconfiguration capability and uninterrupted power quality to the user [6]–[8].

An important objective of using the SST in the FREEDM system is to achieve compatibility and flexibility. It can regulate the low-voltage buses and provide active and reactive power control or power/frequency control for the grid-side port. Figure2 shows the proposed 20-kV·A SST based on the cascaded H bridge multilevel inverter (CHMI). The SST consists of a dual active bridge (DAB) dc/dc stage to step up the 400-V dc input to the high-voltage dc link, a cascade H-Bridge multilevel dc/ac inverter stage to provide active power and reactive power for the 10-kV ac grid, and a dc/ac stage to produce a 220-V ac residential voltage for loads. In China, the utility systems and residential voltage are 10 kV and 220 V, respectively.

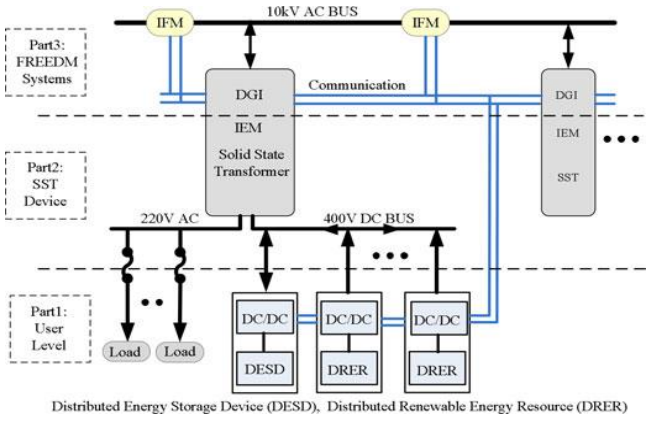


Figure 1. Microgrid interface of the FREEDM system

Despite cascaded H-bridge topology has been widely used in the SST device because of its modularity to achieve medium voltage output and good power quality, it also has several drawbacks [9]–[15]. One of the main drawbacks is the power unbalance at different phases and the dc voltage unbalance at different modules. Various configurations for cascaded H-bridge multilevel converter have been reported in [16]–[22], most of previous research mainly focuses on applications in static synchronous compensator, EV traction drive, and medium-voltage industrial drives for improving power quality and reliability of a power distribution system. In [20] and [21], the proposed system is implemented based on independent PV solar sources with independent MPPT control algorithm for each PV string. The PV input is connected directly to the cascaded H-bridge dc/ac module and the dc–dc DAB stage has been eliminated to reduce the size of the converter. However, it requires three individual PI controllers for each PV cell to balance the inverter output and there is no isolation between the low- and high-voltage sides due to the elimination of the DAB stage and its high-frequency transformer. A single-phase SST to interface with the 7.2-kV distribution system has been reported in [22]. It consists of a cascaded H-bridge ac–dc rectifier, a dc–dc converter (DAB), and an ac–dc inverter stages. Through the interaction of the DAB controller with the rectifier controller, the rectifier dc-link voltages and DAB stage powers can be balanced by selecting the voltage feed-forward and feedback coefficients in DAB modules.

Nevertheless, the optimal selection of these coefficients is not given and it requires three-individual controllers for each DAB module. Furthermore, the power flow from distributed renewable energy source to utility for three-phase system is not discussed. Different topologies other than DAB dc–dc converter to boost the PV source voltage are also proposed for SST in [23] and [24] but the concept is based on transformerless SST where there is no isolation transformer between input and output.

This project extends some of the control methods developed previously [20]–[22] for different applications and validates the concept by means of numerical simulations, validation carried out on a 10-kV·A laboratory prototype. The project investigates the application of the three-phase SST and its controller with the energy flow from the distributed renewable energy resources to the grid under unbalanced conditions. The control scheme resolve the power and voltage unbalanced problems of three-phase SST including the unbalanced of different modules (DAB+CHMI) in each phase and finally inject a purely sinusoidal balanced three-phase current into the ac grid. The controller employs the moving floating neutral point control algorithm to balance the power at the three phase ac side and the dynamic reference voltage method (feed-forward compensation) to balance the dc-link voltage of different modules in each phase. A master–slave control (MSC) is used to control the output of the DAB stage. Compared with the previous methods [20]–[22], the proposed technique have the following features: 1) This project investigates the application of the SST converter in FREEDM system and its control with power flowing from the distributed renewable energy resources to the grid under unbalanced conditions. 2) The DAB stage is used to boost the low input voltage of renewable energy sources to medium voltage level of the ac grid distribution. Therefore, multiple renewable energy sources can be used in parallel to increase the power rating of the system. 3) The dc-link voltage drift is controlled by two independent controllers. The DAB master–slave and the additional feedforward voltage balance mechanism embedded in the CHMI modulation stage. 4) It simplifies the controller of the DAB stages using the master–slave method and provides high-frequency galvanic isolation between the input and output.

II. THREE-PHASE SST MODELING AND CONTROL

The topology and control strategy of a three-phase SST (see Figure 2) are developed in this section. The prototype of the SST is rated as input dc-link voltage of 400 V, output ac-voltage of 10 kV, and output power of 20 kVA. The first stage of SST is high-frequency DAB converter which boosts low-voltage dc input to high-voltage dc link. The second stage is CHMI, which converts the dc-link voltage to medium voltage ac grid, and controls active and reactive power delivered to grid.

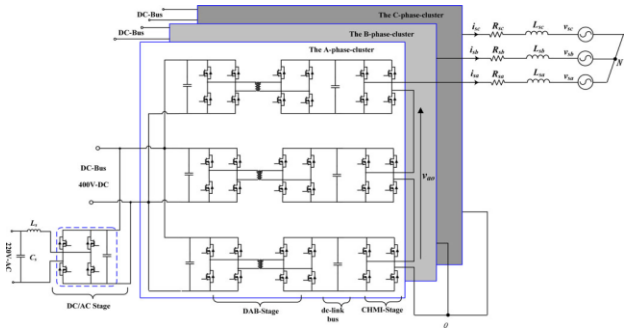


Figure 2. Topology of the proposed 20-kVA three-phase SST

Figure 3 shows architecture of the DAB stages and their control circuit. The DAB stage steps up the 400-V dc input to 4-kV dc output which is fed to CHMI stage. In the proposed control circuit, only one DAB converter is utilized as the master proportional-integral (PI) voltage controller, which executes all control and modulation calculations and sends the resultant converter driving command signals to other DAB slave controllers via high-speed fiber optic. Typically, DAB slave controllers only manage devices switching and protection. Also, to calculate the power transferred by each module and implement the protection of overvoltage and over current, the voltage and current of input side and output side are all sensed. Since circuit structure is completely identical, the output voltage amplitude of each DAB converter should be equal to the reference voltage with the same driving signals assuming that the

components (switches and transformers) of each DAB stage are ideal.

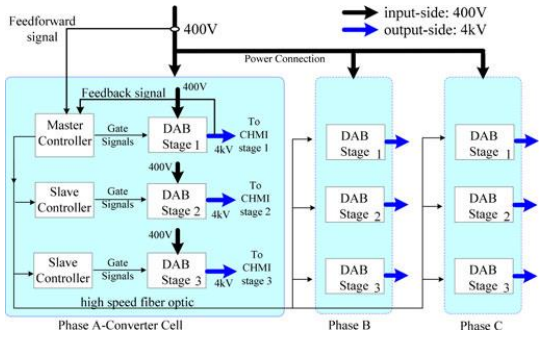


Figure 3. MSC diagram of the DAB converter stages

However, it is unlikely to have 100% identical switching devices and transformer parameters for each DAB, resulting in slightly unbalanced of power transferred by DAB modules. Nevertheless, this unbalanced can be also compensated by the CHMI controller stage, which will be discussed in Section III. Therefore, the proposed master–slave controller in the DAB stage not only provides the high-frequency galvanic isolation, but also simplifies the complex algorithm and improves the dynamic performance. The function of CHMI stage is to produce sinusoidal three phase output voltage/current and control the active/reactive power injected into the grid. Figure4 shows the block diagram of a three-phase decoupled current controller developed for the CHMI stage.

The average of all the dc-link voltages is used to determine command of the total real power references $P*$needed to control the output of the three-phase system. The controller of CHMI stage in Figure4 contains two loops 1) outer voltage loop and 2) inner current loop. The outer voltage loop regulates the average dc-link voltages in order to determine the overall active power P needed to control the system. Therefore, the dc-link voltage drift is indirectly dealt with by modulating the voltage reference amplitude of each phase according to the respective imbalance proportion which causes unbalanced power drawn by each module until the balance is achieved. In addition, the reactive power reference can be controlled at different values depending on the system requirements. According to the three-phase dq transformation, the ac-voltage commands ($v*d$ and $v*q$) in the d-axis and q-axis is expressed by

$$\begin{bmatrix} v_d^* \\ v_q^* \end{bmatrix} = \frac{1}{N}\left(\begin{bmatrix} v_{Sd} \\ 0 \end{bmatrix} - \begin{bmatrix} 0 & -\omega L_{\mathrm{AC}} \\ \omega L_{\mathrm{AC}} & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} - K_P \begin{bmatrix} i_d^* - i_d \\ i_q^* - i_q \end{bmatrix} - K_I \int \begin{bmatrix} i_d^* - i_d \\ i_q^* - i_q \end{bmatrix} dt \right) \quad (1)$$

where id is the d-axis current, iq is the q-axis current, $i*d$ is the d-axis current reference, $i*q$ is the q-axis current reference, ω is the frequency of rotation of the reference frame in rad/sec, vSd is the d-axis component corresponding to the three-phase grid voltage, and LAC is the ac line inductor. Note that the coefficient $1/N$ in Figure 4 represents the number of cascaded converters, which is N = 3in this case. The command voltages are transformed back to the three-phase reference signals $v*ao$, $v*bo$, and $v*co$ by applying the inverse dq transformation, where they will be used as the phase-shifted pulse width modulation (PS-PWM) modulator signals in CHMI stage. Then, (1) can be rearranged as

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{1}{L_{\mathrm{AC}}}\begin{bmatrix} K_P(i_d^* - i_d) + K_I \int (i_d^* - i_d)dt \\ K_P(i_q^* - i_q) + K_I \int (i_q^* - i_q)dt \end{bmatrix}. \quad (2)$$

Equation (2) signifies that id and iq can be controlled independently from each other, which means that the SST can provide active and reactive power control for the 10-kV ac grid independently. Meanwhile, in order to properly address the inherent power and voltage unbalance issues due to the difference of module parameters, an additional control strategy is added into the modulation stage, which is the second focus of this research.

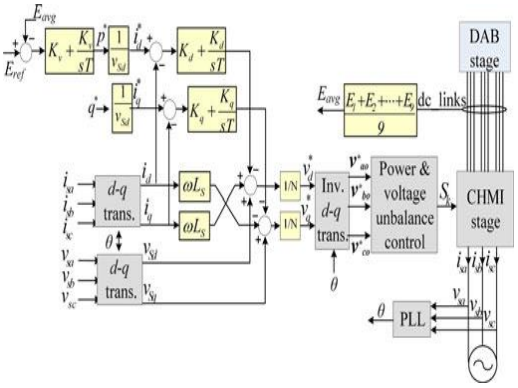


Figure 4. Control scheme of the three-phase grid currents

Due to the modularity of topology, PS-PWM is the optimum modulation method for CHMI stage. The switching state of one H-bridge-module *Sk* is determined by the logical value of two signals (*Sk*1, *Sk*2), which can be "1" and "0" representing the "ON" and "OFF" state of each switch, respectively. This leads to four different binary combinations that generate three different output voltage + *V*dc, 0, and − *V*dc. Since these H bridge- modules are connected in series, the total output voltage of one phase *m* (*m* = *a, b, c*) is given by

$$v_{mN} = \sum_{y=1}^{k} v_{my} = \sum_{y=1}^{k} V_{\mathrm{dc}}\left(S_{y1} - S_{y2}\right) \qquad (3)$$

where *k* is the number of power modules per phase and *V*dc is the dc-link voltage of each module. The series connection of *k* modules will produce 2*k* + 1voltage levels in the total converter output voltage. The PS-PWM modulation principle with three modules per phase is shown in Figure5. Due to the modularity of the topology, each module can be modulated independently using unipolar PWM with the same reference signal [25]. In this project, three modules carrier signals are controlled at the same frequency 1 kHz and shifted by2π/3 rad from each other. Since the phase shift introduces a multiplicative effect, the CMHI line-to-neutral voltage has a switching pattern with three times the frequency the switching devices of each module. Hence, this converter can easily reach medium voltage without the low-frequency transformer and the total harmonic distortion is lower.

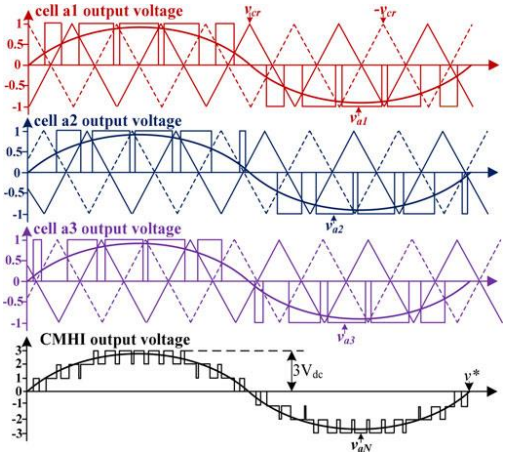


Figure 5. Phase-shifted PWM waveforms for a three-module CHMI

Figure 6 shows the digital control architecture of the CHMI based on DSP and FPGA. The sampled data consists of dc-high side voltage/current and three-phase grid voltage/current. The synchronization of the *dq* transformation is performed through a phase-locked loop to regulate the active and reactive power in the DSP controller. Meanwhile, the power and voltage unbalance compensation calculation have also been added into the controller. Since the frequency of the switching devices of each module is 1 kHz, the sampling frequency is 6 kHz and the reference update period is 1 ms. Therefore, the digital control system has to execute a sequence of voltage/current signal acquisition and voltage reference computation within the sampling period of 167 μs(1 s/6*k*). The DSP sends voltage references every 167 μs to FPGA, which plays an essential role in using phase shifted clock to generate 36 corresponding PWM signals. The problem description and solution of the inherent unbalance among three phases and different modules of one phase are discussed in the next section.

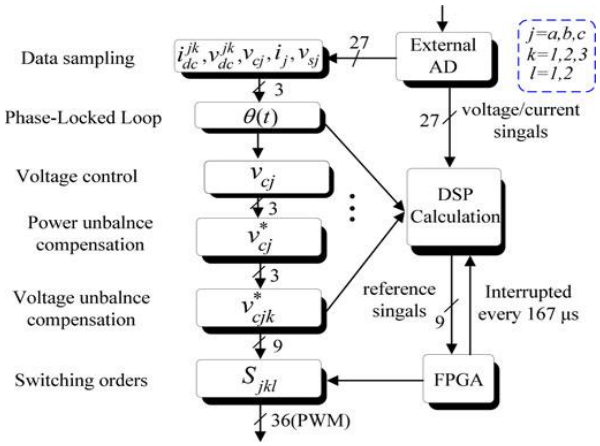


Figure 6. Software block diagram for the CHMI stage

III. MATLAB/ SIMULATION RESULTS

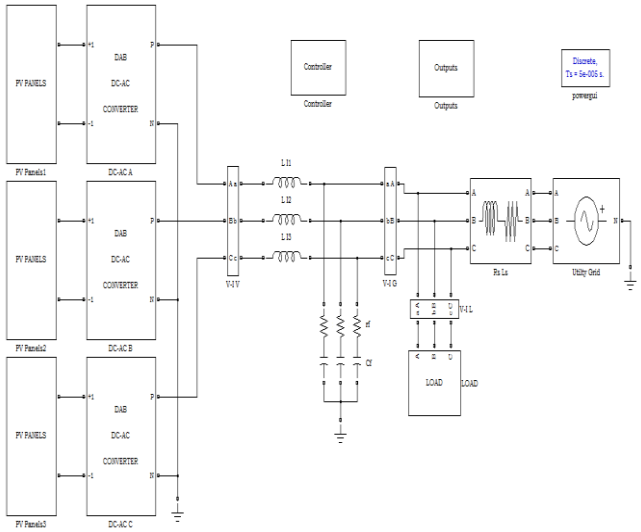


Figure 7. Simulation diagram of proposed system

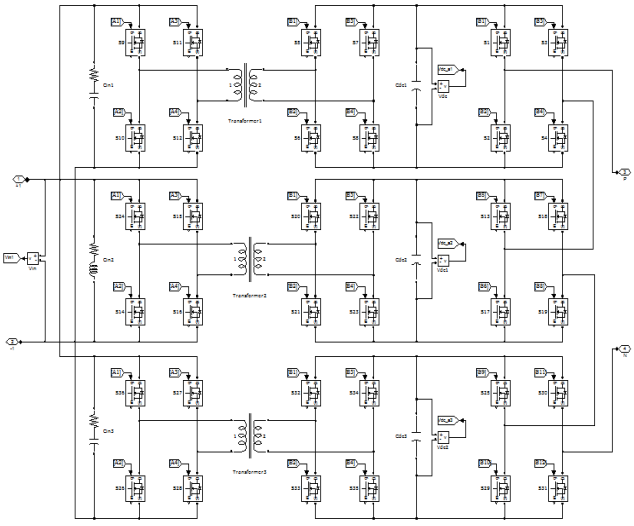


Figure 8. Simulation block diagram ofEMF signals to Pulse signals

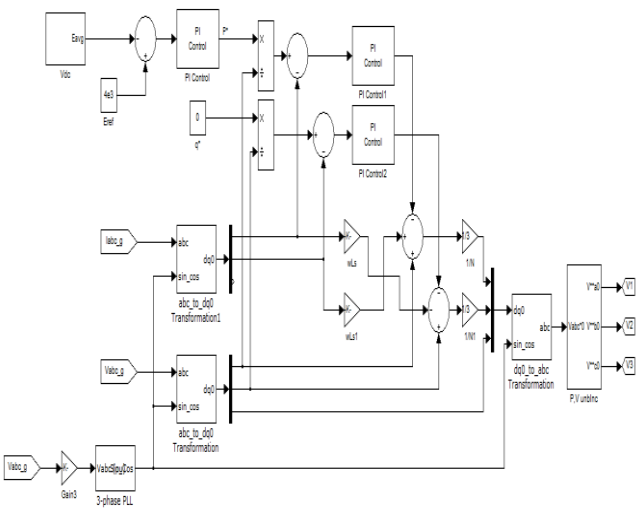


Figure 9. control scheme of grid currentSimulation block

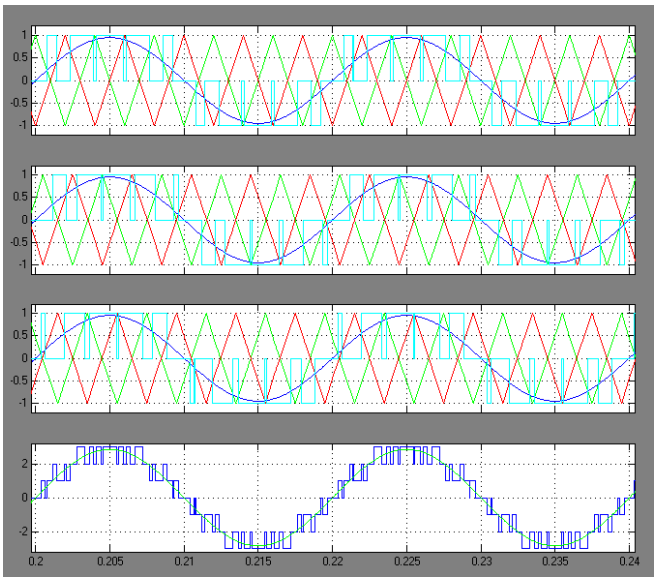


Figure 10. Simulation Phase-shifted PWM waveforms implementation

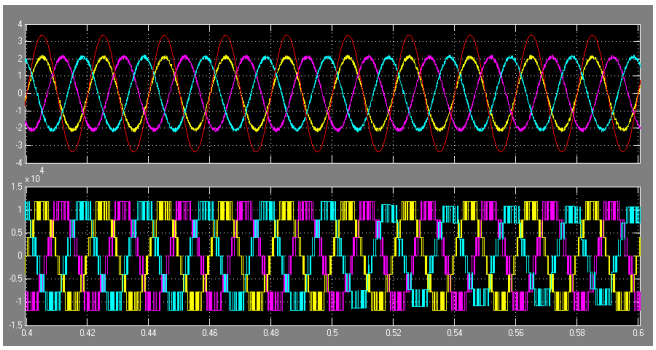
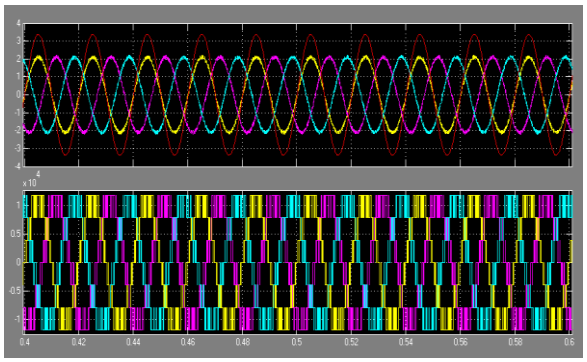


Figure 11. Dynamic performance without power balance controlresults

The three-phase delivered currents to the grid are unbalanced and the line-to-neutral voltage in phase A also becomes distorted. Meanwhile, the unbalanced condition also results in a pulsating power at the gird

side because the active power and reactive power are respectively proportional to the dq synchronous frame components of the grid current isd and isq . Figure 12 shows three-phase output currents with the power balance control. With the power balance control, three-phase grid currents are completely balanced despite the modules are operating at different power levels. This is because the injection of zero-sequence voltage does not affect the line-to-line voltage. To validate the voltage balance control, the dc-link voltages of three modules of phase B are given in Figure15. Figure15(a) shows that the three dc-link voltages cannot maintain at the reference value without voltage unbalance control. The reason is that the CHMI modulation stage imposes the same voltage reference foreach module, while their voltages drift when power transferred are different by DAB modules. The module that delivers more power has higher dc-link voltage. Figure 15(b) shows the three dc-link voltages of phase B with the proposed voltage balance control. The output voltage values of the three modules are equal based on the voltage balance control. The controller modifies the amplitude of each module voltage reference according to their respective unbalance deviation to redistribute the switchingdevices ON/OFF times. This reduction on the voltage reference causes a reduction on the ON time of the module for making a rise on the corresponding dc-link voltage.



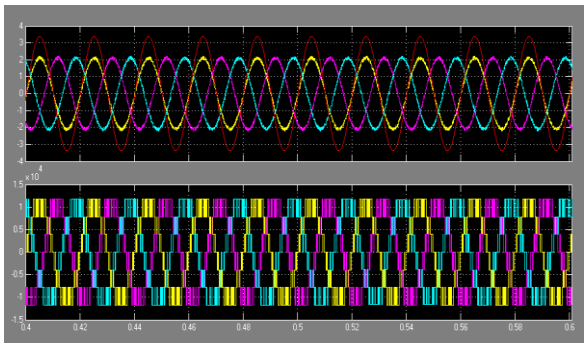


Figure 12. Dynamic performance with power balance controlresults (a)with control 1 (b) With control 2

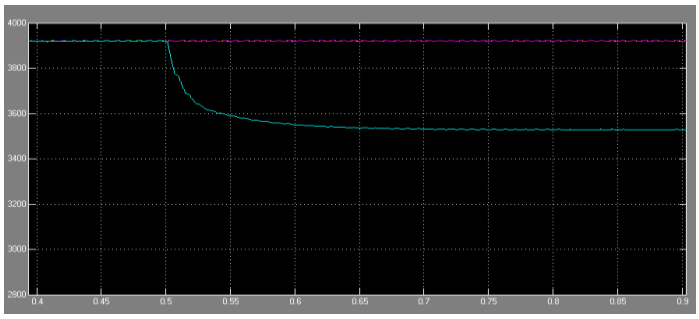


Figure 13. Dynamic performance of three dc-link voltages of phase B. (a)without voltage balance control.

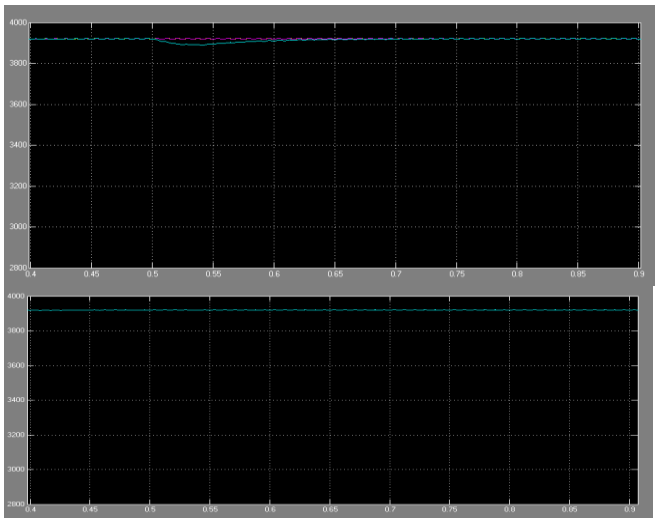


Figure 14. Dynamic performance of three dc-link voltages of phase -C output with voltage balance control.

IV. CONCLUSIONS

In this project, a cascaded H-Bridge converter-based SST is schemed to interconnection between 7.2-kV ac grid and a 400-V dc distribution in smart grid systems. The single-phase dq vector designing and restrain of the SST, including ac/dc rectifier, DAB converter is

developed. A new voltage balance restrain procedure is schemed to resolve the voltage unbalance of the dc links in different H-bridges. The power intrinsic unbalance constraints of the voltage balance restrain for the cascaded H-Bridge rectifier is derived and verified by simulations. Mean-while, a power balance restrain procedure is schemed to regulate the real power transferring through the parallel modules. Finally, the switching model simulation and SST scale-down prototype are instigated with the schemed controller. The results confirm the performance of the SST, including power factor correction, real and reactive power restrain, voltage sag compensation, and the schemed voltage balance restrain.

V. REFERENCES

[1]. J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverter: A survey of topologies, controls, and application," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724 –738, Aug. 2002.

[2]. J. S. Lai, A. Maitra, A. Mansoor, and F. Goodman, "Multilevel intelligent universal transformer for medium voltage applications," in Proc. Conf. Rec. 40th Annu. Meet. Ind. Appl. Soc., Oct. 2005, vol. 3, pp. 1893–1899.

[3]. J. Carrasco, L. Franquelo, J. Bialasiewicz, E. Galvan, R. Guisado, M. Prats, J. Leon, and N. Moreno-Alfonso, "Power-electronic systems for the grid integration of renewable energy sources: A survey," IEEETrans. Ind. Electron., vol. 53, no. 4, pp. 1002–1016, Jun. 2006.

[4]. S. Bhattacharya, T. Zhao, G.Wang, S. Dutta, S. Baek,D.Yu, B. Parkhideh, X. Zhou, and A. Q. Huang, "Design and development of generation-I silicon based solid state transformer," in Proc. IEEE Appl. Power Electron.Conf., Feb. 2010, pp. 1666–1673.

[5]. S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B.Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[6]. T. Zhao, "Design and control of a cascaded H-bridge converter based solid state transformer (SST)," Ph.D. dissertation, Dept. Electr. Eng., North Carolina State Univ., Raleigh, NC, USA, 2010.

[7]. H. Fan and H. Li, "High-frequency transformer isolated bidirectional DC–DC converter modules with high efficiency over wide load range for20 kVA solid-state transformer," IEEE Trans. Power Electron., vol. 26, no. 12, pp. 3599–3608, Dec. 2011.

[8]. H. Zhu and D. Zhang, "Influence ofmulti-junction Ga/As solar array parasitic capacitance in S3R and solvingmethods for high power applications," IEEE Trans. Power Electron., vol. 29, no. 1, pp. 179–190, Jan. 2014.

[9]. G. S. Perantzakis, F. H. Xepapas, and S. N. Manias, "A novel fourlevel voltage source inverter: Influence of switching strategies on the distribution of power losses," IEEE Trans. Power Electron., vol. 22, no. 1, pp. 149–159, Jan. 2007.

[10]. S. Lu and K. A. Corzine, "Advanced control and analysis of cascaded multilevel converters based on P-Q compensation," IEEE Trans. PowerElectron., vol. 22, no. 4, pp. 1242–1252, Jul. 2007.

[11]. L. Maharjan, S. Inoue, and H. Akagi, "A transformerless energy storage system based on a cascade multilevel PWM converter with star configuration," IEEE Trans. Ind. Appl., vol. 44, no. 5, pp. 1621–1630, Sep. 2008.

[12]. C. Govindaraju and K. Baskaran, "Efficient sequential switching hybrid modulation techniques for cascaded multilevel inverters," IEEE Trans.Power Electron., vol. 26, no. 6, pp. 1639–1648, Jun. 2011.

[13]. L. Maharjan, T. Yamagishi, and H. Akagi, "Active-power control of individual converter modules for a battery energy storage system based on a multilevel cascade PWM converter," IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1099–1107, Mar. 2012.