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Closed loop Control of Hybrid Boosting Converter for Renewable Energy Applications

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ABSTRACT

This paper presents a new hybrid boosting converter is used to increase the input dc voltage. In Existing method hybrid boosting converter used with one switch in the converter and produce pulses for that switch in open loop. By using the open loop method, we get only output as produced amount of input which is given. Moreover, we propose a closed loop method for HBC in this project. By using this closed loop control technique, we achieve required output voltage.

Keywords : Hybrid Boosting Converter, Renewable Energy, MVDC

I. INTRODUCTION

IN recent years, the quick improvement of renewable energy system calls for new generation of high gain dc/dc converters with high efficiency and low cost. The front end of "plug and Play" PV system ordinarily requests venture up converter which is fit for boosting the voltage from 35 to 380Vwith control ability due to the low terminal voltage and the prerequisite of MPPT tracking capacity for single PV panel. Considering a wind cultivate with inner medium-voltage dc (MVDC)- system, a MVDC converter ready to help the voltage from 1–6 to 15–60 kV is required to connect the output of generator-confronting rectifier to the MVDC line. Some other energy storage systems, for example, fuel cell fueled system likewise require high-gain dc/dc converter due to their low voltage level at capacity side. Keeping in mind the end goal to accomplish high voltage transformation proportion with high proficiency, numerous high gain upgrade procedures were researched in the past distributions. Among them, switched capacitor structure, tapped/coupled inductor-based method, transformer-based procedure voltage multiplier structure or mixes of them attracted significant attentions. Each technology has its unique advantages and limitations. The switched capacitor dc–dc converter can achieve high effectiveness however has throbbing present and poor control capacity. Presentation of thunderous switched capacitor converter can mitigate the throbbing current however does not understand the control issue.

The tapped-inductor and transformer facilitates gain boosting function but requires snubber circuit to handle leakage problem. The blend of above advancements often outputs promising circuit includes however with intemperate number of parts. In this paper, gain improvement innovation considering adjustment of customary help converter while keeping up single inductor and single switch is

examined, focusing at improving the circuit configuration, diminishing the cost, fulfilling the requests of ordinary high gain applications, what's more, encouraging large scale manufacturing. Gain upgrade from a help converter began from quadratic support. It accomplished higher voltage gain with a solitary switch yet presented high segment voltage stretch. In any case, this converter persuaded high gain converter advancement take after on.

Many gain expansion strategies for help converter by including just diodes and capacitors were examined previously. The strategy for consolidating support converter with customary Dickson multiplier what's more, Cockcroft–Walton multiplier to create new topologies were proposed, for example, topologies in Figure 1(a) what's more, (b). Air core inductor or stray inductor was utilized inside voltage multiplier unit to decrease current throb. A basic circuit utilizing the super lift strategy was proposed and stretched out to higher gain applications such as Figure 1(c). Its partner of negative output topology and twofold outputs topology were proposed and examined furthermore. The idea of multilevel help converters was researched in and the topology of Figure 1(d) was given as focal source association converter. Also, two switched capacitor cells were proposed, and various topologies were determined by applying them to the essential PWM dc–dc converters. Ordinary topologies are appeared as Figure 1(e) and (f). An altered voltage-lift cell was proposed, and the topology of Figure 1(g) was created. Motivated by the above topologies, another mixture boosting converter (HBC) with single switch and single inductor is proposed by utilizing bipolar voltage multiplier (BVM) in this paper.

The second-series HBC is appeared as Figure 1(h). Looked at with other recorded topologies in Figure 1, the proposed converter diminishes the voltage rating of output channel capacitor and displays the nature interleaving operation attributes. Contrasted and the converter in Figure 1(d), the proposed converter has littler

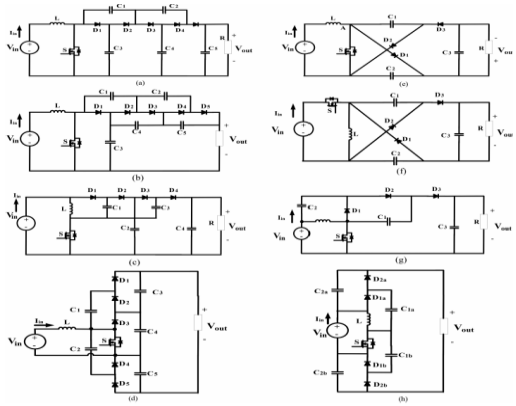

Figure 1. Previous high-gain dc–dc converters with single-switch single-inductor and proposed topology. (a) Boost + Dickson multiplier , (b) Boost + Cockcroft–Walton multiplier , (c) super lift with elementary circuit , (d) central source multilevel boost converter, (e) Cuk derived, (f) Zeta derived , (g) modified voltage lifter, and (h) proposed second-order HBC.

Output ripple and higher parts usage rate with respect to change ratio. Some interleaving advances for swell decrease and power development were accounted for in the writing; however, these strategies are typically in view of circuit branch development which requires more parts. The proposed topology has accomplished littler swell with single switch what's more, single inductor while keeping up high voltage gain.

As of late, numerous more structures accomplishing higher gain were additionally reported, yet they embraced no less than two inductors on the other hand switches, or some depend on tapped inductor/transformer, which may confound the circuit design and increment cost.

II. PROPOSED GENERAL HBC TOPOLOGY AND ITS OPERATIONAL PRINCIPAL

The proposed HBC is appeared in Figure 2. There are two renditions of HBC, odd-series HBC and even-series HBC as appeared in Figure 2(a) and (b). The even-series topology incorporates the info source as a major aspect of the output voltage, prompting to a higher parts usage rate as for a similar voltage gain. Be that as it may, they have comparable different qualities and circuit investigation strategy.

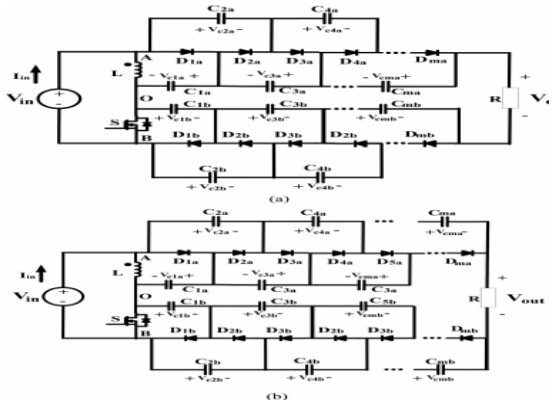

Figure 2. Proposed general HBC topology. (a) Odd-order HBC. (b) Even-order HBC.

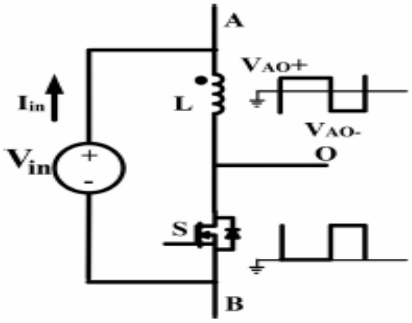

Figure 3. Inductive three-terminal switching core.

A. Inductive Switching Core

In a HBC topology, the inductor, switch and information source serve as an "inductive switching center," appeared as Figure 3.

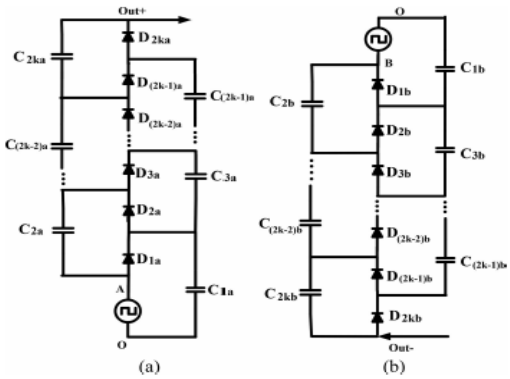

Figure 4. Bipolar voltage multiplier. (a) Positive multiplier. (b) Negative multiplier.

It can create two "complimentary" PWM voltage waveforms at port AO and port OB. Although the two voltage waveforms have their person high voltage level and low voltage level, the hole between two levels is indistinguishable, which is a critical normal for inductive switching center for interleaving operation.

B. BVM

A BVM is made from a positive multiplier branch and a negative multiplier branch, appeared in Figure 4(a) and (b). Positive multiplier is the same as customary voltage multiplier while the negative multiplier has the contribution at the cathode terminal of fell diodes, which can create negative voltage at anode terminal, appeared in Figure 4(b). By characterizing the high voltage level at information AO as VOA+, the low voltage level as VOA–, and the obligation cycle of high voltage level as D, the operational conditions of the even-series positive multiplier is inferred as Figure 5 and showed as taking after:

1) State 1 [0, DTs]: When the voltage at port AO is at abnormal state, diodes $D_{ía}$ (i = 2k – 1, 2k – 3 . . . 3, 1) will be directed sequentially. Every diode turns out to be contrarily one-sided some time recently the following diode completely leads. There are Substrates came about as appeared in Figure 5(a). Capacitor C_{ia} (i = 2, 4 . . . 2k) are released during this time interim. Accepting the flying capacitors get completely charged at unfaltering state and diodes voltage drop are disregarded, the accompanying relationship can be inferred:

$$V_{c1a} = V_{Ao+} \dots\dots (1)$$

$$V_{cia} = V_{c(i+1)a} (i = 2,4,6, \dots, 2k-2) \dots\dots (2)$$

2) State 2[dTs, Ts]: When the voltage at port AO ventures to low level, diode D2k an is led to begin with, appeared as Figure 5(b)- (1). At that point the diodes $D_{ía}$ (i = 2, 4, . . . 2k – 2) will be turned on in a steady progression from high number to low. Every diode will be turned on when the past one gets to be blocked. Just diode D2ka is led for the entire time interim of [0, dTs], since capacitor $C_{(2k-1)a}$ need to somewhat give the heap current during the entire time interim.

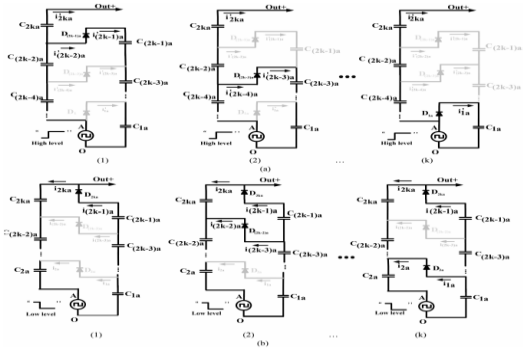

Figure 5. Operation modes of even-order BVM positive branch. (a) State 1[0, DTs]. (b) State 2[DTs,Ts].Despite the fact that not every one of the diodes are directed and obstructed in the meantime, the flying capacitors still have the accompanying relationship by the end of this time interim:

$$V_{c2a} = V_{c1a} - V_{A0-} \dots\dots (3)$$
$$V_{cia} = V_{c(i+1)a} (i = 3,5,7, \dots, 2k-1) \dots\dots (4)$$

As indicated by charge adjust main, the aggregate sum of electrical charge streaming into capacitors C_{ia} (i = 2, 4, . . . 2k) ought to equivalent to that turning out from them in a switching period at consistent state,

$$\sum_{i=1}^{k} \int_{0}^{DT_s} i'_{2ia} dt = \sum_{i=1}^{k} \int_{DT_s}^{T_s} i_{2ia} dt \dots\dots (5)$$

hence in this way, the capacitor assembles C_{ia} (i = 2, 4 . . . 2k) can be supplanted by a comparable capacitor C2a(eq).The diode assemble Día (i = 2, 4 . . . 2k) which gives the charging way to C2a(eq) is comparable to a solitary diode C2a(eq). Additionally, the capacitor amass C_{ia} (i = 1, 3, . . . 2k – 1) can be supplanted by an equal capacitor $C_{1a(eq)}$ and diode gather D_{ia} (i = 1, 3, . . . 2k – 1) by D1a(eq). The last equal even-series positive multiplier branch is given as Figure 6(a). A comparable examination outputs the proportionate negative multiplier branch as appeared in Figure 6(b). As indicated by (1)–(4), the voltage of identical capacitors $C_{1a(eq)}$,$C_{2a(eq)}$ can be communicated as taking after:

$$V_{c2a(eq)} = K(V_{A0+} - V_{A0-}) \dots\dots (6)$$
$$V_{c1a(eq)} = (k-1)(V_{A0+} - V_{A0-}) + V_{A0+} \dots (7)$$

For the negative branch shown in Figure 6(b), the following results can be obtained based on similar analysis:

$$V_{c2b(eq)} = K(V_{0B+} - V_{0B-}) \dots\dots (8)$$
$$V_{c1b(eq)} = (k-1)(V_{0B+} - V_{0B-}) + V_{0B+} \dots (9)$$

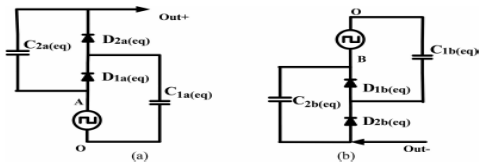

Figure 6. Equivalent circuit. (a) Even-order positive multiplier. (b) Even-order negative multiplier.

Where V_{OB+} is the high voltage level of input port OB and VOB– is the low voltage level.

3) **Equivalent Capacitance Derivation**: Assuming capacitors C_{ia} (i = 1, 2, 3, 2k) have the same capacitance C, to derive the equivalent capacitance of $C_{2a\ (eq)}$ and $C_{1a\ (eq)}$ in expression of C, a voltage ripple-based calculation method is proposed in this section. Assuming the peak to peak voltage ripple of the flying capacitors can be expressed as ΔV_{cia} (i= 1, 2, 3 . . . 2k), the ripple of equivalent capacitor $C_{2a\ (eq)}$ Is ΔV, the following relationship can be approximated:

$$\Delta V = \Delta V_{c2a} + \Delta V_{c4a} + \cdots \Delta V_{c2ka.} \dots (10)$$

In Figure 5, assuming the average current of $i_{\_ia}$ (i = 1, 2, 3 . . . 2k) during [0, dTs] is (i= 1, 2, 3 . . . 2k) $i_{\_2ia(on)}$ and the average current of i_{ia} (i= 1, 2, 3 . . . 2k) during [dTs, Ts] is $i_{ia\ (off)}$ (i = 1, 2, 3 . . . 2k), according to charge balance of capacitors Cia (i = 2, 4 . . . 2k), it can be derived that

$$\overline{i'_{ia(on)}} DT_s = \overline{i_{ia(off)}} D'T_s (i = 2,4, \dots 2k) \dots (11)$$

At the same time, state 1 gives

$$\overline{i'_{ia(on)}} = \overline{i'_{(i+1)a(on)}} (i = 2,4, \dots 2k-2) \dots (12)$$

State 2 gives

$$\overline{i_{ia(off)}} = \overline{i_{(i+1)a(off)}} (i = 1,3, \dots 2k-3) \dots (13)$$

Based on the (11)–(13), the following relationship can be obtained:

$$\overline{i_{2a(off)}} = \overline{i_{4a(off)}} = \cdots \overline{i_{(2k-4)a(off)}} = \overline{i_{(2k-2)a(off)}} = \overline{i_{(2k-1)a(off)}} \dots (14)$$

Based on charge balance of capacitor C2ka, it can be derived that

$$\overline{i_{2(k-1)a(off)}} D'T_s = I_0 T_s \dots (15)$$
$$\overline{i_{2ka(off)}} D'T_s = \overline{i'_{2ka(on)}} DT_s = I_0 DT_s \dots (16)$$

Where

$I_O = \frac{V_{out}}{R}$According to KCL in Figure 5(b), voltage ripple of capacitors C_{ia}(i = 2, 4 . . . 2k) can be obtained

$$C\Delta V_{c2a} = \overline{(\iota_{2ka(off)}} + \overline{\iota_{2k-2a(off)}} + \cdots \overline{\iota_{4a(off)}} + \overline{\iota_{2a(off)}} D'T_s \ldots\ldots\ldots (17)$$

$$C\Delta V_{c4a} = \overline{(\iota_{2ka(off)}} + \overline{\iota_{2k-2a(off)}} + \cdots \overline{\iota_{4a(off)}} D'T_s$$

……

$$C\Delta V_{c4a} = \overline{(\iota_{2ka(off)}} D'T_s \ldots . (18)$$

Where

$D' = 1 - D$based on the equations from (14) to (16), the equation group (17) can be reduced to the following expression:

$$C\Delta V_{c2a} = (k - 1 + D)I_0T_s \ldots (19)$$

$$C\Delta V_{c4a} = (k - 2 + D)I_0T_s \ldots (20)$$

…

$$C\Delta V_{c2ka} = (0 + D)I_0T_s \ldots (21)$$

Substituting (10) to (18), the following equation is derived:

$$C\Delta V = \left(\frac{k(k-1)}{2} + kD\right) I_0T_s \ldots (22)$$

Meanwhile, the following equation can be derived based on discharging stage of equivalent capacitor$C_{2a(eq)}$:

$$C_{2a(eq)}\Delta V = I_0DT_s \ldots . (23)$$

Based on (19) and (20), the equivalent capacitor $C_{2a(eq)}$can be expressed

$$C_{2a(eq)} = \frac{2D}{k(k-1+2D)} C \ldots . . (24)$$

Similarly, to derive the equivalent capacitance of $C_{1a(eq)}$, the following equation can be derived:

$$C\Delta V_{c1a} = kI_0T_s \ldots (25)$$

$$C\Delta V_{c3a} = (k-1)I_0T_s \ldots . (26)$$

…..

$$C\Delta V_{c2(k-1)a} = I_0T_s \ldots . (27)$$

At the same time, the following equation exists:

$$C_{1a(eq)}\Delta V' = I_0T_s \ldots . (28)$$

Where

$$\Delta V' = \Delta V_{c1a} + \Delta V_{c3a} + \cdots \Delta V_{c(2k-1)a} \ldots (29)$$

Therefore, the expression of $C_{1a(eq)}$is obtained

$$C_{1a(eq)} = \frac{2}{(k+1)k} C \ldots\ldots (30)$$

Because of the symmetry, the equivalent capacitance C1b (eq) and C2b (eq) is given as following:

$$C_{1b(eq)} = \frac{2}{(k+1)k} C \ldots . . (31)$$

$$C_{2b(eq)} = \frac{2D'}{k(k-1+2D')} C \ldots . . (32)$$

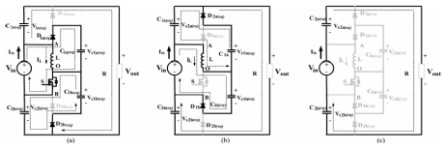

Figure 7. Three operation states. (a) State 1[0, DTs]. (b) State 2[DTs, $(D + D1)Ts$]. (c) State 3[$(D + D1)Ts$, Ts].

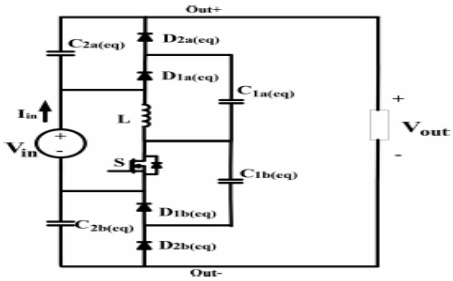

Figure 8. Equivalent even-order HBC.

The derivation of voltage and equivalent value of the equivalent flying capacitors can facilitate the output voltage calculation and ripple estimation.

C. Operation Principle of General Basic HBC

In view of the improvement technique examined in past area, the general even-series HBC in Figure 2(b) can be disentangled to a comparable HBC circuit appeared as Figure 8. Cautious examination of the topology shows that the two "support" like sub circuits are interlaced through the operation of the dynamic switch S. The aggregate output voltage of HBC is the entirety of the output voltage of two support sub circuits in addition to the info voltage. Three operation states are portrayed as Figure 7.

1) State 1[0, DTs]: In Figure 7(a), switch S is turned on and diodes $D_{1a\ (eq)}$, $D_{2b\ (eq)}$ lead while diodes $D_{2a\ (eq)}$ and $D_{1b\ (eq)}$ are conversely one-sided. The inductor L is charged by the information source. In the interim, capacitor $C_{1a\ (eq)}$ is charged by info source and capacitor $C_{2b\ (eq)}$ is charged by capacitor $C_{2b\ (eq)}$. At this interim, the accompanying conditions can be inferred in light of the inductive switching center investigation:

$$V_{A0+} = V_{in} \ldots (33)$$
$$V_{0B-} = 0 \ldots (34)$$

2) State 2[DTs,(D + D1)Ts]: As represented in Figure 7(b),when S is killed, the inductor current will free wheel through diodesD2a(eq) andD1b(eq).The inductor is shared by two charging support circles. In the top circle, capacitor C1a(eq) is discharging energy to capacitor C2a(eq) and load in the meantime. In the base circle, input source charges capacitor C1b(eq) through the inductor L. During this time interim, voltage created at AO and OB is communicated as taking after in view of inductor adjust primary:

$$V_{A0+} = -V_{in}\frac{D}{D_1} \ldots (35)$$
$$V_{0B+} = \frac{V_{in}(D+D_1)}{D_1} \ldots (36)$$

3) State 3[(D + D1) Ts, Ts]: Under specific conditions, the circuit will work under DCM operation mode, subsequently the third state in Figure 7(c) requests. At this express, the turn S is kept off. The inductor current has dropped to zero and every one of the diodes are blocked. The capacitor C2a (eq) and C2a(eq) are in series with info source to control the heap. During this time interim, voltage created at port AO is zero while at OB is Vin.

III. STEADY-STATE ANALYSIS

A. Voltage Gain Derivation in CCM Mode

In steady state, the CCM mode operation waveforms are given as Figure 9(a). The waveforms of VAO and VOB are presented based on operation principal analysis previously. Under CCM condition, D1 = 1– D = D_. Based on (6) and (8), the equivalent voltage of C2a (eq) and C2b (eq) is obtained as

$$V_{c2b(eq)} = k\frac{V_{in}}{D'} \ldots (37)$$

$$V_{c2a(eq)} = k\frac{V_{in}}{D'} \ldots (38)$$

Therefore, the voltage ratio of a general 2kth-order HBC shown in Figure 2(b) is derived as following:

$$\frac{V_{out}}{V_{in}} = 1 + 2k\frac{1}{D'} \ldots (39)$$

B. Voltage Gain Derivation in DCM Mode

Under DCM operation mode, the waveforms of voltage at input port AO, OB are shown in Figure 9(b). Based on (6) and (8), the voltage gain can be expressed as

$$V_{out} = V_{in} + 2kV_{in}\frac{D+D_1}{D_1} \ldots (40)$$

In Figure 9(b), the inductor current can be expressed as following during state 2:

$$I_L = I_{D2a(eq)} + I_{D1b(q)} \ldots (41)$$

According to charge balance principal of the circuit

$$\overline{I_{D2a(eq)}} = \overline{I_{D1b(eq)}} = I_O \ldots (42)$$

Where

$I_{D2a(eq)}$and$I_{D1b(eq)}$

is the average current in the whole switching period. As current waveforms of ID2a (eq)and ID1b (eq) should both have triangle shape, they will share same peak current value, which is half of the inductor peak current. Therefore

$$I_{D2a(eq)p-p} = \frac{1}{2}\frac{V_{in}}{L}DT_S \ldots (43)$$

The average current of ID2a(eq) in a switching period is IO , thus

$$\frac{1}{2}D_1T_S\frac{1}{2}\frac{V_{in}}{L}DT_S\frac{1}{T_S} = I_O \ldots (44)$$

This can be simplified to

$$D_1 = \frac{4I_0L}{V_{in}T_SD} \ldots (45)$$

Substituting (37) to (32), the following equation can be derived:

$$V_{out} = V_{in} + 2k(V_{in} + \frac{V_{in}^2D^2T_S}{L} \ldots (46)$$

Solving the (38) gives the voltage gain in DCM mode

$$\frac{V_{out}}{V_{in}} = \frac{2k+1\sqrt{(2k+1)^2 + k\frac{2D^2T_SR}{L}}}{2} \ldots (47)$$

C. BRM Mode Analysis

In order to derive boundary condition for CCM and DCM mode, the average power balance is used

$$V_{in}(\overline{I_L} + \overline{I_{D1a(eq)}} = V_{out}I_o \ldots (48)$$

Where $\overline{ID_{1a(eq)}} = I_O = \frac{V_{out}}{R} \ldots (49)$

Thus, the average current of IL under CCM condition is

$$\bar{I_L} = \frac{2k}{D'}\frac{V_{out}}{R} \ldots\ldots (50)$$

The current ripple of inductor is

$$\Delta i_L = \frac{V_{in}}{2L} DT_S \ldots\ldots (51)$$

Therefore, the CCM condition is

$$\frac{2k}{D'}\frac{V_{out}}{R} > \frac{V_{in}}{2L} DT_S \ldots\ldots (52)$$

The criteria can be reseriesd as

$$\frac{2L}{RT_S} > \frac{DD'^2}{2k(D'+2K)} = K_{crit}(d) \ldots\ldots (53)$$

In closed loop control of hybrid boosting converter method we wants required amount or high voltage, so we go for close loop or feedback method by using feedback method we take output voltage as feedback and compare that voltage with reference voltage or required voltage and give to PI controller and we tuned the error and produces pulses for switch which is used in hybrid boost converter. These pulses for switch used in the converter changes according to what amount of output voltage produces but in proposed method we get only one output and change that output because of there is no feedback but in extension method we use feedback we get required amount of voltage until the feedback give signals and pulses are change according to these signals we get output.

IV. SIMULATION MODELS AND RESULTS

Proposed method

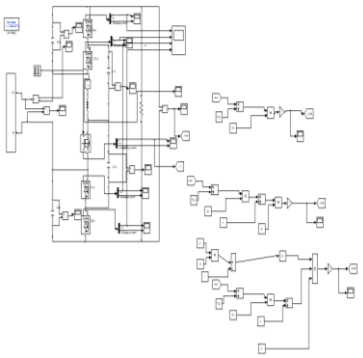

Figure 9. Simulation model of the HBC converter in proposed method

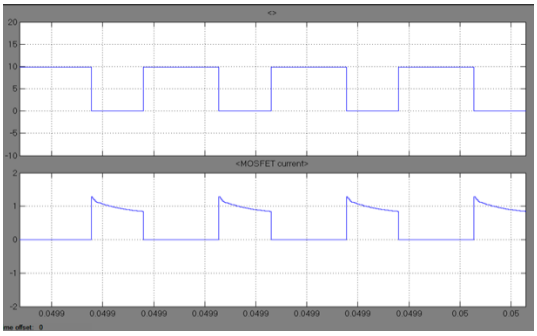

Figure 10a. Simulation waveforms. Vds and Ids

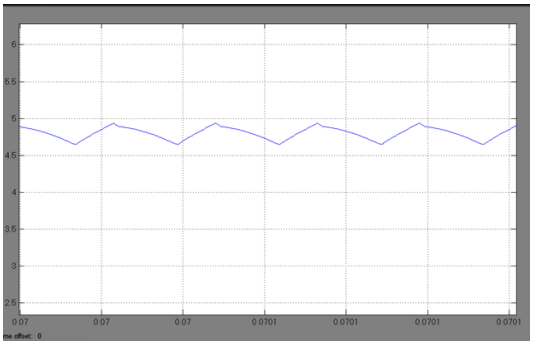

Figure 10b. Simulation waveforms. I_{in}

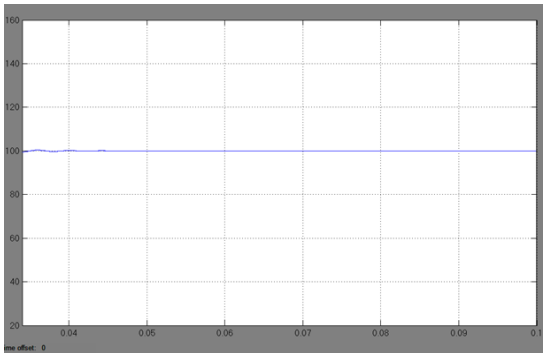

Figure 10c. Simulation waveforms. V_{out}

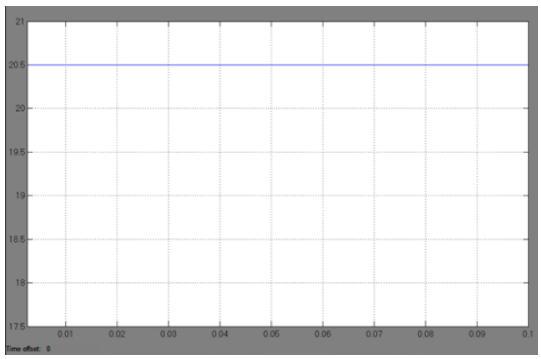

Figure 10 d. Simulation waveforms. Vin

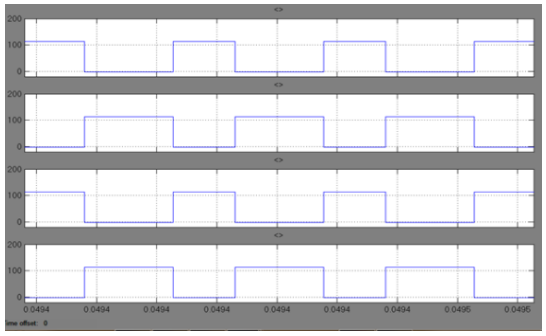

Figure 10e. Simulation waveforms. Diodes voltage: V_{d2a}, V_{d1a}, V_{d1b}, V_{d2b}

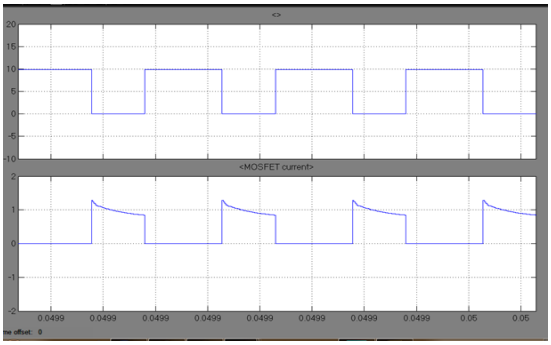

Figure 11 d. Simulation waveforms of voltage ripples under (a) D = 0.5, V_{gs} and I_{gs}

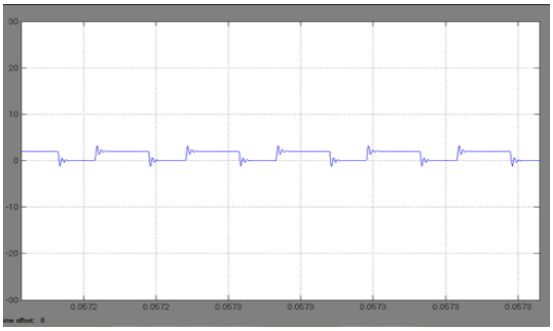

Figure 11a. Simulation waveforms of voltage ripples under (a) D = 0.5, V_{c2a}

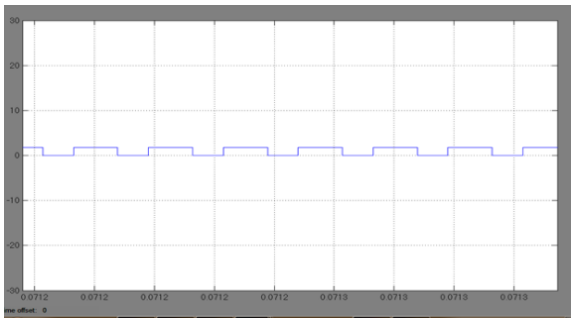

Figure 11e. Simulation waveforms of voltage ripples under (a) D = 0.8, V_{c2a}

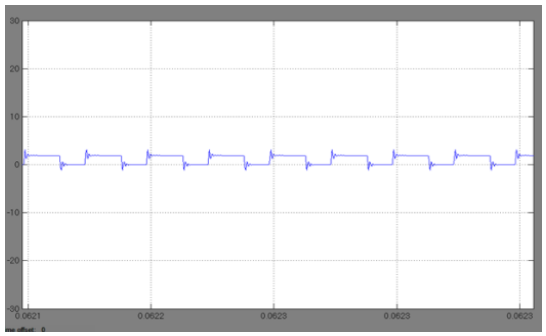

Figure 11b. Simulation waveforms of voltage ripples under (a) D = 0.5, V_{c2b}

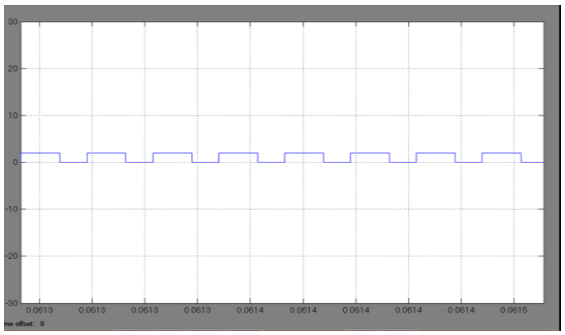

Figure 11f. Simulation waveforms of voltage ripples under (a) D = 0.8, V_{c2b}

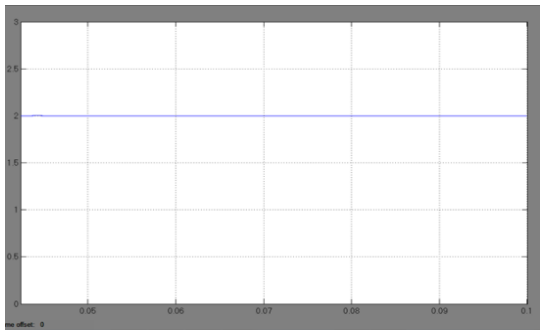

Figure 11c. Simulation waveforms of voltage ripples under (a) D = 0.5, Vout

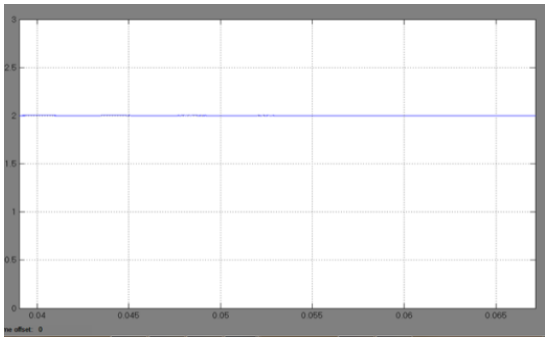

Figure 11g. Simulation waveforms of voltage ripples under (a) D = 0.8, Voutc

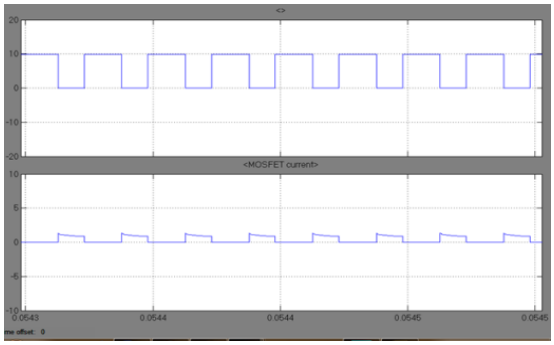

Figure 11h. Simulation waveforms of voltage ripples under (a) D = 0.8, V_{gs} and I_{gs}

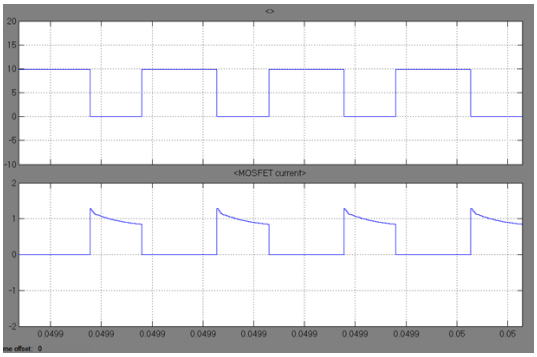

Figure 12d. Simulation waveforms of under (a) BRM condition V_{ds} and I_{ds}

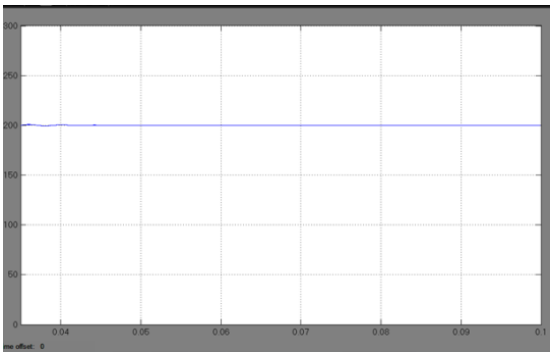

Figure 12a. Simulation waveforms of under (a) BRM condition V_{out}

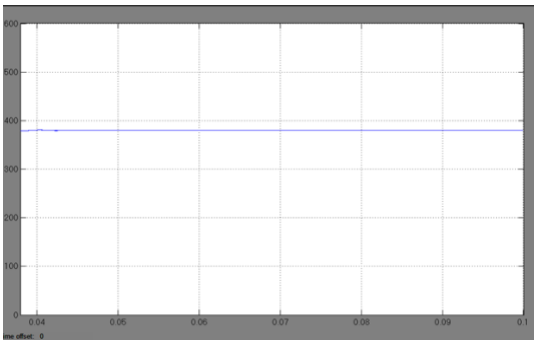

Figure 13a. Simulation waveforms of under (b) DCM condition V_{out}

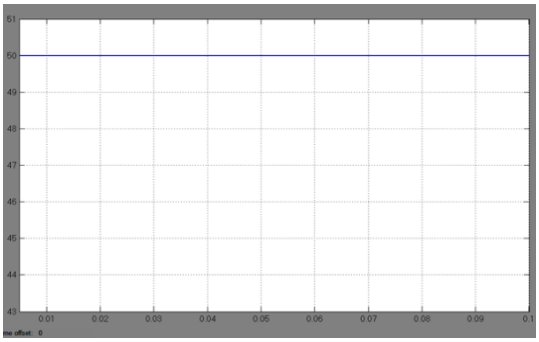

Figure 12b. Simulation waveforms of under (a) BRM condition V_{in}

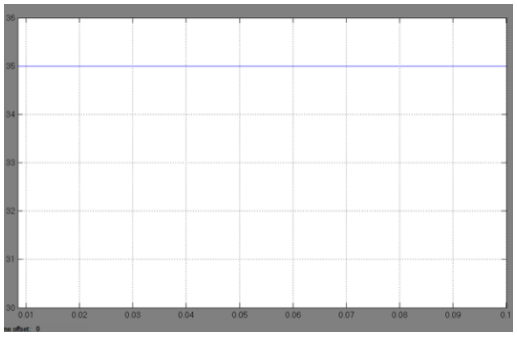

Figure 13b. Simulation waveforms of under (b) DCM condition V_{in}

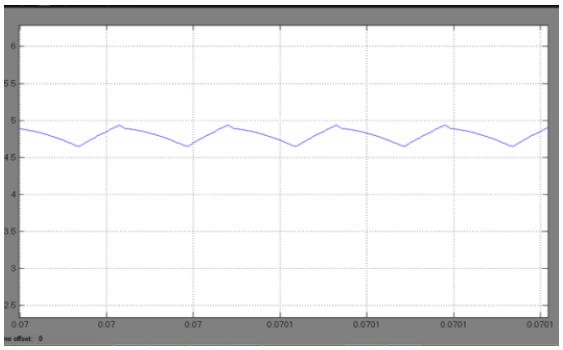

Figure 12c. Simulation waveforms of under (a) BRM condition I_L

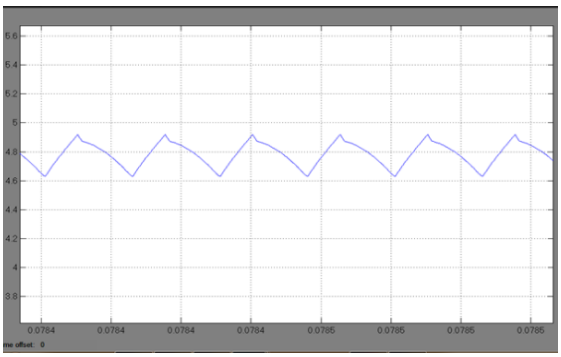

Figure 13c. Simulation waveforms of under (b) DCM condition I_L

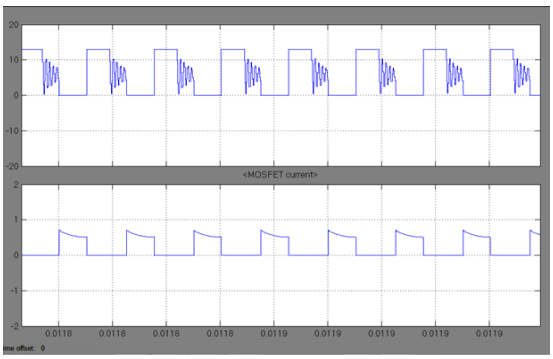

Figure 13. dSimulation waveforms of under (b) DCM condition V_{ds} and I_{ds}

Simulation Models and Results in closed loop control of HBC

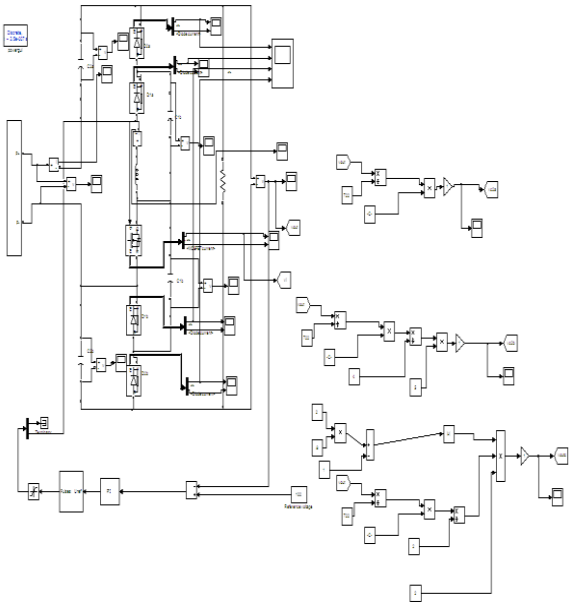

Figure 14. Simulation model of the HBC converter

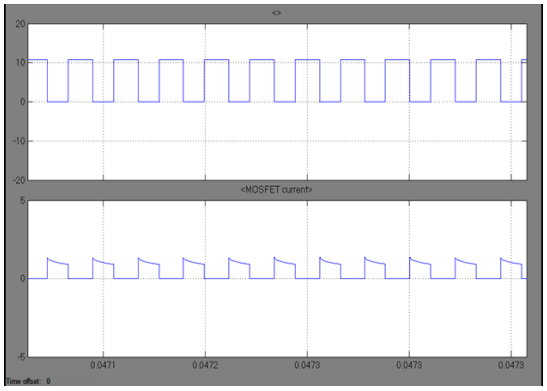

Figure 15a. Simulation waveforms Vds and Ids

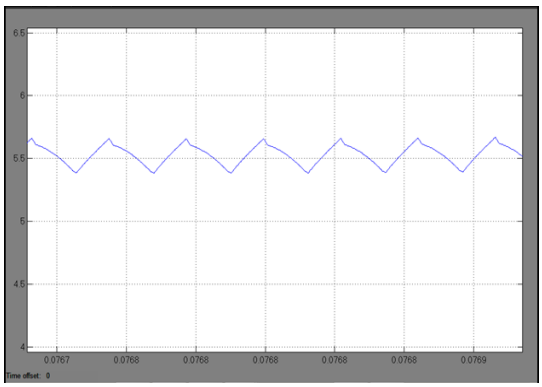

Figure 15.b Simulation waveforms I_{in}

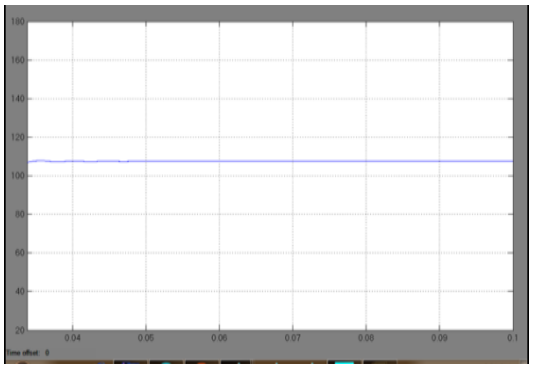

Figure 15.c Simulation waveforms V_{out}

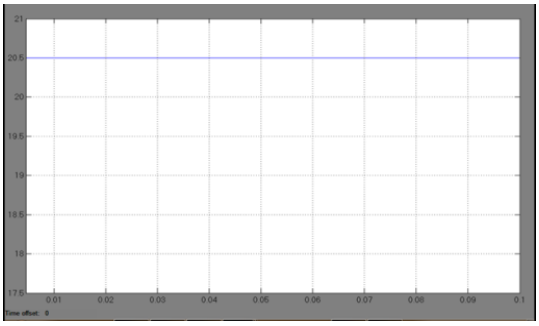

Figure 15.d Simulation waveforms Vin

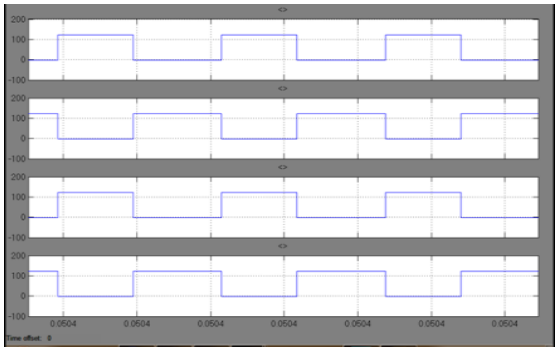

Figure 15.e Simulation waveforms Diodes voltage: Vd2a , Vd1a , Vd1b, Vd2b

Figure 16.a Simulation waveforms of voltage ripples D=0.5: Vc2a

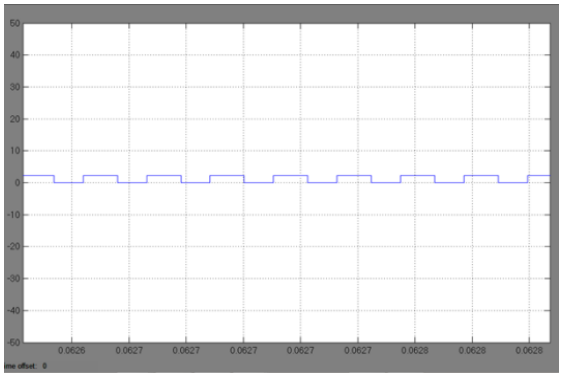

Figure 16.b Simulation waveforms of voltage ripples D=0.5: Vc2b

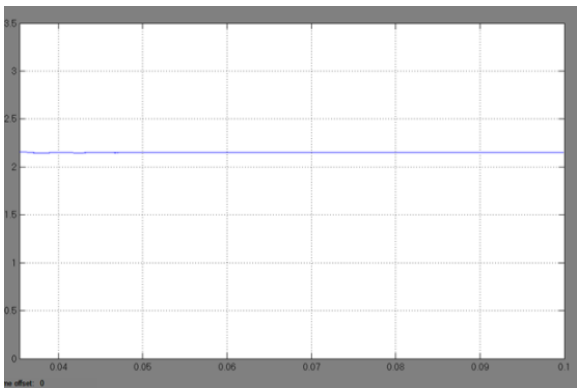

Figure 16.c Simulation waveforms of voltage ripples D=0.5: Voutc

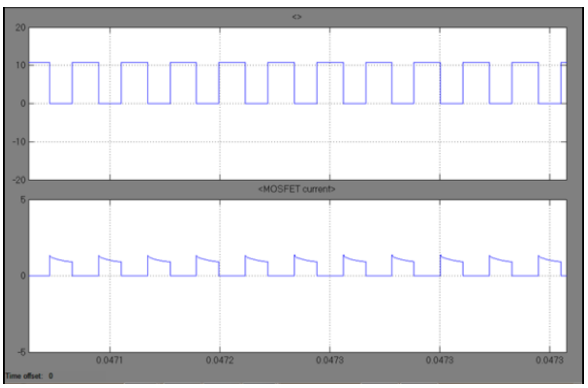

Figure 16.d Simulation waveforms of voltage ripples D=0.5: V_{ds} and I_{ds}

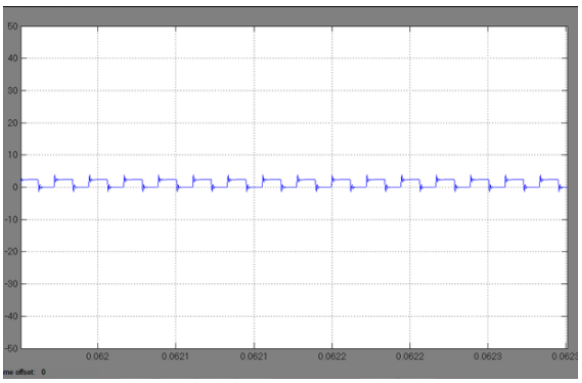

Figure 16.e Simulation waveforms of voltage ripples D=0.8: V_{c2a}

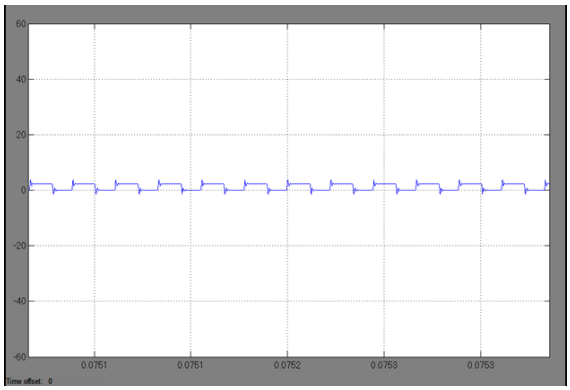

Figure 16.f Simulation waveforms of voltage ripples D=0.8: Vc2b

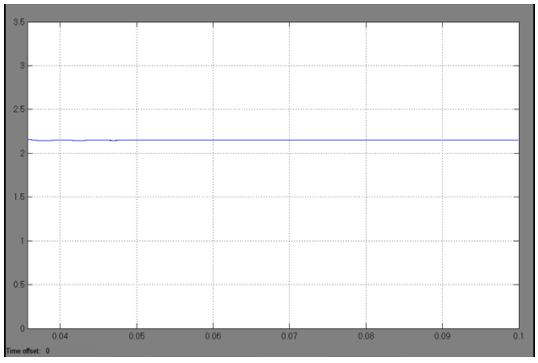

Figure 16. g Simulation waveforms of voltage ripples D=0.8: Voutc

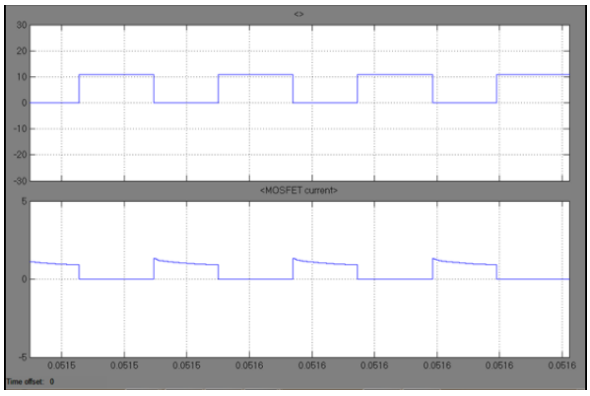

Figure 16. h Simulation waveforms of voltage ripples D=0.8: V_{ds} and I_{ds}

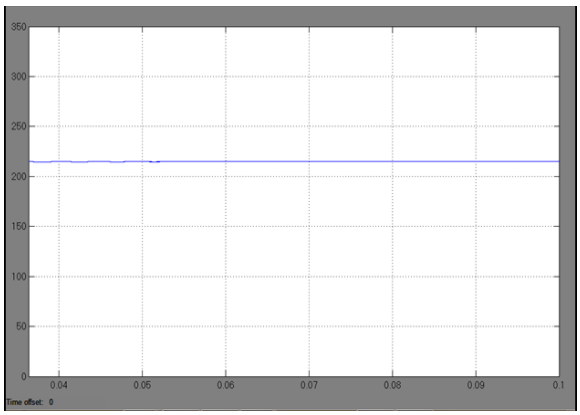

Figure 17.a Simulation waveforms in BVM : V_{out}

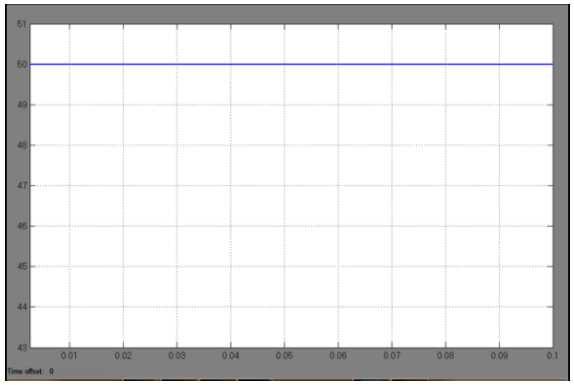

Figure 17.b Simulation waveforms in BVM : Vin

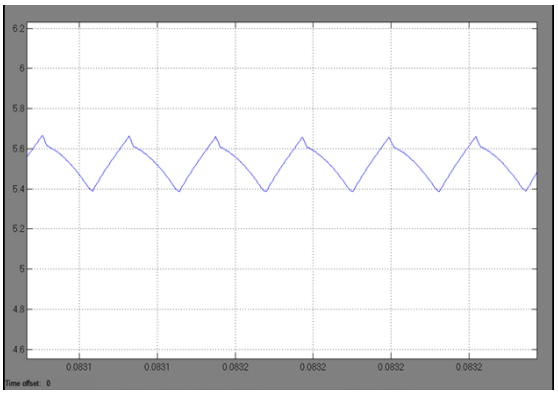

Figure 17.c Simulation waveforms in BVM : I_L

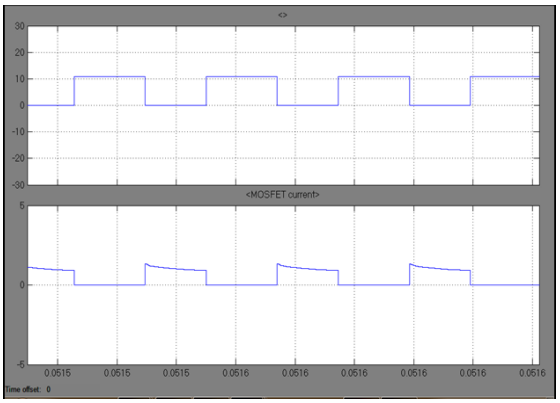

Figure 17.d Simulation waveforms: V_{ds} and I_{ds}

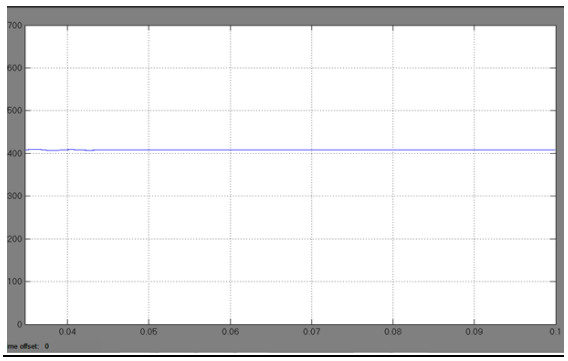

Figure 18.a Simulation waveforms in DCM : Vout

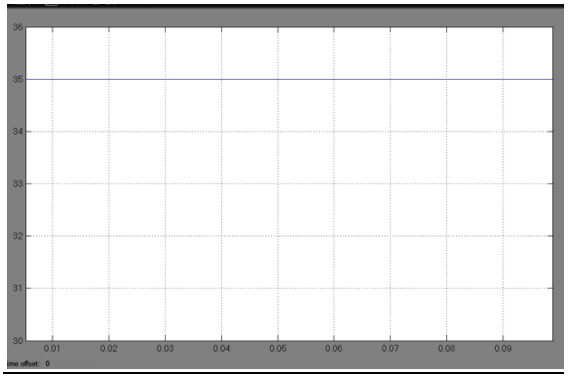

Figure 18.b Simulation waveforms in DCM : Vin

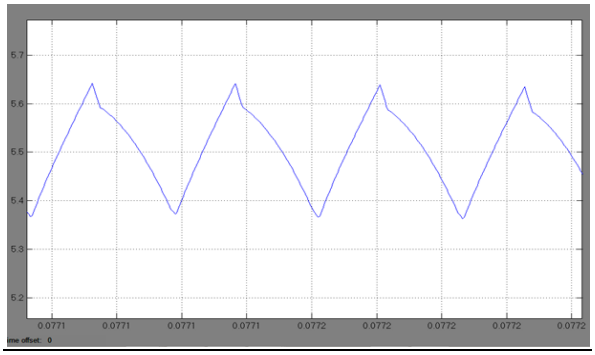

Figure 18. c Simulation waveforms in DCM: IL

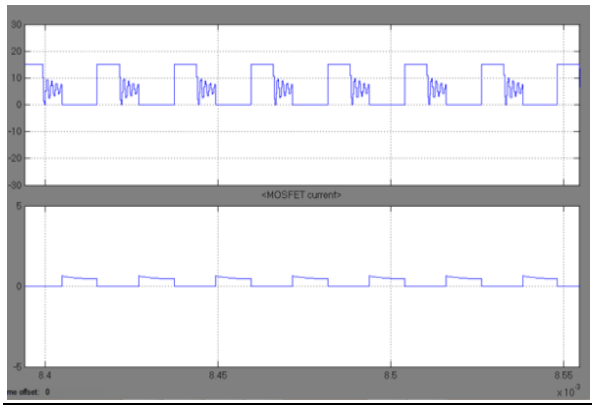

Figure 18.d Simulation waveforms in DCM : V_{ds} and I_{ds}

V. CONCLUSION

This paper presents a new HBC used here for boosting the input low voltage to elevated level voltage. In this

project we wants required amount or high voltage, so we go for close loop or feedback method by using feedback method we take output voltage as feedback and compare that voltage with reference voltage or required voltage and give to PI controller and we tuned the error and produces pulses for switch which is used in hybrid boost converter. These pulses for switch used in the converter changes according to what amount of output voltage produces but in proposed method we get only one output and change that output because of there is no feedback but in extension method we use feedback we get required amount of voltage until the feedback give signals and pulses are change according to these signals we get output.

VI. REFERENCES

[1]. W. Chen, A. Q. Huang, C. Li, G. Wang, and W. Gu, "Analysis and comparison of medium voltage high power DC/DC converters for offshore wind energy systems," IEEE Trans. Power Electron., vol. 28, no. 4, pp. 2014-2023, Apr. 2013.

[2]. J. A. Starzyk, "A DC-DC charge pump design based on voltage doubles," IEEE Trans. Circuits Syst. I Fundam. Theory Appl., vol. 48, no. 3,pp. 350-359, Mar. 2001.

[3]. F. L. Luo and H. Ye, "Positive output multiple-lift push-pull switched capacitor Luo-converters," IEEE Trans. Ind. Electron., vol. 51, no. 3, pp. 594-602, Jun. 2004.

[4]. N. Vazquez, L. Estrada, C. Hernandez, and E. Rodriguez, "The tapped inductor boost converter," in Proc. IEEE Int. Symp. Ind. Electron, Jun. 2007, pp. 538-543.

[5]. R. Wai, C. Lin, R. Duan, and Y. Chang, "High-efficiency DC-DC converter with high voltage gain and reduced switch stress," IEEE Trans. Ind.Electron., vol. 54, no. 1, pp. 354-364, Feb. 2007.

[6]. J. Lee, T. Liang, and J. Chen, "Isolated coupled-inductor-integrated DC-DC converter with no dissipative snubber for solar energy applications,"IEEE Trans. Ind. Electron., vol. 61, no. 7, pp. 3337-3348, Jul. 2014.