Study of Jtag-Tap Controller for Board Level Testing

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ABSTRACT

This paper gives the detailed study of Test Access Port (TAP) and its functions associated with boundary scan testing for various Unit under Test (UUT).It also explain the boundary scan instructions and the signals through the TAP controller. Supports the applications of testing the devices on various factor using JTAG standard.

I. INTRODUCTION

Boundary scan testing is one of the Design for Testability (DFT) which is special method for system level testing. Boundary scan method is formally called as JTAG, is the standard given by the association IEEE. Boundary scan method can test both the digital and the memory blocks and also supports components and the system level. In these paper, the study of JTAG is discussed for different UUT for board level testing.

Table 1. Required Instruction for JTAG

Instruction	Status
BYPASS	Mandatory
CLAMP	Optional
EXTEST	Mandatory
HIGHZ	Optional
IDCODE	Optional
INTEST	Optional
RUNBIST	Optional
SAMPLE/PRELOAD	Mandatory
USERCODE	Optional

Testing of UUT

The standard IEEE 1149.1 is tested for various UUT under the constraint like cluster test, interconnection test, infrastructure test and memory test. Fig 1 explains the mechanism of testing different UUT through the signals from TAP controller.

The infrastructure tests checks the connections between Boundary Scan circuitry and test bus as well as the most important registers within the Boundary Scan circuitry

The interconnection test checks the connections between Boundary Scan pins. This test considers transparent buffers and disables other buses.

The cluster test checks a non-Boundary Scan cluster by means of the surrounding BScan pins.

The completely-automated cluster test permits you to test combinatorial non-Boundary Scan clusters without much effort.
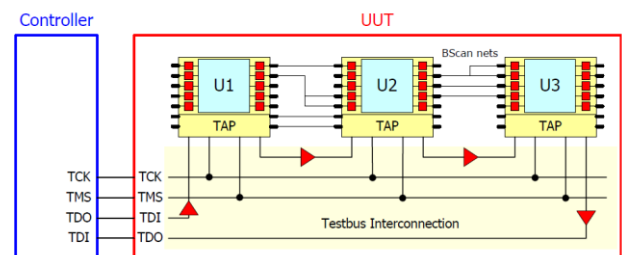

Figure 1. Block of testing different UUT

The TAP state diagram has two main branches and two idle states. Shift IR and Shift DR states are used to insert instructions and test data into the BS device. These are the most important states. TMS signal is used to move through the states While the TAP controller is the heart of any 1149.1 implementation, the instruct-ion register and instruction register decoder can be thought of as the brains. The instruction register stores information concerning which test register or test circuitry is active. Fig 2 shows the state diagram of controller for any boundary scan instructions.

For any instruction code selected, an associated register and/or test circuit is also selected. This is one of the requirements stated in the 1149.1 standard.

Instructions are shifted into the instruction register when the TAP controller is in the SHIFT-IR state and become active when the controller enters the UDPATE-IR state.
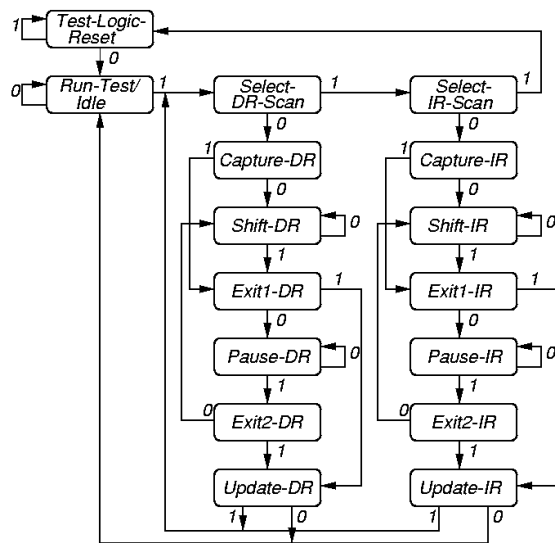

Figure 2. TAP Controller state Diagram

- Capture—DR: Each instruction must identify one or more test data registers that are enabled to operate in test mode when the instruction is selected. In this controller state, data are loaded from the parallel input of these selected test data registers into their shift-register paths on the rising edge of TCK.

- Shift-DR: Each instruction must identify a single test data register that is to be used to shift data between TDI and TDO in the Shift-DR controller state. Shifting allows the previously captured data to be examined and new test input data to be entered. Shifting occurs on the rising edge of TCK in this controller state. In the

- Shift-DR controller state, the TDO output is active (it is inactive in all other controller states except the Shift—IR state).

- Update-DR: This controller state marks the completion of the shifting process. Some test data registers may be provided with a latched parallel output to prevent signals applied to the system logic, or through the chip's system pins, from rippling while new data are shifted into the register. Where such test data registers are selected by the current instruction, the new data is transferred to their parallel outputs on the falling edge of TCK in this controller state.
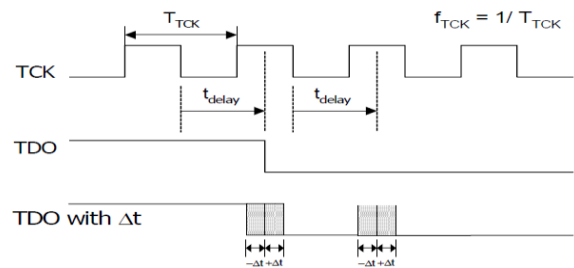

Figure 3. Timing diagram for TAP signals

The delay time (tdelay) to be entered is the time between the falling TCK edge at the controller's connector until the respective TDO signal edge from the UUT arrives at the controller's connector.

- ✓ tdelay includes the delay of **Distance POD** and/or testbus cable and UUT.
- ✓ Δt is the delay time tolerance. It is used to compensate inaccuracies of delay time and TCK frequency.
- ✓ If the exact value of tdelay is known, a value of 5 ns should be entered as Δt.

- ✓ The higher the desired test frequency is, the more accurately Δt has to be defined. The TCK frequency is set by the software according to the condition: **FTCK <= 1/ (4 x (Δt + 2 ns))**

Figure 3 shows that +Δt and −Δt form an undefined area where TDO is not exactly predicted.

However, it is important for the Boundary Scan technique that a rising edge of TCK may only occur after this undefined area to ensure a safe value for TDO. The distance between two undefined areas has to be at least as wide as an undefined area to achieve independence of the delay time.

Test Access Port (TAP) includes these signals:
Test Clock Input (*TCK*) -- Clock for test logic Can run at different rate from system clock

Test Mode Select (TMS) -- Switches system from functional to test mode

Test Data Input (TDI) -- Accepts serial test data and instructions -- used to shift in vectors or one of many test instructions

Test Data Output (TDO) -- Serially shifts out test results captured in boundary scan chain (or device ID or other internal registers)

Test Reset (TRST) -- Optional asynchronous TAP controller reset

II. REFERENCES

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