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Design of Reversible Logic Alu Using Quantum Dot Cellular Automata

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ABSTRACT

Conservative logic is a logic which reflects the property that there is equal number of one's in the inputs as well as in the output. It can be reversible or irreversible in nature. Reversibility is nothing but the circuit exhibits one-to-one mapping between input and output vector, and also represents for each input vector there is an unique output vector and vice versa. Reversibility is mainly preferred because it can provide the methodology for designing low power circuits. Unlike computation mechanisms that involve the transfer of electrons, as in CMOS gates, QCA computation does not involve electron transfer between adjacent QCA cells. Hence power dissipation is very less in circuits designed with QCA cells. Since only few electrons are involved in QCA computations, it is susceptible to thermal issues. Therefore it is important to consider power as an important parameter during the QCA design process. The major advantages of this technology are lesser power dissipation, improved speed and dense structures. In this project design of reversible combinational circuits like ALUs which is designed with new gates, Mux, Adders, based on QCA technology is proposed to provide advantages like reduction in no of quantum cost, garbage outputs, complexity of gates, area.

Keywords: Arithmetic logic unit (ALU), Reversible logic, QCA, Quantum Cost, Garbage Outputs.

I. INTRODUCTION

As digital systems are becoming faster and complex therefore the power consumption by circuits becomes the major issue. In the circuits that are not reversible, for every bit of information lost in logic computations, kT*log2 joules of heat energy is generated, where k is Boltzmann's constant and T is the absolute temperature at which computation is performed[1]. This power dissipation can be reduced by using reversible logic [2]. Also, Bennett [3] showed that in order to keep a circuit away from dissipating any power, it had to be composed of reversible gates. Computation that is currently carried out depends upon the number of operations that will destroy the information e.g. in AND gate there are two inputs and one output, the two inputs will be either be 1 or 0 and the output depends upon the two inputs [4]. The output is 1 if both the inputs are 1 and the output is 0 if either of the input is 0 or both inputs are 0. Every time when the gate's output is 0 we lose information, because we do not know that the input lines are in which of the three possible states (0 and 1, 1 and 0, or 0 and 0). In fact, any logic gate that has more input lines than the output lines inevitably discards information, because we cannot deduce the input from the output.

The continuous scaling down of feature size has pushed CMOS technology to approach its practical and theoretical limits [5]. Lot of research efforts at nano scale is in progress to explore alternate viable technologies for future integrated circuits (ICs).

While exponential decreasing the feature size in CMOS (complementary metal-oxide-semiconductor)

technology, devices are getting more prone to high leakage current and also getting more sensitive to circuit noise [6]. Landauer computed that in each irreversible operation the heat generated will be in the order of KT, the power dissipation is mainly due to the erasure of the intermediate states that are been used in the computation process. When one bit of data gets erased means the energy dissipation will be in terms of KTln2, where K is the Boltzmann's constant and T is the absolute temperature [7].

QCA provides an alternative to the silicon technology.QCA based circuits have the advantage of high speed, high integrity and low power consumption [8]. Also QCA circuits have the advantage of high parallel processing.

QCA is emerging as a potential technology that could be used in future computing circuits/systems replacing existing Silicon technology. It provides a new computing and information transformation paradigm [9]. It is a transistor less technology that uses a square nanostructure called QCA cell comprising of 4 quantum dots [10]. Two free electrons are introduced in a four quantum dot based QCA cell which can tunnel amongst the quantum dots and take seat in any one of them. The two free electrons settle into two stable states within QCA cell that are used to encode two binary states in digital circuits. QCA cells are arranged in arrays for a particular computation and communicate with each other by Coulomb interactions. The alignment of electrons at edges of array provides the computational output. The alignment of polarizations in a QCA circuit is managed by applying an external clock and functions according to the rules of Boolean algebra [11].

QCA cells perform computation by interacting coulombically with neighboring cells to influence each other's polarization. A high-level diagram of a four-dot QCA cell appears in Figure 2.1. Four quantum dots are positioned to form a square. Quantum dots are small semi-conductor or metal islands with a diameter that is small enough to make their charging energy greater than k BT (where kB is Boltzmann's constant and T is the operating temperature) [12]. (In the future, they will shrink to regions within specially designed molecules.) If this is the case, they will trap individual charge barriers.
Exactly two mobile electrons are loaded in the cell and can move to different quantum dots in the QCA cell by means of electron tunneling.
Columbic repulsion will cause the electrons to occupy only the corners of the QCA cell resulting in two specific polarizations [13].

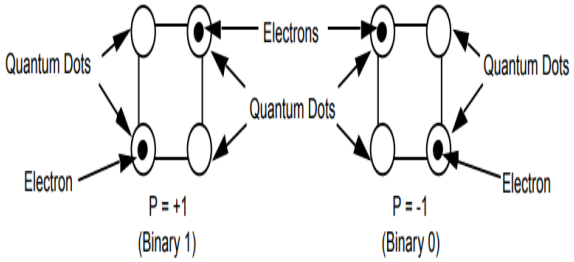

Figure 1. QCA cell polarizations and representations of binary 1 and binary 0.

An ALU is very important part of a computer. It is basically considered as the heart of a computer. It allows the computer to perform many other arithmetic and logic functions. Since every computer needs to be able to do these functions, they are always included in a CPU [14]-[15]. A simple ALU consists of two operands, one control signal to select the operation to be performed and one output signal to give the result of desired operation. Reversible ALU is designed for modular arithmetic operations apart from logical operations.

II. PROPOSED REVERSIBLE GATES

The Proposed Gates satisfies the property of **Reversibility** and **Universality**. Reversibility represents the unique mapping between the input and the output bit vectors [3]. Universality represents reversible in the realization of AND, OR and NOT operations. The proposed structures undergoes reversibility by execution and satisfies the property of Universality by executing AND, OR and NOT operations. This novel gates with different operation

help in design Arithmetic and logical unit. The representation of the novel reversible gate called Reversible Gate 1, Reversible Gate2 and Reversible Gate 3; Reversible Gate 4 along with their output functionality is mentioned in Figure 1, Figure 2, Figure 3, and Figure 4.

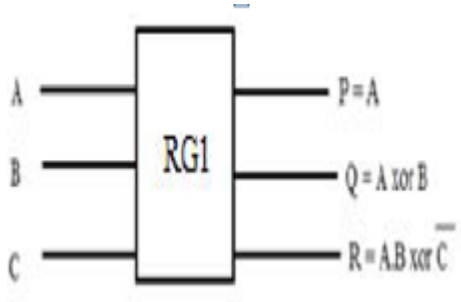

Figure 2. Reversible gate1

The above shown Figure is one of the proposed reversible gates. As it is reversible gate the total number of inputs is equal to the total number of outputs. Which represents the operations for the inputs A, B, C as P is A, Q is A XOR B , R is AB XOR ~C.

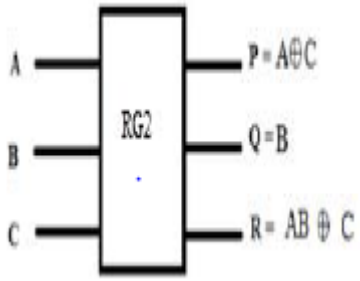

Figure 3. Reversible gate 2

The reversible gate2 (RG2) shows the functionality of P is A xor C, and keeping output same as input for Q, R is A AND B XOR C.

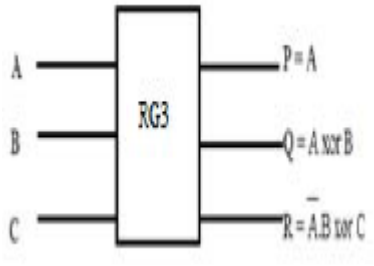

Figure 4. Reversible gate3

The reversible gate 3 performs operations as output P is passed by the input A, Q is A XOR B, R is ~A AND B XOR C

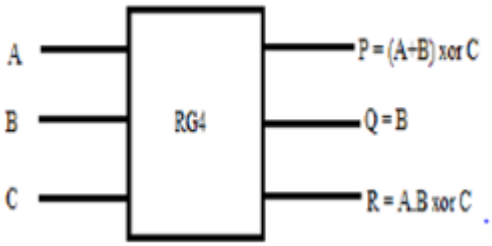

Figure 5 . Reversible gate4

These gates can be used in the ALU design to obtain Significant reduction in the reversible logic parameters.

HNG Gate , It is a 4x4 gate and its logic circuit is as shown in the figure1. It has quantum cost six. It is used for designing adders like ripple carry adder. It reduces the garbage and gate counts by producing the sum and carry in the same gate.

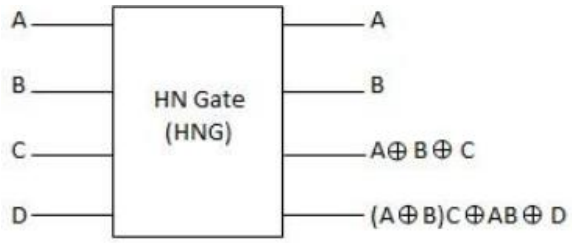

Figure 6 . HN gate

III. ARCHITECTURES IN QCAD

A. Multiplexer Design

The Multiplexer design is based on the majority configuration of the QCA cells. The Multiplexer

design is as follows:

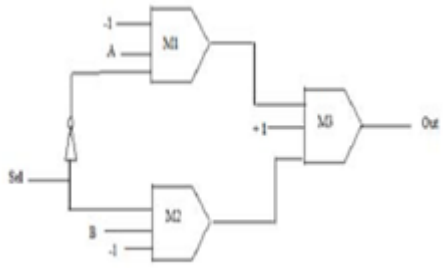

Figure 7. MUX with majority gate

Figure 7 shows the Multiplexer design based on the majority configuration of the QCA cells. Three majority gates and one inverter are needed to construct the multiplexer. The majority gate representation of the function is as follows:

F = M3 (M1 (Sel, A ,0), M2 (Sel,B,0),1)

Where M1, M2, M3 denotes the majority cells and 'Sel' denotes the select lines.. The input and the constant cells are placed in a proper way so that the outputs of the two majority gates M1 and M2 are propagated to the third majority gate M3 (OR operation) with equal time delay.

B. Arithmetic and Logical unit

In the Processor architecture the ALU is considered as the heart of the system. An arithmetic and logical unit should be capable of producing larger number of possible arithmetic and logic functions. Based on the reversible gate structure the ALU design can be made remarkably, the reversible gates should maximize the operations of arithmetic and logical unit. But the cost of the circuit selects lines used for designing the circuit garbage outputs of the circuit design, circuit delays must be reduced, to ensure this at each stage verification should be made whether the reversibility is present in each and every part of the design and the outputs should propagate in a manner to achieve the correct operation of the circuit and also to achieve reversibility of the design.

a. Functions of Proposed Arithmetic Unit

The Arithmetic unit is responsible for handling the Arithmetic operations executed by the program . The proposed arithmetic unit is designed based on the novel reversible gates. The functions of the proposed arithmetic unit are shown in Table 1.

Table 1. Functions of arithmetic unit

Control Inputs			Output	Results
C_0	C_1	C_2		
0	0	0	B	Transfer B
0	0	1	B+1	Increment B
0	1	0	A+B	Addition
0	1	1	A+B+1	Addition with carry
1	0	0	A+B	1's complement subtraction
1	0	1	A+B+1	2's complement subtraction
1	1	0	B-1	Decrement B
1	1	1	B	Transfer B

The output function is realized based on the equation 1,

OUT = (AC0+AC1) xor B xor C2 --------- (1)

Where A, B are the inputs given to the reversible gates and C0, C1, C2 are the control inputs. Based on the control inputs the arithmetic functions like transfer operation, increment, decrement, addition, addition with carry, 1's complement subtraction, 2's complement subtraction etc are been performed for the ALU operation.

b. Design of Arithmetic Unit Based On Novel Reversible Gates

The design of Arithmetic Unit composes of five Reversible Novel structures. The design constitutes of three Reversible gate2 (RG2), two Reversible gate3 (RG3) and one Reversible gate4 (RG4). Its corresponding Quantum Cost is 32. The Number of Garbage outputs used here is 6. The number of constant inputs employed here is 1.

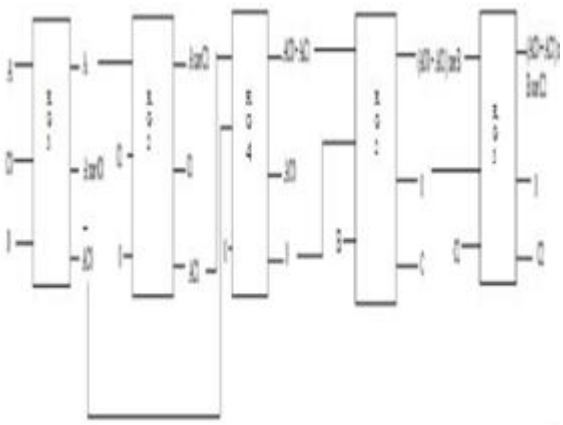

Figure.9 Design of Arithmetic Unit

The Figure 9 shows the design of Arithmetic unit. The operation of Arithmetic unit is as follows initially for the RG3 gate the inputs given will be A, C0 and 0. C0 is the control inputs given to the arithmetic unit design and 0 is the constant inputs in the design. The resultant outputs from the RG2 gate is A, A xor C0, A'C0. The output A is propagated to the next reversible gate RG2, where the second output A xor C0 is considered as the garbage output (that is unused output in the design). Hence the next reversible gate has an input of A, C1, 0 where c1 is the control inputs and 0 is the constant inputs the procured output will be A xor C1, C1, AC1, where A xor C1 and C1 is the garbage output and AC1 is propagated to the next Reversible gate. The next reversible gate used is RG4, the inputs given to RG4 is A'C0 which is the output received from the RG3 is propagated to this RG4 gate as an input and the second input will be AC0 which is the output obtained from the RG2 gate is propagated as the input to RG4 and the another input will be 0 the corresponding outputs obtained from the reversible gate4 is AC0+AC1, A'C0 and 0. Here A'C0 is considered as the garbage output function. The outputs AC0+AC1 and 0 is propagated back to the next stage of the process. The next reversible gate2 takes the inputs AC0+AC1, 0 and B and performs the corresponding operation with respect to the gate and procures the outputs. The received output from RG2 is (AC0+AC1) xor B. Here the garbage output obtained is C1. At the final stage the outputs (AC0+AC1) xor B and 0 is propagated to the next stage of the RG2 with an additional input of C2, where C2 is the control inputs. The obtained output from the RG2 is (AC0+AC1) xor B xor C2, 0, C2. The outputs C2 and 0 is taken as the garbage outputs. For example, when the control input C0, C1, C2 is equal to 111, the output from RG3 is A', the output from RG2 is A, by giving this two input to the RG4 gate the respective output will be A'+A this function is given as the input to the RG2 gate, the obtained output is B. Then this output is propagated to RG2 as the input after getting processed, the output obtained from RG2 is B. Therefore for the control input combination of 111 the transfer operation (B) is carried out.

c. Functions of Proposed Logic Unit

The Logical unit is the another important constituent in the Central Processing Unit as it is responsible for handling the logical operations executed by the programmer. The proposed design of logical unit design is based on the novel reversible gates. The functions of the proposed logical unit are shown in Table 2. The functionalities of Logical unit can be designed by the output equation as follows:

OUT = A'B'C0+AB'C1+A'BC2+ABC3 ---- (2)

Table 2. Table for Logical functions

Control Inputs				Output	Results
C0	C1	C2	C3		
0	0	0	0	0	-
0	0	0	1	A.B	AND
0	0	1	0	B	COPY
0	1	0	1	A	COPY
0	1	1	0	A xor B	XOR
0	1	1	1	A+B	OR
1	0	0	0	(A+B)'	NOR
1	0	0	1	(A xor B)'	Equal
1	0	1	0	A'	NOT
1	1	0	0	B'	NOT
1	1	1	0	(A.B)'	NAND
1	1	1	1	1	Constant

The value of C0, C1, C2, C3 is taken as the control inputs based on the control input values that is by changing the inputs combinations of 0's and 1's the respective logical functions can be obtained. The obtained logical functions from the above control

inputs are AND, COPY, XOR, OR, NOR, Equal, NOT, NAND and Constant.

d. Design of Logic Unit Based On Novel Reversible Gates

The proposed design of logical unit is based on the proposed novel reversible structures. The logical unit comprises of nine novel reversible gates. Its corresponding Quantum Cost is 32. The Number of Garbage outputs used here is 6. The number of constant inputs employed here is 1.

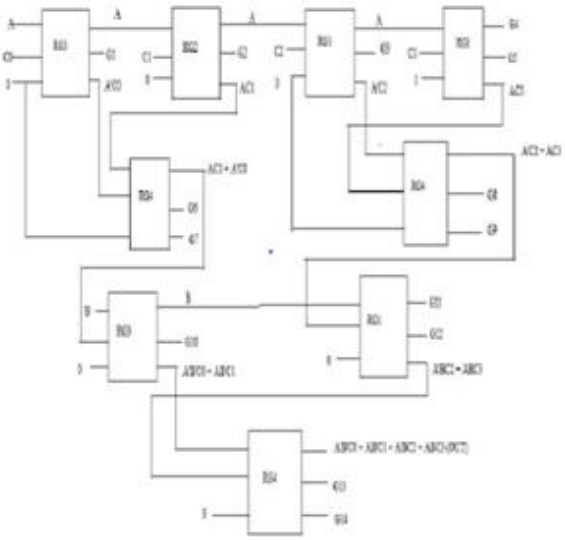

Figure 10. Design of Logic Unit

The Figure 10 depicts the design of Logical Unit. The operation of Logical unit is as follows: Initially the input applied to the reversible gate3 is A, C0 and 0, where C0 is the control inputs After proceeding over the RG3 gate operation the corresponding obtained output will be A, A'C0 and one Garbage output (unused function in the circuit). The obtained output A from the RG3 gate is given to the next reversible gate RG2. The RG2 which takes the input A, C1, 0. After preceding over RG2 operation the obtained output function will be A, AC1 and one Garbage output. The RG4 takes two inputs that is A'C0 from RG3 and AC1 from RG4 the obtained output will be A'C0+AC1 and which includes two garbage outputs. The obtained output from RG2 A is given as the input to the RG3 gate with an additional input of C2 and 0, where C2 is the control input and 0 is the constant input to the reversible gate. The obtained output from RG3 is A, A'C2 with an additional of one garbage output. Next the output from RG3 is given to RG1 and it takes the input of C3 and 1, Where C3 is the control input and 1 is the constant input. The obtained output from RG1 includes two garbage outputs with an additional output of AC3. The outputs from RG3 and RG1 gate A'C2 and AC3 respectively is given to the RG4 gate with an additional input 0 obtained from RG3 gate. The obtained output from RG4 is A'C2+AC3 with an additional output of two garbage's. Further one of the output from RG4 (AC1+A'C0) is given to the RG3 gate with an additional input of B and 0, where 0 is the constant input provided to the gate. The output of RG3 gate is B, A'B'C0 + AB'C1 with one garbage output. At the next stage the output obtained from RG3 is given to RG1 and the output obtained from

A'C2+AC3 is given as the input to RG1 with the additional input of 0. The obtained output from RG1 is A'BC2+ABC3 with the two garbage outputs. At the next stage the outputs from RG3 and RG1 A'B'C2+AB'C1 and A'BC2+ABC3 respectively given as the input to RG4 gate with an additional constant input of 0. The additional output from the RG4 includes additional two garbage's. Hence the total reversible gate required to design the logical unit will be 9. The total garbage outputs obtained is 14. The number of constant inputs employed in the logical unit design is 2 as the constant inputs are getting propagated to the various reversible gates in the circuitry. C0, C1, C2, C3 are the control inputs in the design corresponding to the control inputs the logical functions can be preceded. The control inputs should be increased to perform more logical operations. For example, for the control input combination 0001, from the gates RG3, RG2, RG1 only the garbage values will be generated. From the gate RG4 the output will be AC3, this output is further given to RG1 which gets multiplied by B and the corresponding output from RG1 is ABC3, this function is given as the input to the RG4 gate with the other inputs which is generated as garbage's. Hence the final output obtained from RG4 gate is AB

that is the multiplication operation is carried out for the corresponding control input combination of 0001. The design of Arithmetic unit and Logical unit should be integrated together in order to form a complete design. The integration can be done by using the multiplexer. Where the multiplexer receives the inputs from the arithmetic and logical unit and depending upon the select lines the required operations will be performed.

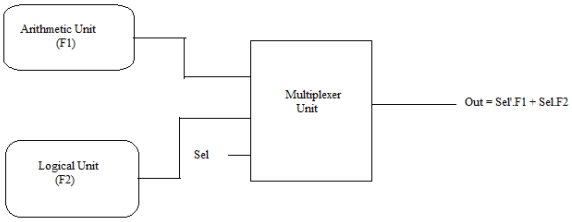

Figure 11. Integration of Arithmetic and Logical Unit

Figure 11 shows the Integration of Arithmetic and Logical Unit. The multiplexer design takes the input F1 from the arithmetic unit and F2 from the logical unit and sel is the select lines. The output of the multiplexer will be satisfying the equation 4.

OUT = SEL'.F1 + SEL.F2 ------ (4)

Table 3. Integration of ALU in MUX table

SEL	OPERATION	OPTIONS
0	Arithmetic operation	Add, Sub, Transfer, Complement etc…
1	Logical operation	AND, XOR, OR, COPY etc…

When the select line is equal to 1 the Logical operation will be performed. When select line is equal to 0 the Arithmetic operation will be performed. On selecting F1 the arithmetic operations like transfer operation, increment, decrement, addition, addition with carry, 1's complement subtraction, 2's complement subtraction etc are been performed. On selecting F2 the logical operations like AND, COPY, XOR, OR, NOR, Equal, NOT, NAND, Constant is performed. As compared to the existing multiplexer design the multiplexer design based on the majority gate configuration is comparatively better in terms of the number of majority gates used as the multiplexer design is based upon the majority cell configuration. The one bit ALU is extended to any number of bits by integrating the multiplexer design. The fixed point ALU can be achieved by this integration of the arithmetic unit and logical unit by using multiplexer.

IV. RESULTS AND DISCUSSION

The MUX, Ripple carry adder and Arithmetic unit, Logical unit, Multiplexer based on majority gate configuration, Integration of Arithmetic and Logical unit has been designed. They are simulated using the QCA Designer tool. The comparison between the existing and the proposed ALU has been performed in this section.

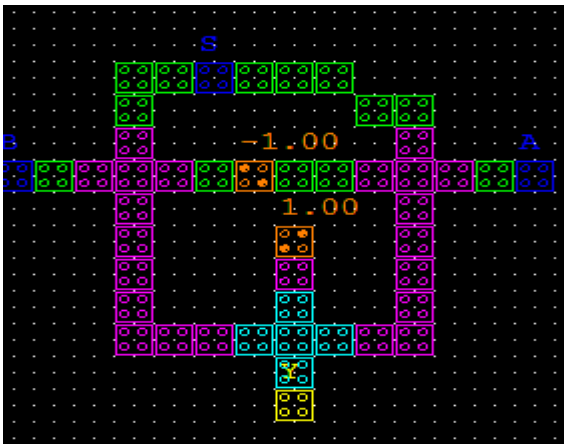

Figure 12. QCA layout for the Multiplexer.

Figure 12 depicts the design of Multiplexer with three majority gates. Having constant values -1 for 0 and +1 for 1 to get logic 1 and -0 constant values.

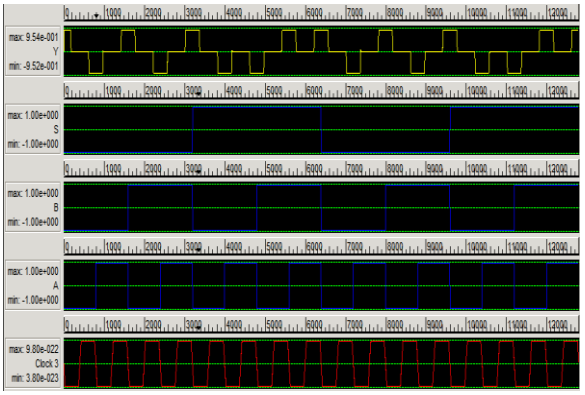

Figure 13. Simulation result for Multiplexer.

This above figure shows the output result for the multiplexer.

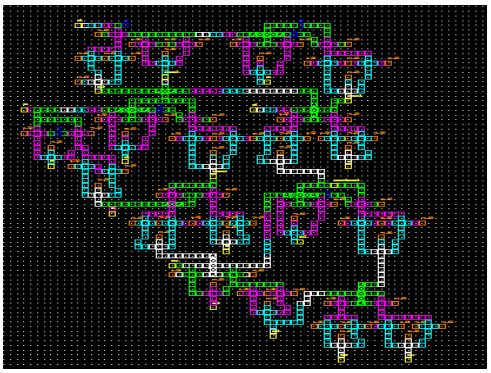

Figure 16. QCA layout for the Logic unit

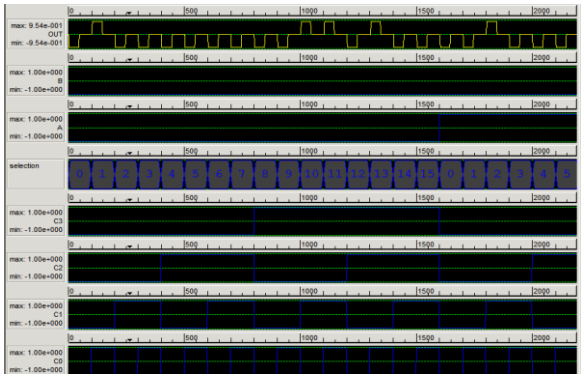

Figure 17. Simulation result for the Logic unit

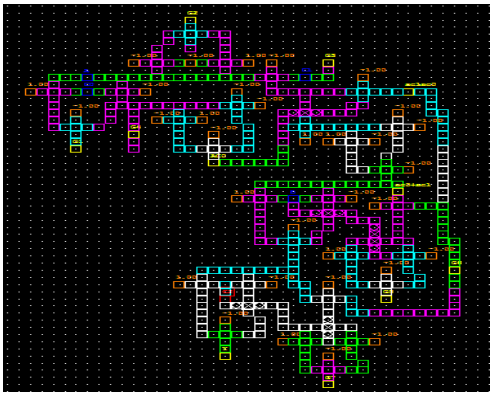

Figure 18. QCA layout for the Arithmetic unit.

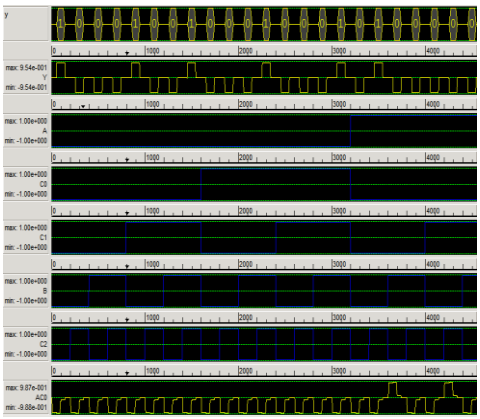

Figure 19. Simulation output for the Arithmetic unit

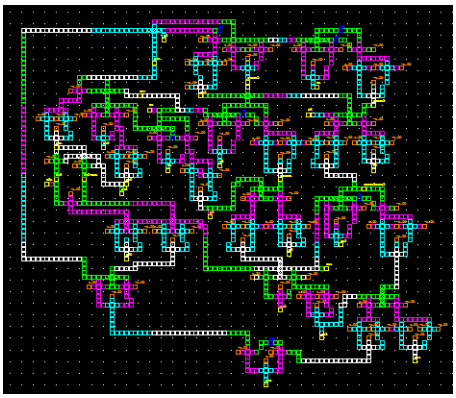

Figure 20. QCA layout for the ALU.

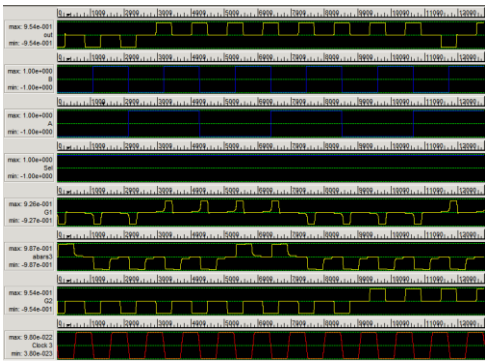

Figure 21. Simulation result for the ALU

V. CONCLUSION AND FUTURE WORK

In this paper three novel Reversible Gates are proposed for ALU. The proposed gates are having minimum number of cells as compared to the existing gates such as Fred kin gate. The proposed gates show improvement in terms of optimization parameters in reversible logic as compared to the existing reversible gates. The design is validated in the QCA platform. The proposed QCA based MUX, Ripple carry adder and arithmetic and logic unit shows prodigious improvement in the design parameters of reversible logic and the simulation constraints such as area, simulation time and number of cells employed in the design. Hence the proposed system has minimum area with QCA and low power dissipation with Reversible Logic. The proposed ALU can be used in the Processor architecture and in Future the entire architecture can be designed using the reversible logic concepts and gates.

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