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Modulation Techniques for Transformer-less Inverters

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ABSTRACT

In grid connected applications which is having low power, a single-phase inverter can have a good performance. As can be inferred from the title, the PV inverter is a key element of grid connected PV power system whose main function is the conversion the DC power generated by PV panel into the grid synchronized AC power. These inverters use either a low frequency transformer or a high frequency transformer. In PV applications it has been studied that the transformer can be removed in order to reduce the losses, cost, size and weight of the system simultaneously increasing the system performance. In this paper different inverter modulation techniques are discussed which are used to analyse the system changes which occur due to the removal of transformer. This paper also presents some of the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor clamped inverter (flying capacitor) and cascaded-multilevel inverter.

Keywords: Modulation techniques, Inverter Topologies, Transformerless System

I. INTRODUCTION

As it can be noticed from the current market trends that power electronics technology is gaining sudden boom of demand because of its fast response and autonomous control. In near future this technology will be able to provide sufficient advantages in processing power from renewable energy sources. Various technologies have also been developed for PV inverters with the main purpose of reducing the maintenance cost and increasing the efficiency the system. Recently, many other countries have taken their steps for increasing the share of renewable energy in power plants (e.g. wind, solar, tidal etc.). Once the renewable energy is used as a major player of energy in future power systems, the conventional technology of regulating voltage will encounter various problems and the voltage quality of power grids will be lowered significantly.

II. PHOTOVOLTIC CELL

The photovoltaic effect was experimentally demonstrated by French physicist Edmond Becquerel. The world's first photovoltaic cell was developed by him in 1983. Willoughby Smith first described it as the "Effect of Light on Selenium during the passage of an Electric Current" in a 20th February 1873 issue of Nature. Charles Fritts built the first solid state photovoltaic cell by coating the semiconductor selenium with a thin layer of gold to form the junctions, the device was only around 1% efficient. A grid-connected PV system consists of solar panels, inverters, a power conditioning unit and grid connection equipment. The grid-connected PV system supplies the excess power, beyond consumption by the connected load, to the utility grid.

When PV is installed in grid, certain problems appear, as the PV panel is typically built in a sandwich structure, a capacitance to earth appears creating a path for leakage current. This can compromise personal safety and potential difference imposed by

switching action of the inverter which injects a capacitive ground current. The transformerless structure requires more complex solution, typically resulting in novel topologies in order to keep the leakage current and DC current injection under control in order to comply with the safety issue and to exhibit the high efficiency.

III. TRANSFORMERLESS CONCEPT

When power is transmitted to the grid using transformer, the size of the system is increased and system becomes more complex. Also, various types of losses such as iron losses, copper losses, hysteresis losses, eddy current losses, stray loss, and dielectric losses increases. When transformer is connected to the system the overall cost (installation as well as maintenance cost) increases.

Transformerless inverters are light, compact, and relatively in-expensive. Transformerless concept is advantageous because of their high efficiencies which reach up to 97-98% which is highly attractive for distributed power generator systems.

To make the system transformerless, certain multilevel inverter topologies are used which include an array of power semiconductors and capacitor voltage sources whose output generates voltages with stepped waveform. By adding the number of levels of the inverter, the output voltage will be a step voltage generating a staircase waveform which has reduced harmonic distortion. However, a high number of levels increases the complexity and introduce voltage Imbalance problem in the system. Three different topologies have been proposed for multilevel inverters:

1) Diode-Clamped Inverter (neutral-point clamped)
2) Capacitor-Clamped Inverter (flying capacitor)
3) Cascaded Multilevel Inverter

The most important features of multilevel inverters are:

1) They can generate output voltages with extremely low distortions.
2) They can draw input current with very low distortion.
3) They operate with a lower switching frequency.

IV. INVERTER TOPOLOGIES

A. Diode-Clamped Inverter

A three-level diode-clamped inverter is presented in below Fig. 1(a). In this circuit dc-voltage is split into three levels by two series-connected bulk capacitors C_1 and C_2. The middle point of the two capacitors (*n)* can be defined as the neutral point. The output voltage has 3 states $+V_{dc}/2$, 0 and $-V_{dc}/2$. For voltage level $+V_{dc}/2$ switches S_1 and S_2 need to be turned on, for $-V_{dc}/2$ switches S_1' and S_2' need to be turned on and for 0 level S_2 and S_1' need to be turned on. The key components that distinguish this circuit from a two-level inverter are diodes D_1 and D_1'. These two diodes clamp the switch voltage to half the level of the dc voltage. When both S_1 and S_2 are turned on, the voltage across a and 0 is V_{dc} i.e. $V_{an} = V_{dc}$. In this case D_1' balances out the voltage sharing between S_1' and S_2'. Note that the output voltage V_{an} is ac and V_{a0} is dc.

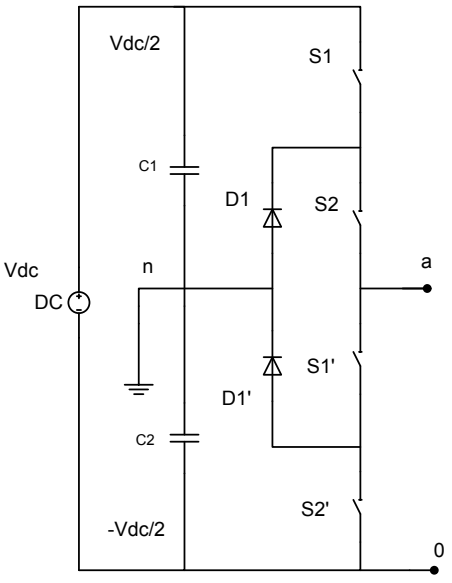

Figure 1(a). Three level Diode-Clamped Multilevel Inverter Circuit

Fig.1(b) shows a five-level diode-clamped inverter where the dc bus consists of four capacitors C_1, C_2, C_3

and C_4. For dc-voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$.

To explain the synthesis of staircase voltage, the neutral point (n) is considered as the reference point. There are five switch combinations to synthesize five-level voltages across a and n.

1) For voltage level $V_{an} = V_{dc}/2$, turn ON all upper switches from S_1 to S_4.

2) For voltage level $V_{an} = V_{dc}/4$, turn ON three upper switches $S_2 – S_4$ and one lower switch S_1'.

3) For voltage level $V_{an} = 0$, turn ON two upper switches S_3 and S_4 and two lower switches S_1' and S_2'.

4) For voltage level $V_{an} = -V_{dc}/4$, turn ON one upper switch S_4 and three lower switches $S_1' – S_3'$.

5) For voltage level $V_{an} = -V_{dc}/2$, turn ON all lower switches S_1' to S_4'.

Four complementary switch pairs exist in each phase. The complementary switch pair is defined such that turning on one of the switches will exclude the other from being turned on. In this example, the four complementary pairs are (S_1, S_1'), (S_2, S_2'), (S_3, S_3'), and (S_4, S_4').

The number of diodes required for each phase will be (m-1) * (m-2).

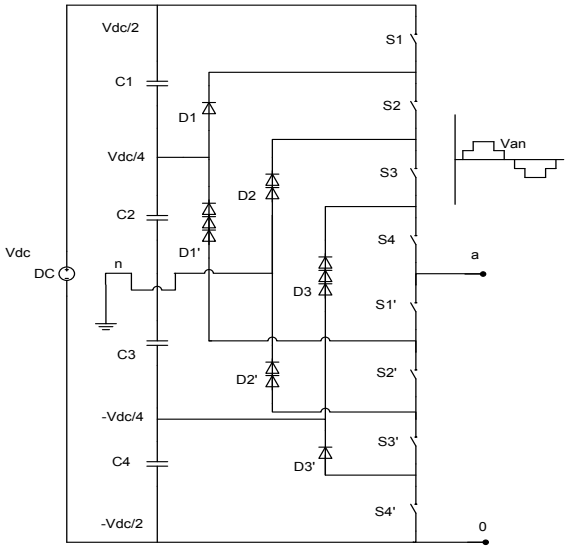

Figure 1(b). Five level Diode-Clamped Multilevel Inverter Circuit

B. Capacitor-Clamped Inverter

Fig.2 shows one phase-leg of capacitor-clamped inverter. The inverter is also called the flying capacitor inverter. The independent capacitors clamping the device voltage to one capacitor voltage level. The inverter in Fig. 2 shows a three-level output across a and n, i.e. $V_{an} = V_{dc}/2$, 0 or $-V_{dc}/2$. For voltage level $V_{dc}/2$, switches S_1 and S_2 needs to be turned on, for $-V_{dc}/2$ switches S_1 and S_2 need to be turned on and for 0 level voltage either pair (S_1, S_1') or (S_2, S_2') needs to be turned on. Clamping capacitor C_1 is charged when S_1 and $S_1'$are turned on and is discharged when S_2 and S_2' are turned on.

The voltage output of a five-level capacitor-clamped converter has more flexibility as compared to a diode-clamped converter of same level. The neutral point (n) and V_{an} can be synthesized by the following switch combinations-

1) For voltage level $V_{an} = V_{dc}/2$, turn on all upper switches $S_1 – S_4$.

2) For voltage level $V_{an} = V_{dc}/4$, there are three combinations:

a) S_1, S_2, S_3, S_1'.

b) S_2, S_3, S_4, S_4'.

c) S_1, S_3, S_4, S_3'.

3) For voltage level $V_{an} = 0$, there are six combinations:

a) S_1, S_2, S_1', S_2'.

b) S_3, S_4, S_3', S_4'.

c) S_1, S_3, S_1', S_3'.

d)S_1, S_4, S_2', S_3'.

e) S_2, S_4, S_2', S_4'.

f) S_2, S_3, S_1', S_4'.

4) For voltage level $V_{an} = -V_{dc}/4$, there are three combinations:

a) S_1, S_1', S_2', S_3'.

b) S_4, S_2', S_3', S_4'.

c) S_3, S_1', S_3', S_4'.

5) For voltage level $V_{an} = -V_{dc}/2$, turn on all lower switches $S_1' – S_4'$.

The capacitors with positive polarity are in discharging mode, whereas those with negative polarity are in charging mode. By selecting the proper combination of capacitors, it is possible to balance the capacitor charge. Similar to diode clamping, this also requires a large number of bulk capacitors to clamp the voltage.

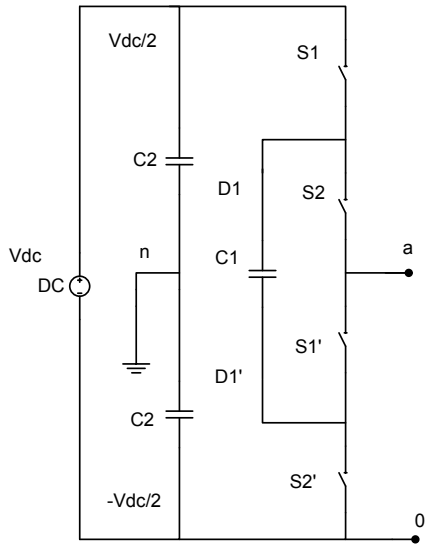

Figure 2. Three level Capacitor-Clamped Multilevel Inverter Circuit

C. Cascaded Multilevel Inverter

Another converter topology can be used in transformerless system, which is based on the series connection of several single-phase inverters. Fig.3 shows the circuit diagram of one phase leg of a nine-level inverter. The resulting phase voltage is obtained by the addition of the voltages generated by the different cells. Each single-phase full-bridge inverter generates three voltages of the output: $+V_{dc}$, 0 and $-V_{dc}$. The resulting output ac voltage varies from $-4V_{dc}$ to $+4V_{dc}$ and the staircase waveform is nearly sinusoidal even without filtering.

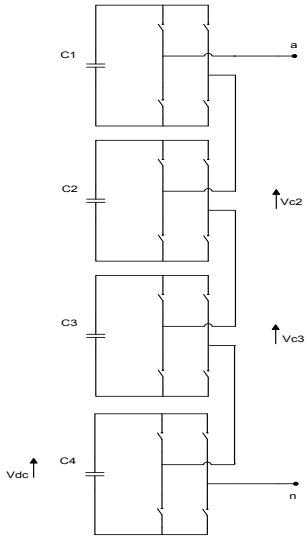

Figure 3. Cascaded Multilevel Inverter Circuit

V. MODULATION TECHNIQUES

Different PWM switching patterns can be used in transformerless single phase inverter bridges. The main modulation strategies used are:

(a) Bipolar Modulation

(b) Unipolar Modulation

Fig.4 shows a simplified circuit diagram of a single-phase H-bridge inverter. It is composed of 2 inverter legs with 2 IGBT devices in each leg. The inverter dc bus voltage V_d is usually fixed, while its ac output voltage V_{AB} can be adjusted by either bipolar or unipolar modulation schemes.

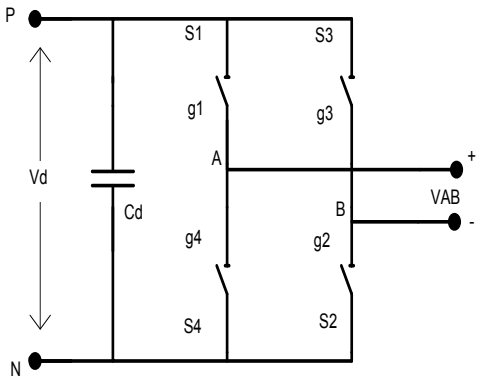

Figure 4. Single-phase H-bridge Inverter

A. Bipolar Pulse-Width Modulation

Fig.5 shows a set of typical waveforms of the H-bridge inverter with bipolar modulation, where v_m is the sinusoidal modulating wave, v_{cr} is the triangular carrier wave, and v_{g1} and v_{g3} are the gate signals for the upper switches S_1 and S_3, respectively. The upper and the lower switches in the same inverter leg operate in a complementary manner with one switch turned on and the other turned off. Thus, we only need to consider two independent gate signals, v_{g1} and v_{g3}, which are generated by comparing v_m with v_{cr}. Since the waveform of v_{AB} switches between the positive and negative dc voltages $\pm V_d$ and $-V_d$ this scheme is known as bipolar modulation. The switching frequency of the IGBT device, referred to as device switching frequency f_{sw} is equal to the carrier frequency f_{cr}.

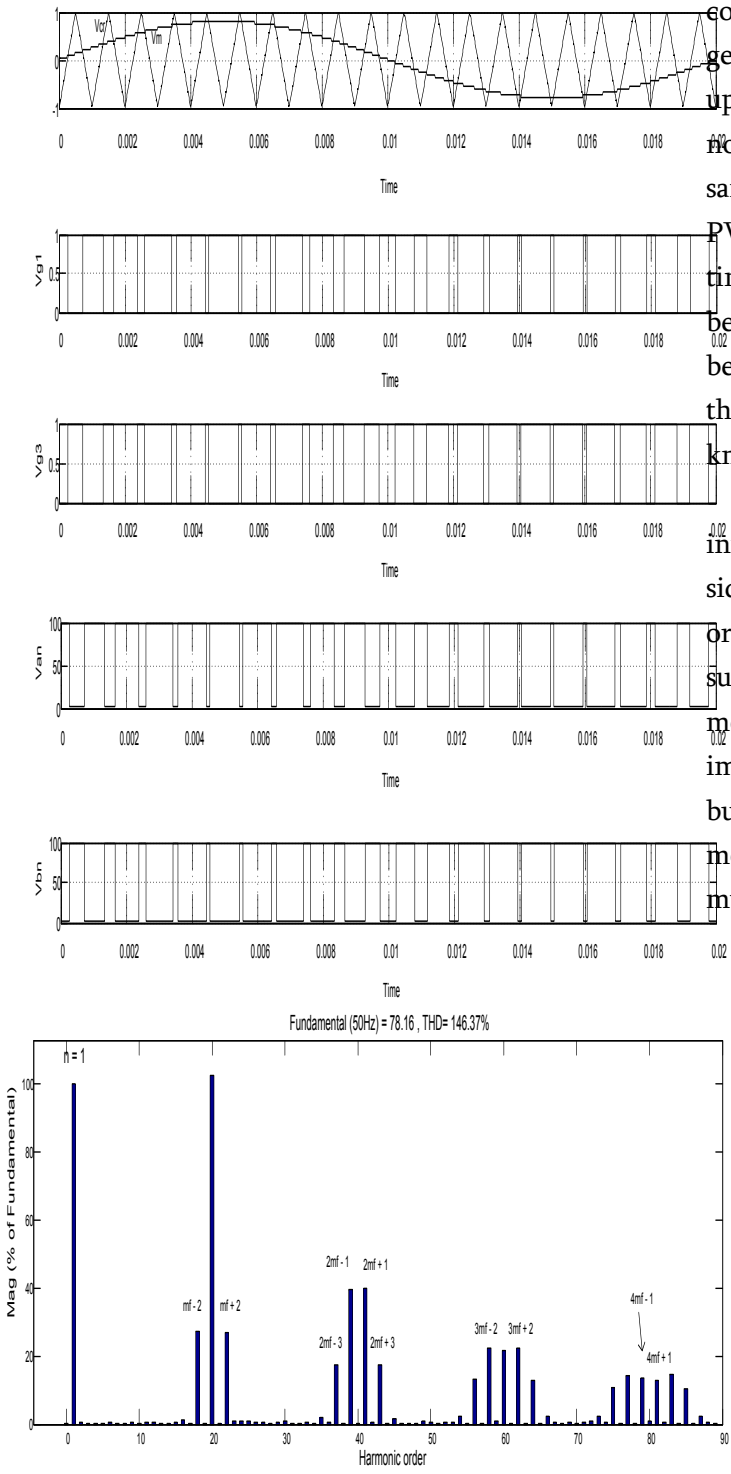

Figure 5. Bipolar PWM for the H-bridge inverter operating at mf = 20, ma = 0.8, fm = 50 Hz, and fcr = 1000 Hz.

B. Unipolar Pulse-Width Modulation

The unipolar modulation requires two sinusoidal modulating waves, vm and -vm of the same magnitude and frequency but 180° out of phase as shown in Fig.6(a). The two modulating waves are compared with a common triangular carrier wave vcr, generating two gating signals, vg1 and vg3, for the upper switches, S1 and S3, respectively. It can be noted that the 2 upper devices do not switch at the same time, which is distinguished from the bipolar PWM where all four devices are switched at the same time. The inverter output voltage vAB switches either between 0 and +Vd during the positive half-cycle or between 0 and –Vd during the negative half-cycle of the fundamental frequency. Thus, this scheme is known as unipolar modulation

Fig.6(b) shows the harmonic spectrum of the inverter output voltage vAB. The harmonics appear as sidebands centred around 2mf and 4mf. The low-order harmonics generated by the bipolar modulation, such as mf and mf ± 2, are eliminated by the unipolar modulation. The unipolar modulation can also be implemented by using only one modulating wave vm but two phase-shifted carrier waves, vcr and -vcr. This modulation technique is often used in the CHB multilevel inverters.

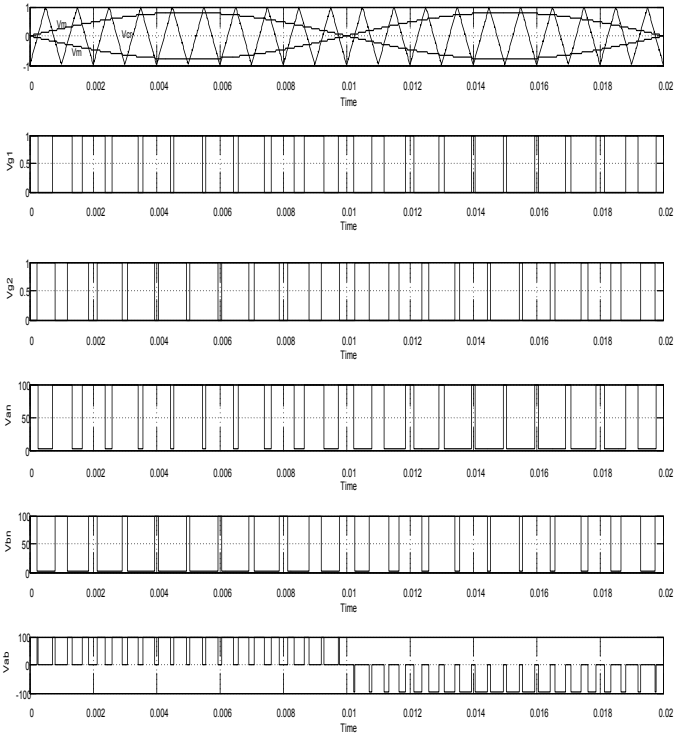

Figure 6(a). Unipolar PWM with two phase-shifted modulating waves (mf = 20, ma = 0.8, fm = 50 Hz and fcr = 1000 Hz).

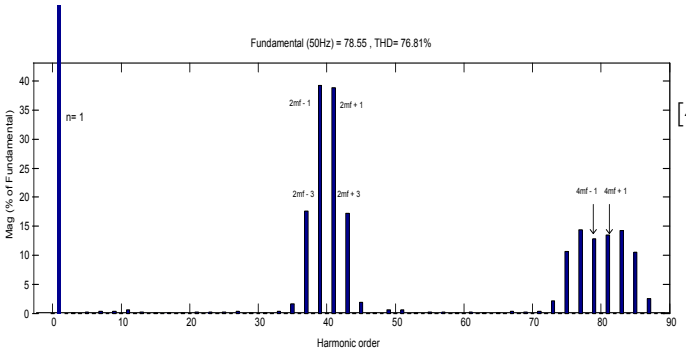

Figure 6(b). Harmonic Spectrum

VI. CONCLUSION

In this paper several topologies without transformer suitable for low power grid connected systems have been studied. Both topologies and modulation techniques have a great effect on PV based grid connected inverters. Amongst these topologies cascaded multilevel inverter topology has been identified as the most promising topology. With the use of this topology measures are necessary to decrease the capacitive current which is caused by the potential difference imposed on PV array. Two modulation techniques have been discussed briefly and the waveforms as well as THD results have been shown. Unipolar modulation is better than bipolar as it eliminates the lower order harmonics which is good for the system.

VII. REFERENCES

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