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A Unified Anti-Windup Scheme For PID Controllers

T. Bhuvanendhiran[1], Dr. S. Abraham Lincon[2]

[1]Research Scholar, Department of Electronics & Instrumentation Engineering, Annamalai University, Chidambaram, Tamil Nadu, India

[2]Professor, Department of Electronics & Instrumentation Engineering, Annamalai University, Chidambaram, Tamil Nadu, India

tbhuvanendhiran@yahoo.co.in[1], linsun_2k5@yahoo.co.in[2]

ABSTRACT

This paper presents an anti-windup scheme for PID controllers. The designed work is based on back-calculation and conditional integration schemes. A combined anti-windup scheme is used to eliminate the drawback of back- calculation and conditional integration schemes. Particularly, this scheme it can ensure a better performance for processes with various normalised delay times, an extra tuning parameters are not necessary. Thus, it is more appropriate for execution of industrial regulators due its simplicity.

Keywords: Anti-Wind Up, PID Controller, Normalised Delay Time, Saturation

I. INTRODUCTION

Proportional- Integral- derivative (PID) controllers are most widely used in various industrial settings in spite of several devised control strategies have been developed in the field of automatic control system. On the other hand the PID controller performances are affected in the presence of saturation actuators, which cause the integrator windup [1]. To design the controller to eliminate the integrator windup problem, the actuator constraints has to be taken in to the account, and prevent the degradation of PID performance, subsequently to include an anti-windup compensation scheme. In this scenario a number of schemes have been work out to design the compensator [2, 3]. Mainly they belong to two altered approaches, that is to say, conditional integration and back calculation [4]. Also the conditioning scheme presented in [5, 6]. However, due to a considerable delay time in the process, these schemes are not suitable. They might need an additional tuning attempt, which is objectionable for industrialized regulators. for that reason, a combined anti-windup scheme are implemented to the first order process with various normalised delay times, since the integrator windup occur in lower order process.

II. ANTI- WINDUP SCHEMES FOR PID CONTROLLERS

A. Generalities

The PID controller is described in the Laplace domain:

$$U(s) = Kp\left(E(s) + \frac{1}{T_i s}E(s) - \frac{sTd}{1+s(Td/N)}Y(s)\right) \qquad (1)$$

Where K_p is the proportional gain

T_i is the integral time constant

T_d is the derivative time constant and

N is generally set the value between 5 and 33 [7].

The integrator windup occurs, when a step change in input causes the actuator to saturate. Then the system error decrease more slowly than in the ideal one. Consequently, the value of the integral term becomes huge. As a result, the value of output reaches that of input, the controller still saturates due to the integral term and usually leads to big overshoots and settling times. In general, the integrator windup mainly occurs when a step is applied to the reference set point signal rather than the manipulated variable [8].when the process is a lower order the integrator windup mostly takes place. For these reasons, the first order plus delay time systems are consider in this work.

B. Conditional Integration Scheme

To avoid integrator windup, the Conditional Integration can be adopted. In this Scheme, the integral term is increased only when certain conditions are satisfied, otherwise it is kept constant.

The diverse cases can be described as follows:

1. The integral term is limited to a selected value
2. The integration is stopped when the system error is large, i.e. when $|e| > \bar{e}$ where $\bar{e}$ is a selected value
3. The integration is stopped when the controller saturates, i.e. when $u \neq u_s$
4. The integration is stopped when the controller saturates and the system error and the manipulated variable have the same sign, i.e. when $u \neq u_s$ and $e \times u > 0$.

The above methods have been implemented and compared, fourth case is the best one [4, 9].figure .1 Shows the conditional integration anti-windup scheme.

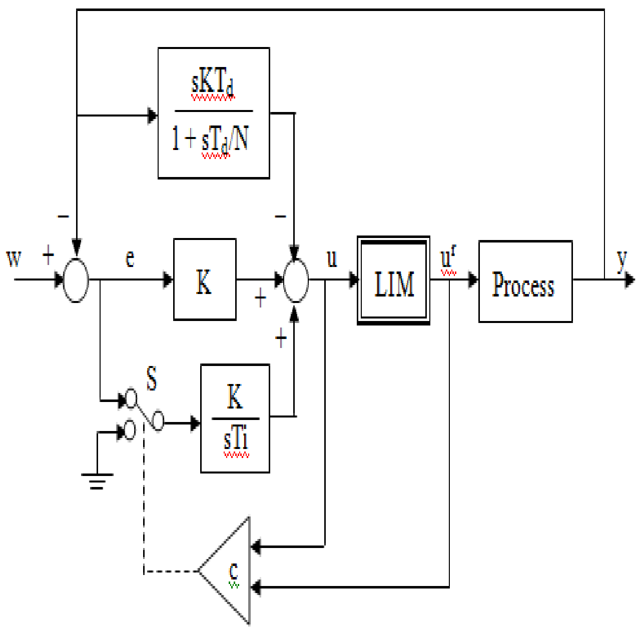

Figure 1. Anti-Windup Scheme of Conditional Integration.

C. Back- Calculation scheme

The back calculation scheme is the substitute approach of conditional integration scheme. Once the controller saturates, it recomputed the integral term. Whenever the difference occurs between saturated and unsaturated control signal, eventually the integral value is decreased by means of feedback, as shown in Figure 2. The integrator input (e_i), as shown in equation (2). Where T_t is called tracking time constant, it determines the rate at which the integral term is reset and its choice of value gives the performances of the complete control scheme.

$$e_i = \frac{K_p}{T_i} e + \frac{1}{T_t}(u_s - u) \qquad (2)$$

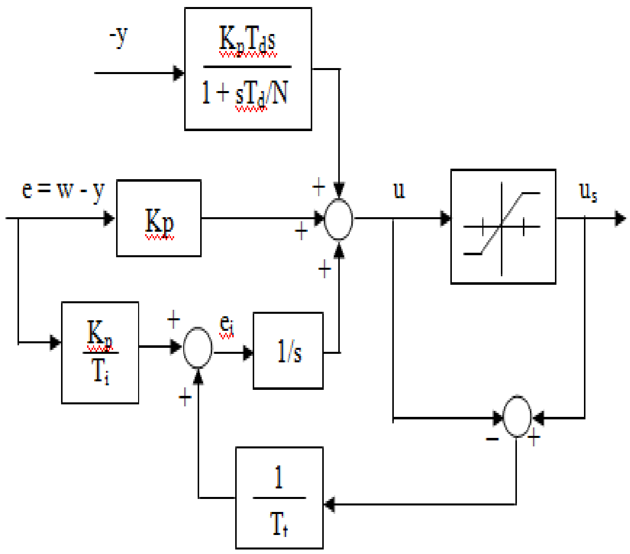

Figure 2. Anti-Windup scheme of Back-Calculation

D. Combined Scheme

A simple modification is made in combined scheme, to overcome the drawbacks between conditional integration and back calculation scheme. In particular, the back-calculation works when the controller Saturates, the system error has the same sign of the manipulated variable and the system output has left from before reference value. This can be stated as:

$$e_i = \begin{cases} \frac{K_p}{T_i} e + \frac{1}{T_t}(u_s - u), & \text{if } u \neq u_s \, and \, u \times e > 0 \\ \frac{K_p}{T_i} e & \text{otherwise} \end{cases} \quad (3)$$

The intension of (3) is to permit an increase in the integral term, while the process output (transient) has not started due the delay time. The combined scheme basically performs as the standard back calculation scheme when delay time is small. In any case, it is possible to set a single value for T_t for various cases. And this value can be considerably lesser than T_i allowing improved performance for small normalized delay times.

III. SIMULATION RESULTS

Different anti-windup schemes are designed and incorporated to the various processes with different normalized delay times θ_1=0.2 and θ_2=0.4, which is depicted in following:

$$P_1(s) = \frac{1}{10s+1} e^{-2S} \quad (4)$$

$$P_2(s) = \frac{1}{10s+1} e^{-4S} \quad (5)$$

For both processes, Ziegler-Nichols formula has been applied, to get the PID parameters tuning values, the values are described in Table 1.

Parameter	$P_1(s)$	$P_2(s)$
K_p	6	3
T_i	4	8
Td	1	2
N	10	10

Table 1.PID Tuning Parameters Values

A positive unit step input has been applied to the system and output of the system with different anti-windup schemes for process $p_1(s)$ and $P_2(s)$ are shown in figure 3, figure 4, figure 5 and figure 6. And also without anti-windup scheme for process $P_1(s)$ and $P_2(s)$ are shown in figure 7 and figure 8. The observations made from responses and performance criteria, the combined scheme provided better performance for both first order processes with various normalized delay times. Particularly the overshoot and settling times are very less when compared to without anti-windup schemes. The table 2 and 3 shows the performance criteria of process $P_1(s)$ and $P_2(s)$.

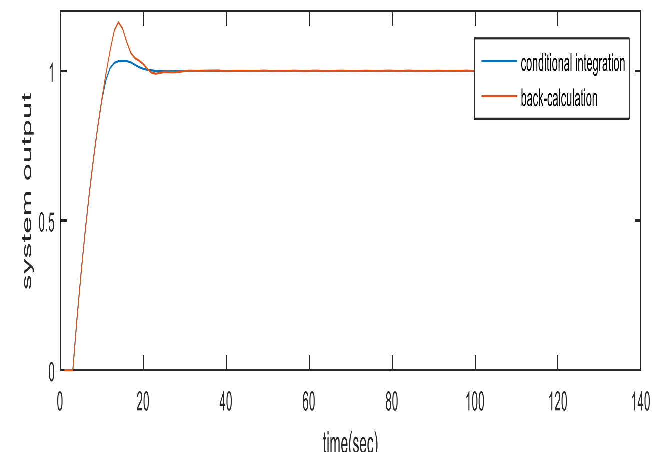

Figure 3. Step Response for P1(S) For the Considered Anti-Windup Schemes

Conditional integration 2. Back-calculation with Tt=Ti

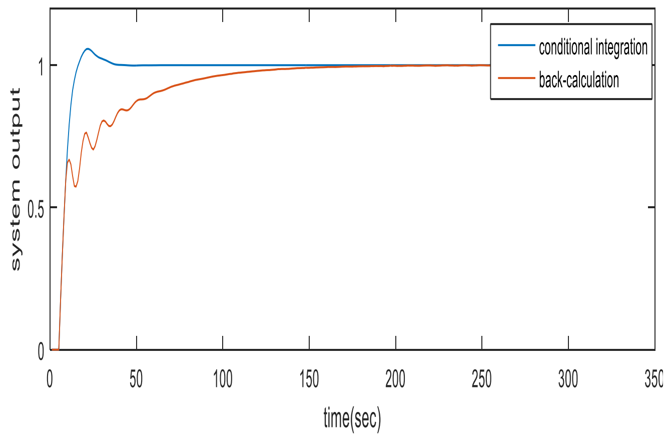

Figure 4. Step Response for $P_2(S)$ For the Considered Anti-Windup Schemes

1. Conditional integration 2. Back-Calculation with T_t=T_i

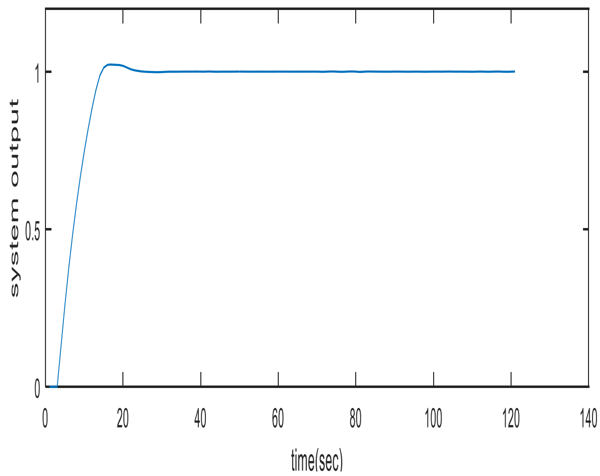

Figure 5. Step Response for $P_1(S)$ For the Combined Anti-Windup Schemes

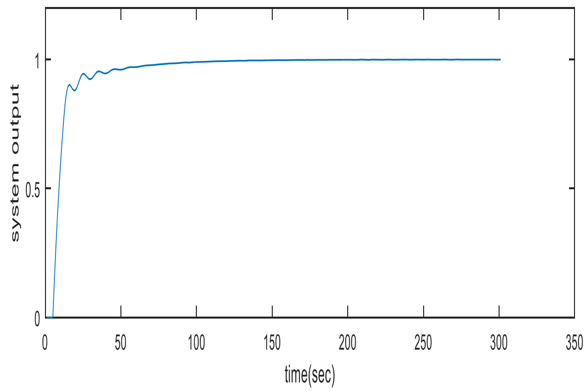

Figure 6. Step Response for $P_2(S)$ For the Combined Anti-Windup Schemes

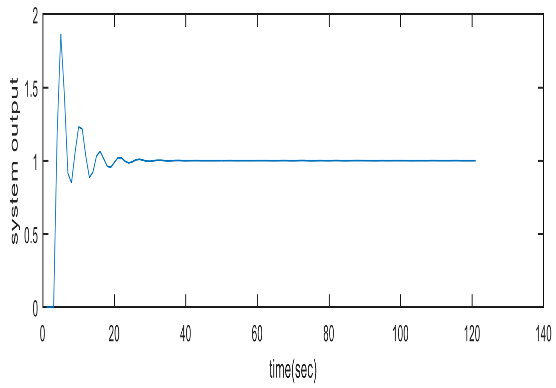

Figure 7. Step Response for P1 (S) For Without Anti-Windup Schemes

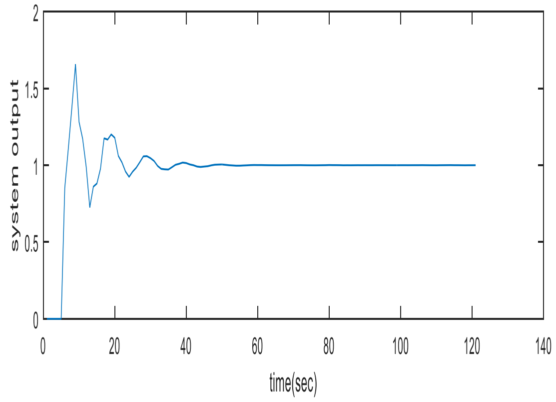

Figure 8. Step Response for P2 (S) For Without Anti-Windup Schemes

Table 3. Comparison Criteria for Process $P_1(s)$

Schemes	ISE	IAE	Settling Time (t_s) in secs.	% over shoot (% M_p)
Without anti-windup	3.03	4.85	21.10	86.47

Conditional Integration	4.82	6.75	18.02	3.36
Back Calculation	4.791	7.09	22.42	11.43
Combined Scheme	4.82	6.76	19.27	2.20

Table 4. Comparison Criteria for Process $P_2(s)$

Schemes	ISE	IAE	Settling Time (t_s) in secs.	% over shoot (% M_p)
No anti-windup	4.95	7.78	35.52	65.75
Conditional Integration	6.24	8.39	31.11	5.75
Back Calculation	9.75	22.8	118.02	0.05
Combined Scheme	6.95	12.16	72.67	0.01

IV. CONCLUSION

Combined anti-windup scheme for PID controller has been implemented to the first order process with delay time, this combined scheme offer good performance over a wide range of processes without any extra tuning effort from the control system engineer. And it is very suitable to adopt the industrial regulators due to its overall simplicity.

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